1-MHz, 45-µA CMOS RAIL-TO-RAIL OPERATIONAL AMPLIFIER

Check for Samples: OPA2348-HiRel

FEATURES

- **0°C to 70°C Known Good Die**
- **Separated (Sawn) Die Mounted on Wafer Tape**
- **Controlled Baseline**
- **Low Quiescent Current (I_Q): 45 µA (Typ)**
- **Low Cost**
- **Rail-to-Rail Input and Output**
- **Single Supply: 2.1 V to 5.5 V**
- **Input Bias Current: 0.5 pA (Typ)**
- **High Speed:Power With Bandwidth: 1 MHz**

APPLICATIONS

- **Portable Equipment**
- **Battery-Powered Equipment**
- **Smoke Alarms**
- **CO Detectors**
- **Medical Instrumentation**

DESCRIPTION

The OPA2348 is a single-supply low-power CMOS operational amplifier. Featuring an extended bandwidth of 1 MHz and a supply current of 45 µA, the OPA2348 is useful for low-power applications on single supplies of 2.1 V to 5.5 V.

Low supply current of 45 µA and an input bias current of 0.5 pA make the OPA2348 an optimal candidate for low-power high-impedance applications such as smoke detectors and other sensors.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	KGD	OPA2348CKGD4	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
10 mils.	Silicon with backgrind	V-	Al-Si-Cu (0.5%)

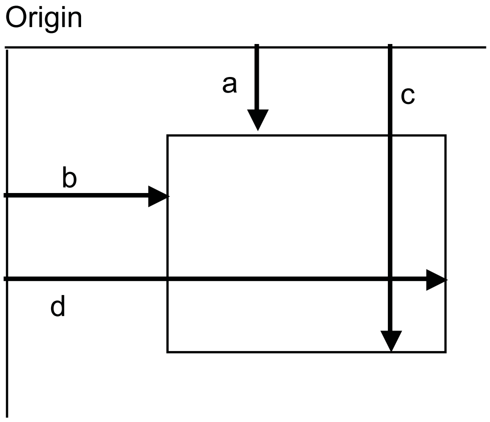
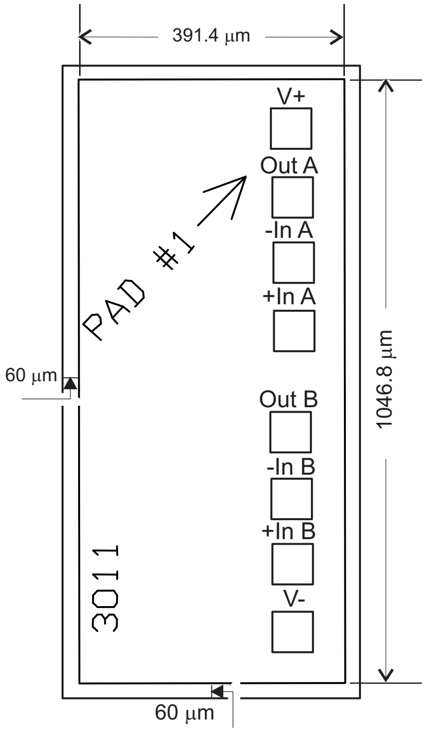


Table 1. BOND PAD COORDINATES

DESCRIPTION	PAD NUMBER	a	b	c	d
V+	1	965.6	5	1041.8	81.2
Out A	2	839.4	5	915.6	81.2
-In A	3	713.2	5	789.4	81.2
+In A	4	587	5	663.2	81.2
Out B	5	383.6	5	459.8	81.2
-In B	6	257.4	5	333.6	81.2
+In B	7	131.2	5	207.4	81.2
V-	8	5	5	81.2	81.2


391.4 µm
1046.8 µm
60 µm
60 µm
V+
Out A
-In A
+In A
Out B
-In B
+In B
V-
PAD #1
3011

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_S	Supply voltage, V– to V+	7.5 V
V_{IN}	Input voltage, signal input terminals(2)	(V– – 0.5 V) to (V+ + 0.5 V)
I_{IN}	Input current, signal input terminals(2)	10 mA
	Output short-circuit duration(3)	Continuous
θ_{JA}	Thermal impedance, junction to free air(4)	97.1°C/W
T_A	Operating free-air temperature	0°C to 70°C
T_{STG}	Storage temperature	–0°C to 70°C
T_J	Operating virtual-junction temperature	70°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.1	5.5	V
T_A	Operating free-air temperature	0	70	°C

ELECTRICAL CHARACTERISTICS

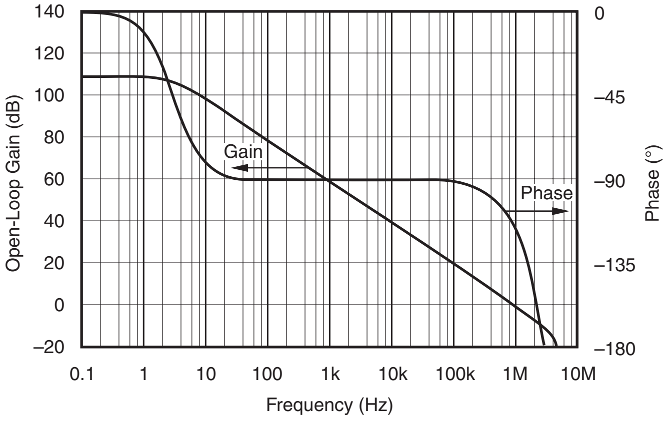
V_S = 2.5 V to 5.5 V, R_L = 100 kΩ connected to V_S/2, V_{OUT} = V_S/2 (unless otherwise noted)

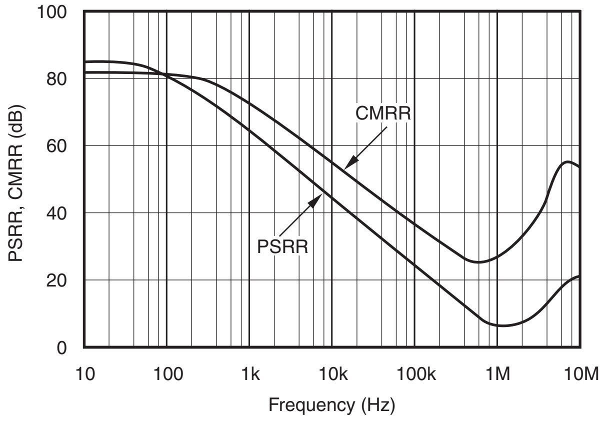
PARAMETER			TEST CONDITIONS	T_A [1]	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage		V_S = 5 V, V_{CM} = (V–) + 0.8 V	25°C		1	5	mV
				Full range			6	
$\Delta V_{OS}/\Delta T$	Offset voltage drift over temperature			Full range		4		μV/°C
PSRR	Offset voltage drift vs power supply		V_S = 2.5 V to 5.5 V, V_{CM} < (V+) – 1.7 V	25°C		60	175	μV/V
				Full range			300	
	Offset voltage channel separation		dc	25°C		0.2		μV/V
			f = 1 kHz	25°C		134		dB
V_{CM}	Input common-mode voltage range			25°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Input common-mode rejection ratio		(V–) – 0.2 V < V_{CM} < (V+) – 1.7 V	25°C	70	82		dB
				Full range	66			
			V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V	25°C	60	71		
			V_S = 5.5 V, (V–) < V_{CM} < (V+)	Full range	56			
I_B	Input bias current			25°C		±0.5	±10	pA
I_{OS}	Input offset current			25°C		±0.5	±10	pA
Z_I	Input impedance		Differential	25°C		10^{13}‖3		Ω‖pF
			Common-mode			10^{13}‖3		
	Input voltage noise		V_{CM} < (V+) – 1.7 V, f = 0.1 Hz to 10 Hz	25°C		10		μV_{PP}
V_n	Input voltage noise density		V_{CM} < (V+) – 1.7 V, f = 1 kHz	25°C		35		nV/√Hz
I_n	Input current noise density		V_{CM} < (V+) – 1.7 V, f = 1 kHz	25°C		4		fA/√Hz
A_{OL}	Open-loop voltage gain		V_S = 5 V, R_L = 100 kΩ, 0.025 V < V_O < 4.975 V	25°C	94	108		dB
				Full range	90			
			V_S = 5V, R_L = 5 kΩ, 0.125 V < V_O < 4.875 V	25°C	90	98		
				Full range	88			
	Voltage output swing from rail		RL = 100 kΩ, A_{OL} > 94 dB	25°C		18	25	mV
				Full range			25	
			RL = 5 kΩ, A_{OL} > 90 dB	25°C		100	125	
				Full range			125	
I_{SC}	Output short-circuit current			25°C		±10		mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*	25°C				
GBW	Gain-bandwidth product		C_L = 100 pF	25°C		1		MHz
SR	Slew rate		C_L = 100 pF, G = +1	25°C		0.5		V/μs
t_s	Settling time	0.1%	C_L = 100 pF, V_S = 5.5 V, 2V- step, G = +1	25°C		5		μs
		0.01%				7		
	Overload recovery time		V_{IN} × Gain > V_S	25°C		1.6		μs
THD+N	Total harmonic distortion plus noise		C_L = 100 pF, V_S = 5.5 V, V_O = 3 V_{PP}, G = +1, f = 1 kHz	25°C		0.0023		%
I_Q	Quiescent current		Per amplifier	25°C		45	65	μA
				Full range			75	

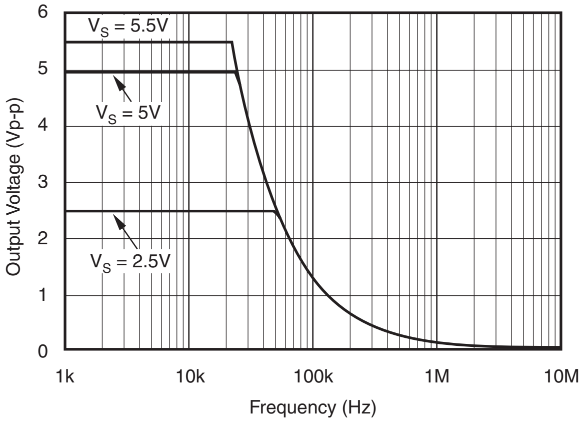
(1) Full range T_A = 0°C to 70°C

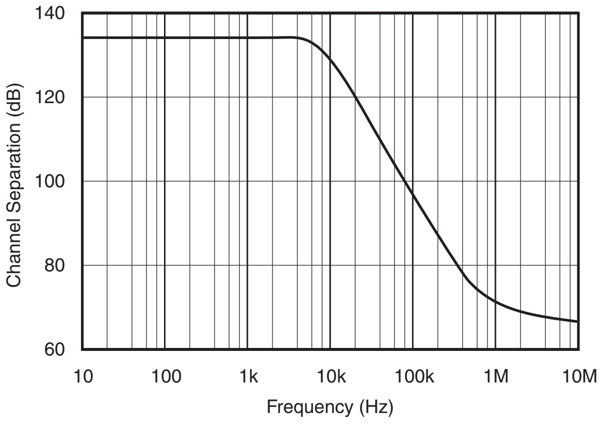
TYPICAL CHARACTERISTICS

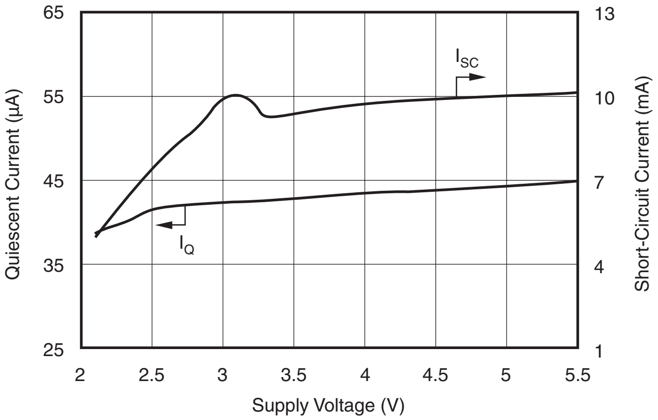
T_A = 25°C, R_L = 100 kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$ (unless otherwise noted)

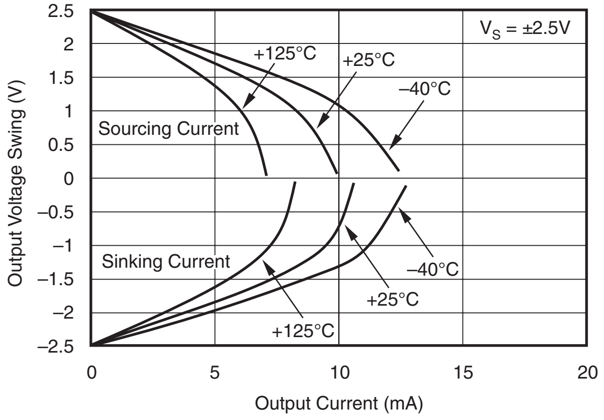

OPEN-LOOP GAIN AND PHASE vs FREQUENCY


PSRR AND CMRR vs FREQUENCY


MAXIMUM OUTPUT VOLTAGE vs FREQUENCY


CHANNEL SEPARATION vs FREQUENCY

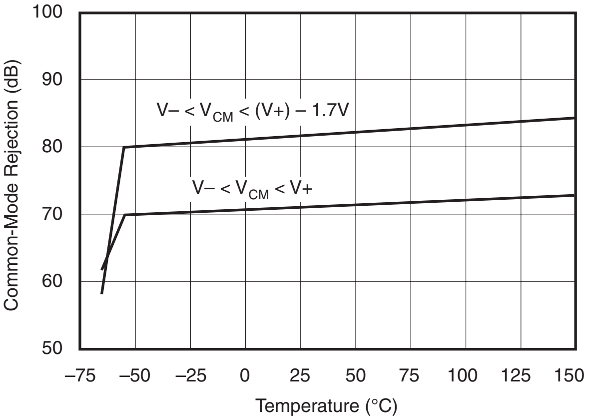

QUIESCENT AND SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

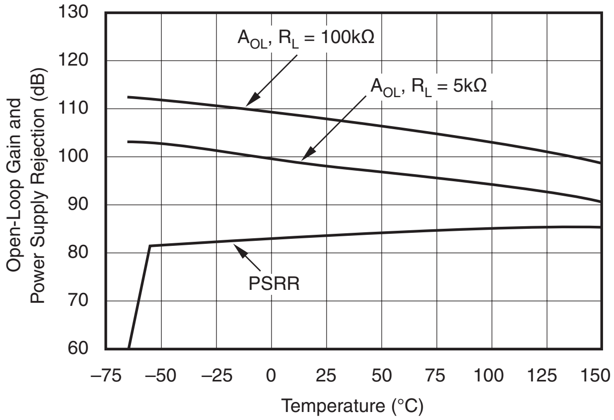
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, R_L = 100 kΩ connected to $V_S/2$, $V_{OUT} = V_S/2$ (unless otherwise noted)

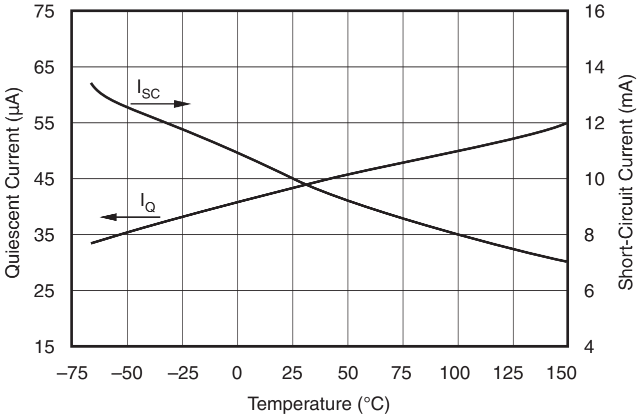
COMMON-MODE REJECTION vs TEMPERATURE



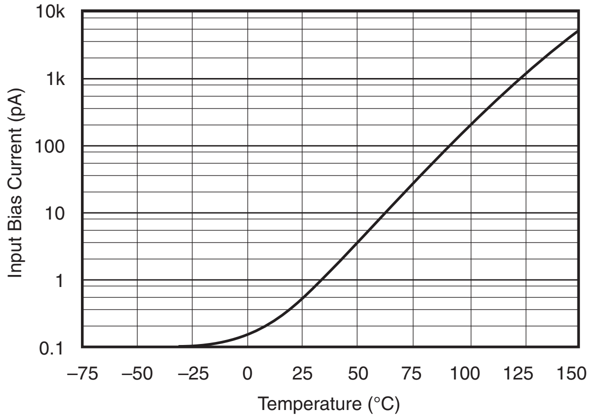
OPEN-LOOP GAIN AND PSRR vs TEMPERATURE



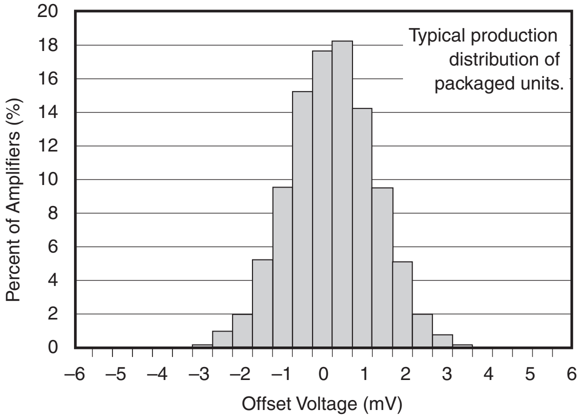
QUIESCENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



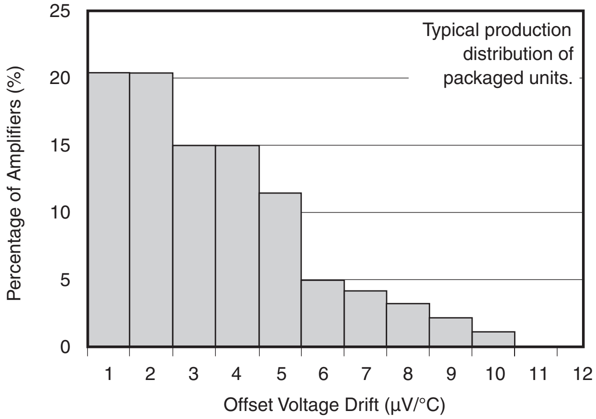
INPUT BIAS (I_B) CURRENT vs TEMPERATURE



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



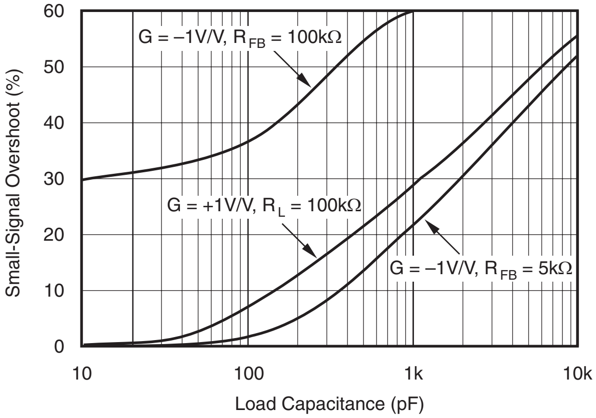
OFFSET VOLTAGE DRIFT MAGNITUDE PRODUCTION DISTRIBUTION



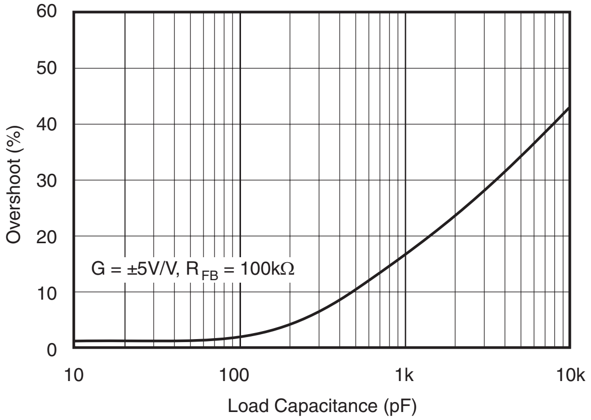
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, R_L = 100 kΩ connected to V_S/2, V_{OUT} = V_S/2 (unless otherwise noted)

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

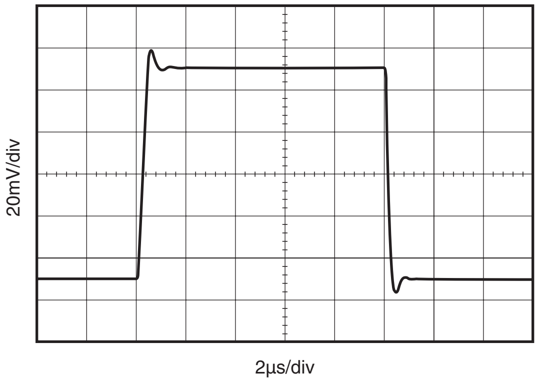


PERCENT OVERSHOOT vs LOAD CAPACITANCE



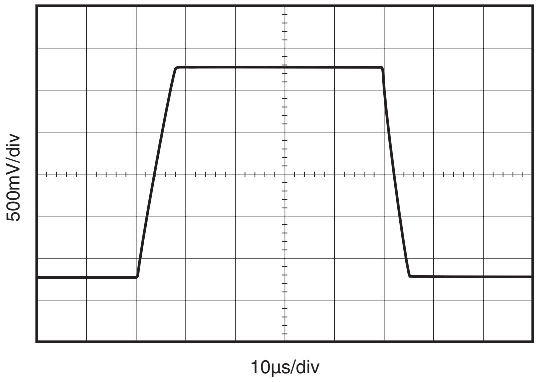
SMALL-SIGNAL STEP RESPONSE

G = +1V/V, R_L = 100kΩ, C_L = 100pF

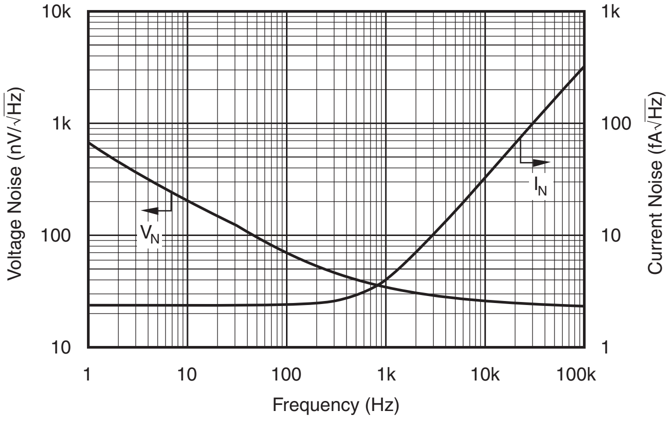


LARGE-SIGNAL STEP RESPONSE

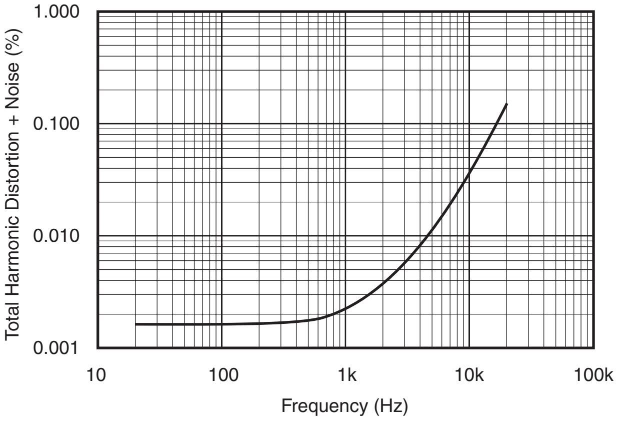
G = +1V/V, R_L = 100kΩ, C_L = 100pF



INPUT CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



APPLICATION INFORMATION

OPA2348 op amps are unity-gain stable and suitable for a wide range of general-purpose applications.

The OPA2348 features wide bandwidth and unity-gain stability with rail-to-rail input and output for increased dynamic range. Figure 1 shows the input and output waveforms for the OPA2348 in unity-gain configuration. Operation is from a single 5-V supply with a 100-kΩ load connected to $V_S/2$. The input is a 5-V_{PP} sinusoid. Output voltage is approximately 4.98 V_{PP}.

Power-supply pins should be bypassed with 0.01-μF ceramic capacitors.

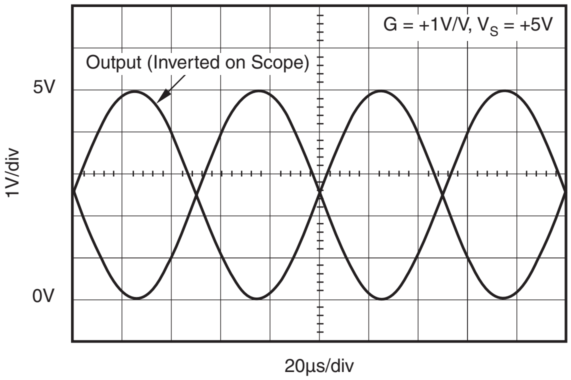


Figure 1. Rail-to-Rail Input/Output

Operating Voltage

OPA2348 op amps are fully specified and tested from 2.5 V to 5.5 V. However, supply voltage may range from 2.1 V to 5.5 V. Parameters are tested over the specified supply range, a unique feature of the OPA2348. In addition, all temperature specifications apply from 0°C to 70°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics*.

Common-Mode Voltage Range

The input common-mode voltage range of the OPA2348 extends 200 mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.2 V to 300 mV above the positive supply, while the P-channel pair is on for inputs from 300 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region, shown in Figure 2, can vary ±300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within the 200-mV transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

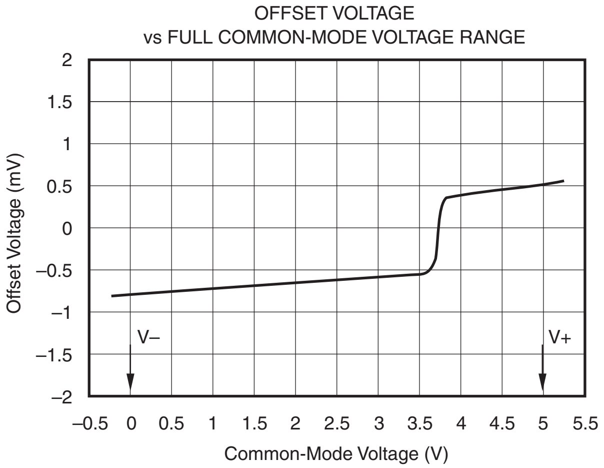


Figure 2. Behavior of Typical Transition Region at Room Temperature

Rail-to-Rail Input

The input common-mode range extends from (V–) – 0.2 V to (V+) + 0.2 V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500 mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, do not cause any damage to the op amp. Unlike some other op amps, if input current is limited the inputs may go beyond the power supplies without phase inversion, as shown in Figure 3.

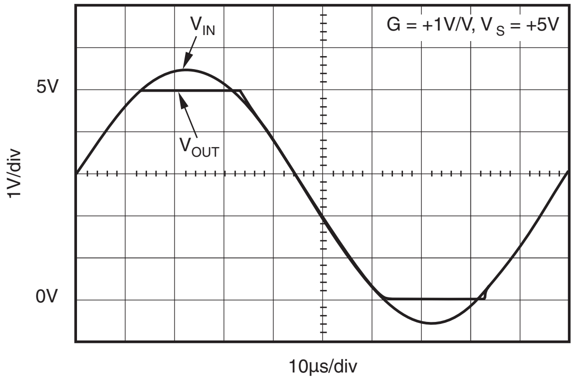


Figure 3. No Phase Inversion With Inputs Greater Than Power-Supply Voltage

Normally, input currents are 0.5 pA. However, large inputs (greater than 500 mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10 mA. This is easily accomplished with an input voltage resistor, as shown in Figure 4.

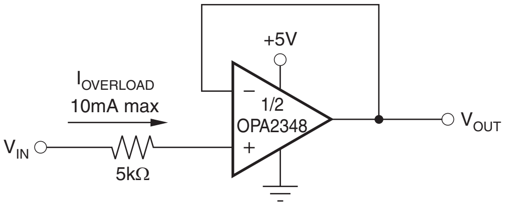


Figure 4. Input Current Protection for Voltages Exceeding the Supply Voltage

Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 5-kΩ loads connected to any potential between V+ and ground. For light resistive loads (>100 kΩ), the output voltage can typically swing to within 18 mV from supply rail. With moderate resistive loads (10 kΩ to 50 kΩ), the output voltage can typically swing to within 100 mV of the supply rails while maintaining high open-loop gain (see the typical characteristic "Output Voltage Swing vs Output Current").

Capacitive Load and Stability

The OPA2348 in a unity-gain configuration can directly drive up to 250-pF pure capacitive load. Increasing the gain enhances the amplifier’s ability to drive greater capacitive loads (see the typical characteristic "Small-Signal Overshoot vs Capacitive Load"). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10 Ω to 20 Ω) resistor, R_S, in series with the output, as shown in Figure 5. This significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a direct current (dc) error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L and is generally negligible.

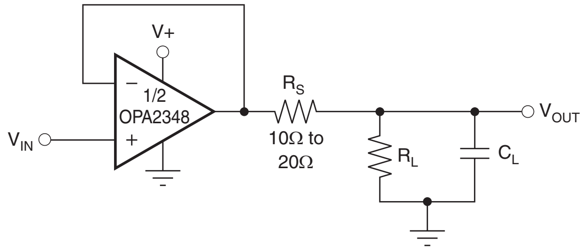


Figure 5. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small-valued resistors. For example, when driving a 500-pF load, reducing the resistor values from 100 kΩ to 5 kΩ decreases overshoot from 55% to 13% (see the typical characteristic "Small-Signal Overshoot vs. Load Capacitance"). However, when large valued resistors cannot be avoided, a small (4 pF to 6 pF) capacitor, C_{FB}, can be inserted in the feedback, as shown in Figure 6. This significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the amplifier's input capacitance and PC board parasitic capacitance.

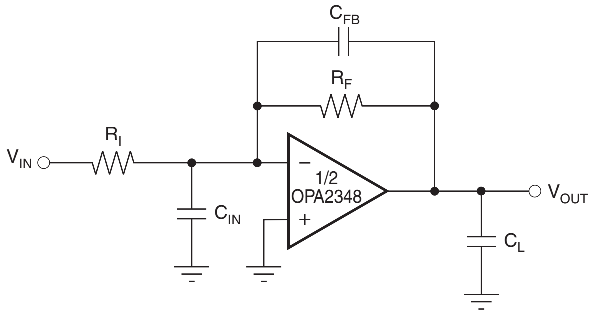


Figure 6. Improving Capacitive Load Drive

Driving Analog-to-Digital Converters (ADCs)

The OPA2348 op amps are optimized for driving medium-speed sampling ADCs. The OPA2348 op amps buffer the ADC input capacitance and resulting charge injection while providing signal gain.

Figure 7 shows the OPA2348 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, micropower sampling converter in the MSOP-8 package. When used with the low-power miniature packages of the OPA348, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide for anti-aliasing filter and charge injection current.

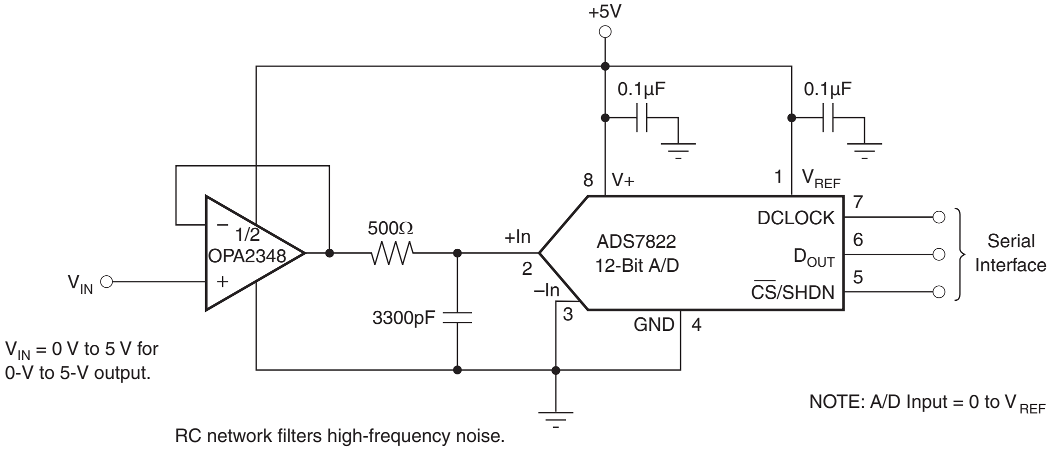
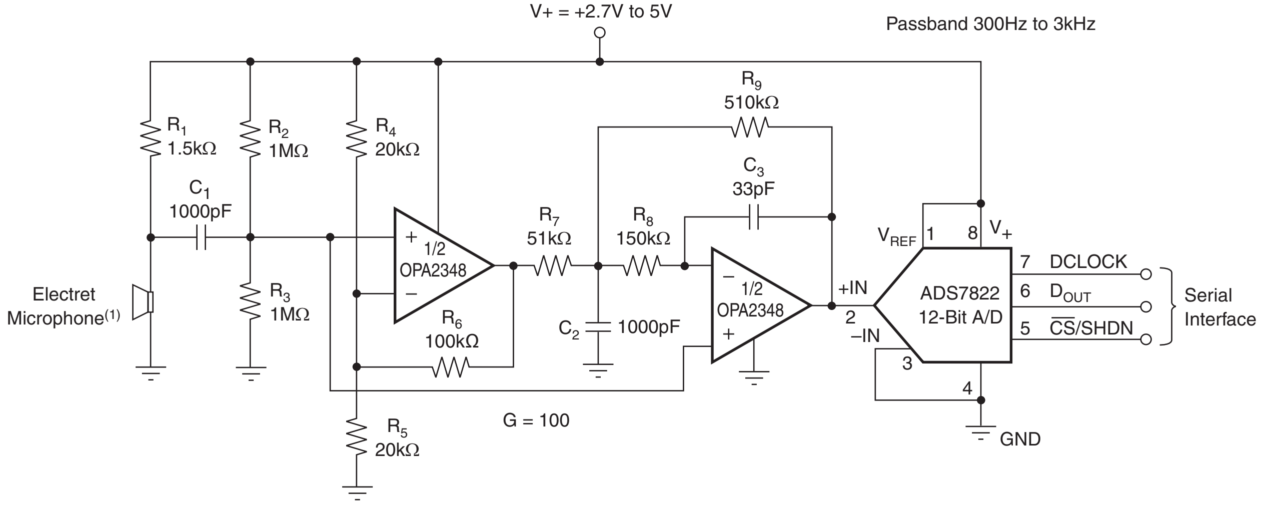


Figure 7. Noninverting Configuration Driving ADS7822

The OPA2348 can also be used in noninverting configuration driving ADS7822 in limited low-power applications. In this configuration, an RC network at the ADC input can be used to provide for antialiasing filter and charge injection current. See Figure 7 for the OPA2348 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit operates with V_S = 2.7 V to 5 V with less than 250-μA typical quiescent current.



(1) Electret microphone powered by R_1.

Figure 8. Speech Bandpass Filtered Data Acquisition System

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA2348CKGD4	ACTIVE	XCEPT	KGD	0	1	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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