

OP281/OP481—SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ $V_S = 3.0\text{ V}$, $V_{CM} = 1.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted. *)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	Note 1 $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			1.5 2.5	mV mV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		3	10	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1	7	nA
Input Voltage Range			0		2	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	65	95		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 1\text{ M}\Omega$, $V_O = 0.3\text{ V to } 2.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	5 2	13		V/mV V/mV
Offset Voltage Drift	$\Delta V_{OS}/DT$			10		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/DT$			20		$\text{pA}/^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/DT$			2		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to GND, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	2.925	2.96		V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to V+, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		25	75	mV
Short Circuit Limit	I_{SC}			± 1.1		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 12\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	76	95		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		3	4 5	μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$, $C_L = 50\text{ pF}$		25		V/ms
Turn On Time		$A_V = 1$, $V_O = 1$		40		μs
Turn On Time		$A_V = 20$, $V_O = 1$		50		μs
Saturation Recovery Time				65		μs
Gain Bandwidth Product	GBP			95		kHz
Phase Margin	ϕ_o			70		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		75		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			<1		$\text{pA}/\sqrt{\text{Hz}}$

* V_{OS} is tested under a no load condition.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ $V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.*)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	Note 1 $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1	1.5	mV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		3	10	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1	7	nA
Input Voltage Range			0		4	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }4.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	65	90		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 1\text{ M}\Omega$, $V_O = 0.5\text{ V to }4.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	5	15		V/mV
Offset Voltage Drift	$\Delta V_{OS}/DT$	$-40^\circ\text{C to }+85^\circ\text{C}$		10		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/DT$			20		$\text{pA}/^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/DT$			2		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to GND, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	4.925	4.96		V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to V+, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		25	75	mV
Short Circuit Limit	I_{SC}			± 3.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }12\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	76	95		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		3.2	4	μA
					5	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$, $C_L = 50\text{ pF}$		27		V/ms
Saturation Recovery Time				120		μs
Gain Bandwidth Product	GBP			100		kHz
Phase Margin	ϕ_o			74		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		75		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			<1		$\text{pA}/\sqrt{\text{Hz}}$

* V_{OS} is tested under a no load condition.

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OP281/OP481

ELECTRICAL SPECIFICATIONS (@ $V_S = \pm 5.0\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. *)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	Note 1 $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1	1.5	mV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		3	10	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1	7	nA
Input Voltage Range			-5		+4	V
Common-Mode Rejection	CMRR	$V_{CM} = -5.0\text{ V to }+4.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	65	95		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 1\text{ M}\Omega$, $V_O = \pm 4.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	5	13		V/mV
Offset Voltage Drift	$\Delta V_{OS}/DT$	$-40^\circ\text{C to }+85^\circ\text{C}$		10		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/DT$			20		$\text{pA}/^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/DT$			2		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L = 100\text{ k}\Omega$ to GND, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	± 4.925	± 4.98		V
Short Circuit Limit	I_{SC}			12		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.35\text{ V to } \pm 6\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	76	95		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		3.3	5	μA
					6	μA
DYNAMIC PERFORMANCE						
Slew Rate	$\pm SR$	$R_L = 100\text{ k}\Omega$, $C_L = 50\text{ pF}$		28		V/ms
Gain Bandwidth Product	GBP			105		kHz
Phase Margin	ϕ_o			75		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		85		$\text{nV}/\sqrt{\text{Hz}}$
Voltage Noise Density	e_n	$f = 10\text{ kHz}$		75		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			<1		$\text{pA}/\sqrt{\text{Hz}}$

* V_{OS} is tested under a no load condition.

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	16 V
Input Voltage	GND to $V_S + 10$ V
Differential Input Voltage	± 3.5 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposures to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP281GS	-40°C to $+85^{\circ}\text{C}$	8-Lead SOIC	R-8
OP281GRU	-40°C to $+85^{\circ}\text{C}$	8-Lead TSSOP	RU-8
OP481GS	-40°C to $+85^{\circ}\text{C}$	14-Lead SOIC	R-14
OP481GRU	-40°C to $+85^{\circ}\text{C}$	14-Lead TSSOP	RU-14

Package Type	θ_{JA}^*	θ_{JC}	Unit
8-Lead SOIC (R)(S)	158	43	$^{\circ}\text{C}/\text{W}$
8-Lead TSSOP (RU)	240	43	$^{\circ}\text{C}/\text{W}$
14-Lead SOIC (R)(S)	120	36	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU)	240	43	$^{\circ}\text{C}/\text{W}$

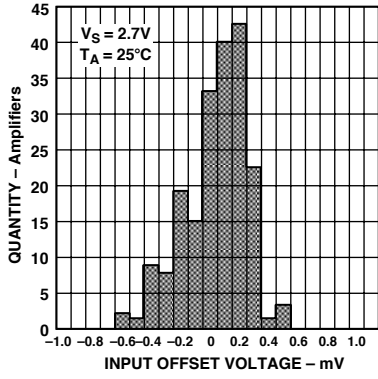
* θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for TSSOP and SOIC packages.

CAUTION

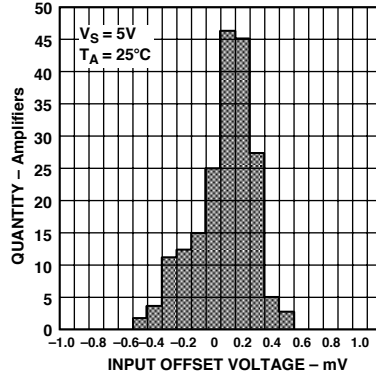
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP281/OP481 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



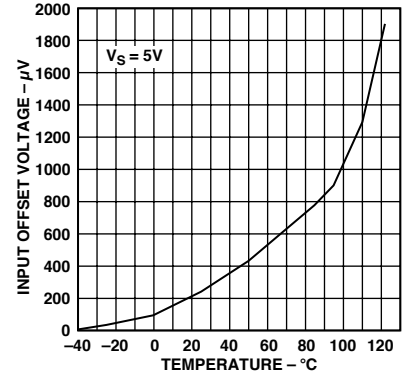
OP281/OP481—Typical Performance Characteristics



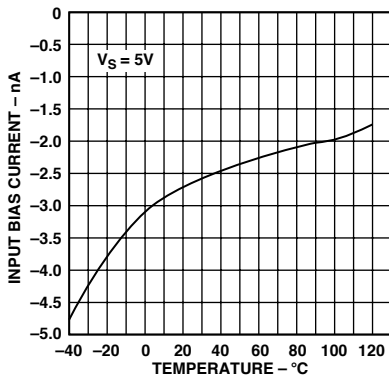
TPC 1. Input Offset Voltage Distribution



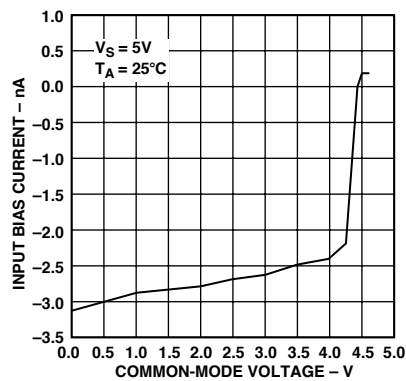
TPC 2. Input Offset Voltage Distribution



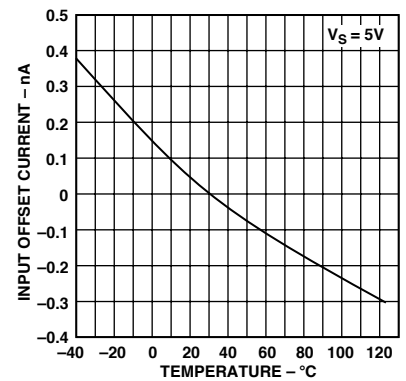
TPC 3. Input Offset Voltage vs. Temperature



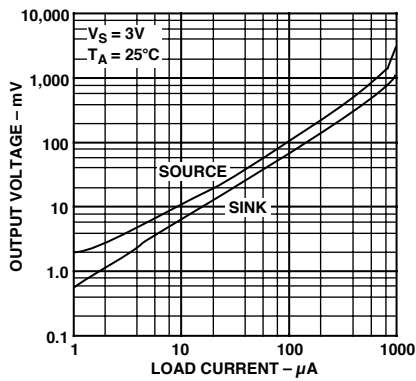
TPC 4. Input Bias Current vs. Temperature



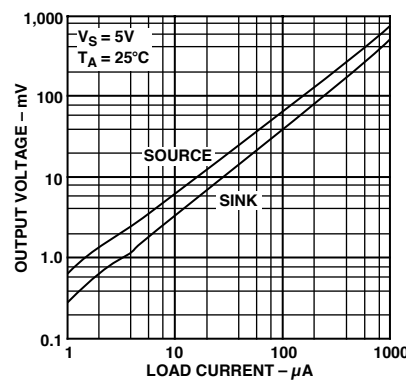
TPC 5. Input Bias Current vs. Common-Mode Voltage



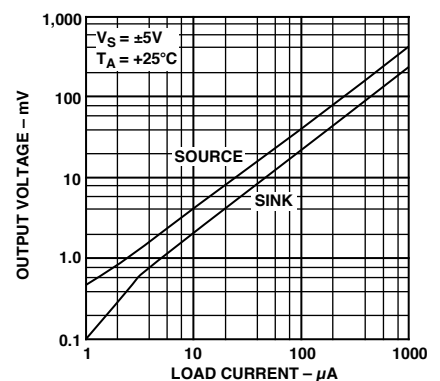
TPC 6. Input Offset Current vs. Temperature



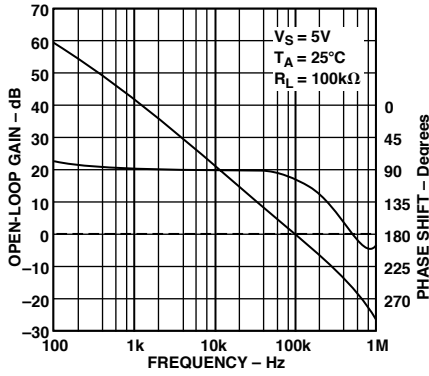
TPC 7. Output Voltage to Supply Rail vs. Load Current



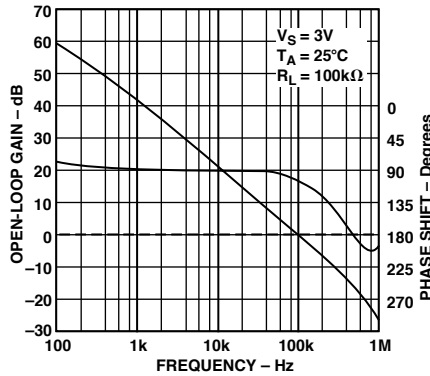
TPC 8. Output Voltage to Supply Rail vs. Load Current



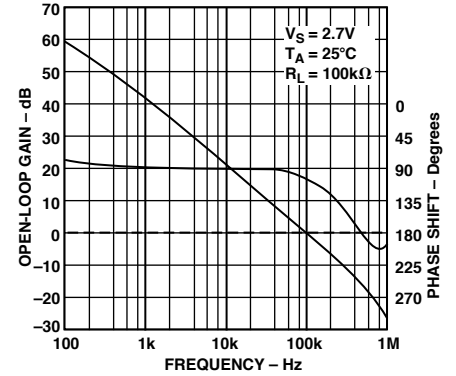
TPC 9. Output Voltage to Supply Rail vs. Load Current



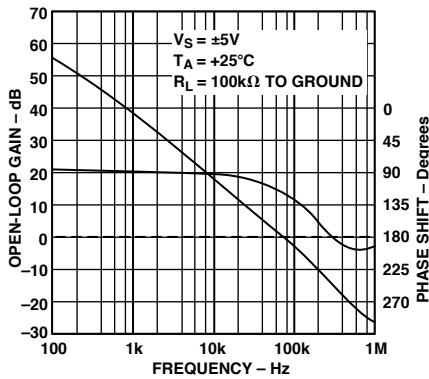
TPC 10. Open-Loop Gain and Phase vs. Frequency



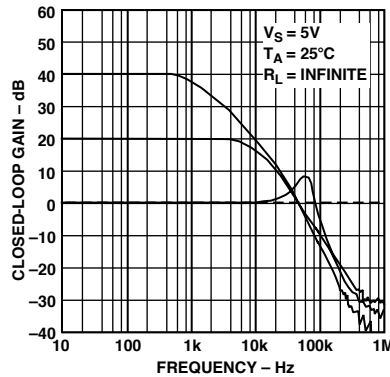
TPC 11. Open-Loop Gain and Phase vs. Frequency



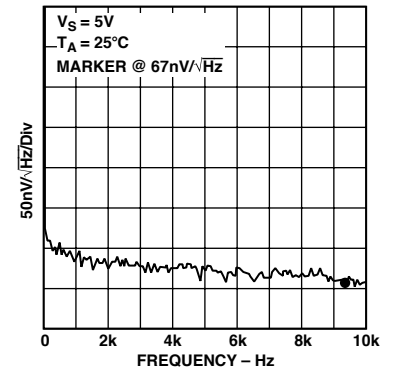
TPC 12. Open-Loop Gain and Phase vs. Frequency



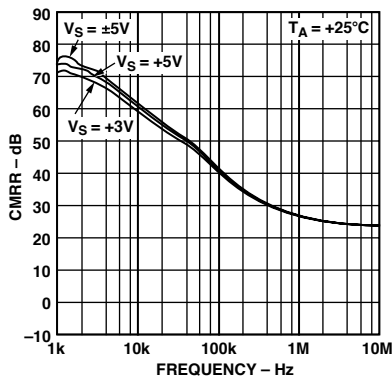
TPC 13. Open-Loop Gain and Phase vs. Frequency



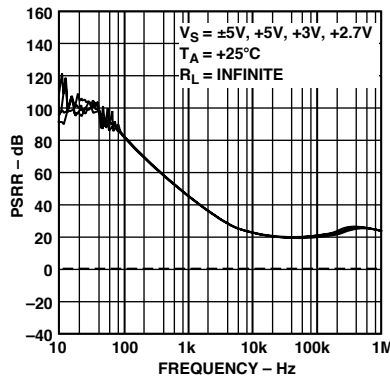
TPC 14. Closed-Loop Gain vs. Frequency



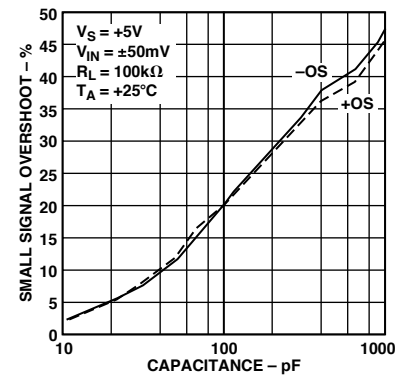
TPC 15. Voltage Noise Density vs. Frequency



TPC 16. CMRR vs. Frequency

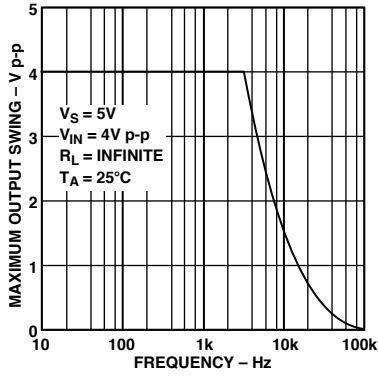


TPC 17. PSRR vs. Frequency

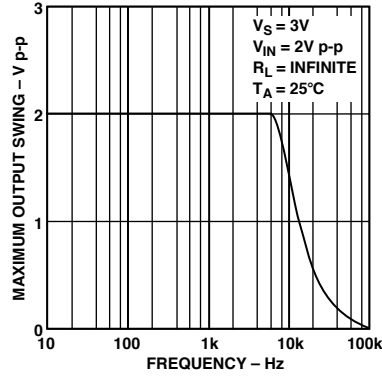


TPC 18. Small Signal Overshoot vs. Load Capacitance

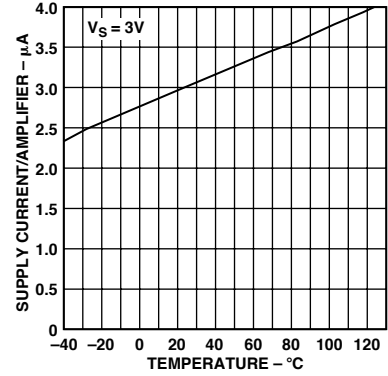
OP281/OP481



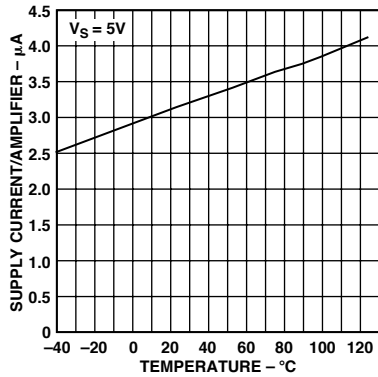
TPC 19. Maximum Output Swing vs. Frequency



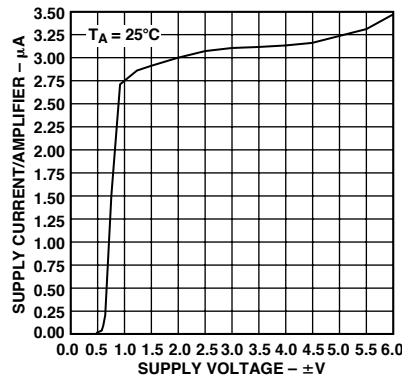
TPC 20. Maximum Output Swing vs. Frequency



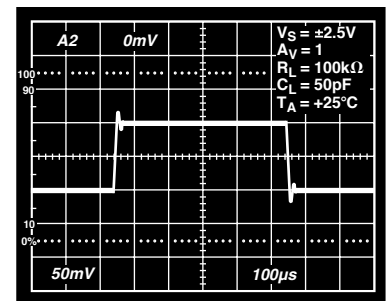
TPC 21. Supply Current/Amplifier vs. Temperature



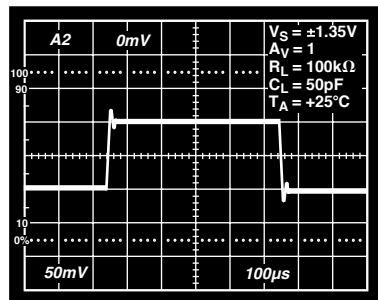
TPC 22. Supply Current/Amplifier vs. Temperature



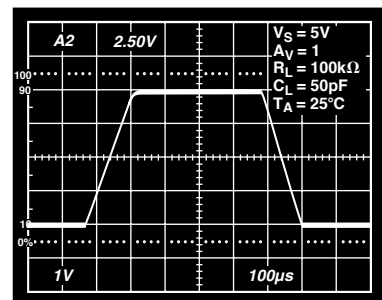
TPC 23. Supply Current/Amplifier vs. Supply Voltage



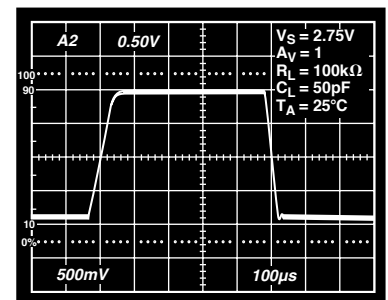
TPC 24. Small Signal Transient Response



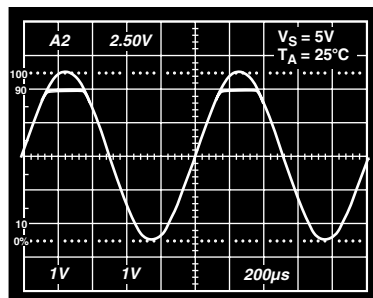
TPC 25. Small Signal Transient Response



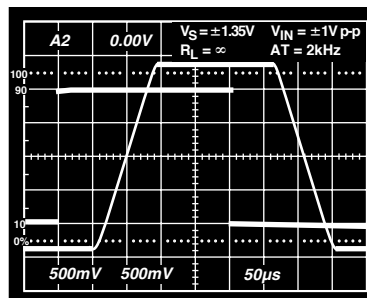
TPC 26. Large Signal Transient Response



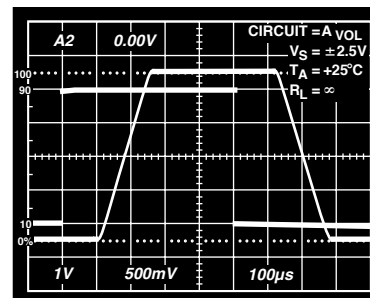
TPC 27. Large Signal Transient Response



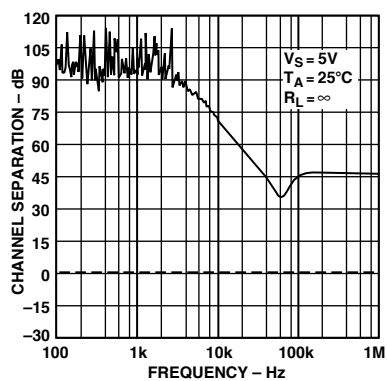
TPC 28. No Phase Reversal



TPC 29. Saturation Recovery Time



TPC 30. Saturation Recovery Time



TPC 31. Channel Separation vs. Frequency

OP281/OP481

APPLICATIONS

Theory of Operation

The OPx81 family of op amps is comprised of extremely low powered, rail-to-rail output amplifiers, requiring less than 4 μA of quiescent current per amplifier. Many other competitors' devices may be advertised as low supply current amplifiers but draw significantly more current as the outputs of these devices are driven to a supply rail. The OPx81's supply current remains under 4 μA even with the output driven to either supply rail. Supply currents should meet the specification as long as the inputs and outputs remain within the range of the power supplies.

Figure 1 shows a simplified schematic of a single channel for the OPx81. A bipolar differential pair is used in the input stage. PNP transistors are used to allow the input stage to remain linear with the common-mode range extending to ground. This is an important consideration for single-supply applications. The bipolar front end also contributes less noise than a MOS front end with only nano-amps of bias currents. The output of the op amp consists of a pair of CMOS transistors in a common source configuration. This setup allows the output of the amplifier to swing to within millivolts of either supply rail. The headroom required by the output stage is limited by the amount of current being driven into the load. The lower the output current, the closer the output can go to either supply rail. TPCs 7, 8, and 9 show the output voltage headroom versus load current. This behavior is typical of rail-to-rail output amplifiers.

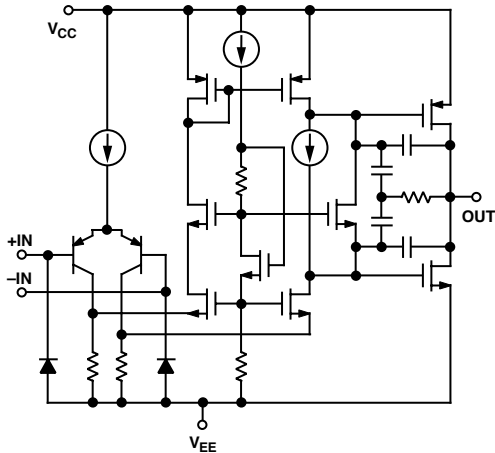


Figure 1. Simplified Schematic of a Single OPx81 Channel

Input Overvoltage Protection

The input stage to the OPx81 family of op amps consists of a PNP differential pair. If the base voltage of either of these input transistors drops to more than 0.6 V below the negative supply, the input ESD protection diodes will become forward biased, and large currents will begin to flow. In addition to possibly damaging the device, this will create a phase reversal effect at the output. To prevent these effects from happening, the input current should be limited to less than 0.5 mA.

This can be done quite easily by placing a resistor in series with the input to the device. The size of the resistor should be proportional to the lowest possible input signal excursion and can be found using the following formula:

$$R = \frac{V_{EE} - V_{IN, MIN}}{0.5 \times 10^{-3}}$$

where:

V_{EE} is the negative power supply for the amplifier.

$V_{IN, MIN}$ is the lowest input voltage excursion expected.

For example, a single channel of the OPx81 is to be used with a single-supply voltage of +5 V where the input signal could possibly go as low as -1 V. Because the amplifier is powered from a single supply, V_{EE} is ground, so the necessary series resistance should be 2 k Ω .

Input Offset Voltage

The OPx81 family of op amps was designed for low offset voltages less than 1 mV.

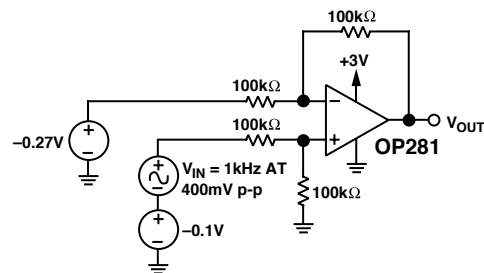


Figure 2. Single OPx81 Channel Configured as a Difference Amplifier Operating at $V_{CM} < 0\text{ V}$

Input Common-Mode Voltage Range

The OPx81 is rated with an input common-mode voltage range from V_{EE} to 1 V under V_{CC} . However, the op amp can still operate even with a common-mode voltage that is slightly less than V_{EE} . Figure 2 shows a single OPx81 channel configured as a difference amplifier with a single-supply voltage of 3 V. Negative dc voltages are applied at both input terminals creating a common-mode voltage that is less than ground. A 400 mV p-p input signal is then applied to the noninverting input. Figure 3 shows the input and output waves. Notice how the output of the amplifier also drops slightly negative without distortion.

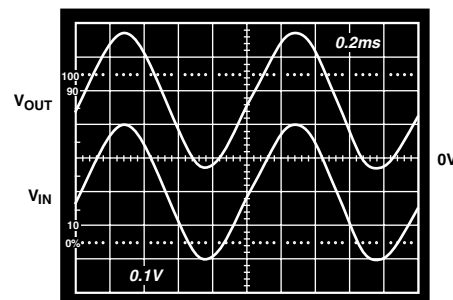


Figure 3. Input and Output Signals with $V_{CM} < 0\text{ V}$

Capacitive Loading

Most low supply current amplifiers have difficulty driving capacitive loads due to the higher currents required from the output stage for such loads. Higher capacitance at the output will increase the amount of overshoot and ringing in the amplifier's step response and could even affect the stability of the device. However, through careful design of the output stage and its high phase margin, the OPx81 family can tolerate some degree of capacitive loading. Figure 4 shows the step response of a single channel with a 10 nF capacitor connected at the output. Notice that the overshoot of the output does not exceed more than 10% with such a load, even with a supply voltage of only 3 V.

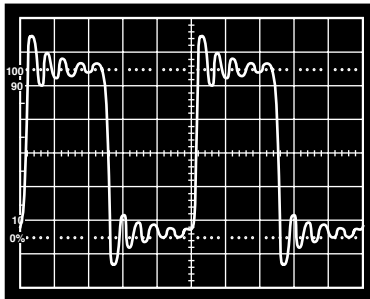


Figure 4. Ringing and Overshoot of the Output of the Amplifier

Micropower Reference Voltage Generator

Many single-supply circuits are configured with the circuit biased to 1/2 of the supply voltage. In these cases, a false ground reference can be created by using a voltage divider buffered by an amplifier. Figure 5 shows the schematic for such a circuit.

The two 1 MΩ resistors generate the reference voltage while drawing only 1.5 μA of current from a 3 V supply. A capacitor connected from the inverting terminal to the output of the op amp provides compensation to allow for a bypass capacitor to be connected at the reference output. This bypass capacitor helps to establish an ac ground for the reference output. The entire reference generator draws less than 5 μA from a 3 V supply source.

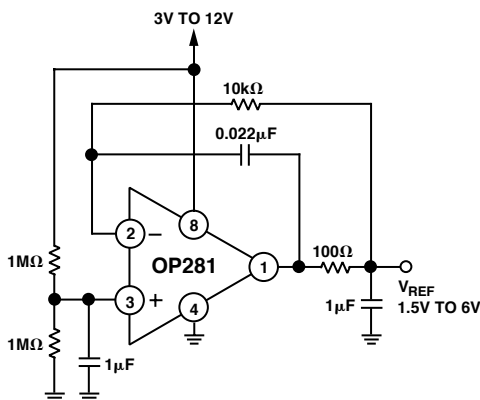


Figure 5. Single Channel Configured as a Micropower Bias Voltage Generator

Window Comparator

The extremely low power supply current demands of the OPx81 family make it ideal for use in long-life battery-powered applications such as a monitoring system. Figure 6 shows a circuit that uses the OP281 as a window comparator.

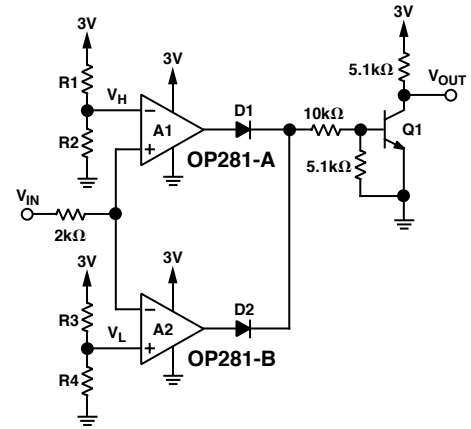


Figure 6. Using the OP281 as a Window Comparator

The threshold limits for the window are set by V_H and V_L , provided that $V_H > V_L$. The output of A1 will stay at the negative rail, in this case ground, as long as the input voltage is less than V_H . Similarly, the output of A2 will stay at ground as long the input voltage is higher than V_L . As long as V_{IN} remains between V_L and V_H , the outputs of both op amps will be 0 V. With no current flowing in either D1 or D2, the base of Q1 will stay at ground, putting the transistor in cutoff and forcing V_{OUT} to the positive supply rail. If the input voltage rises above V_H , the output of A2 stays at ground, but the output of A1 will go to the positive rail, and D1 will conduct current. This creates a base voltage that will turn on Q1 and drive V_{OUT} low. The same condition occurs if V_{IN} falls below V_L with A2's output going high, and D2 conducting current. Therefore, V_{OUT} will be high if the input voltage is between V_L and V_H , and V_{OUT} will be low if the input voltage moves outside of that range.

The R1 and R2 voltage divider sets the upper window voltage, and the R3 and R4 voltage divider sets the lower voltage for the window. For the window comparator to function properly, V_H must be a greater voltage than V_L .

$$V_H = \frac{R2}{R1 + R2}$$

$$V_L = \frac{R4}{R3 + R4}$$

The 2 kΩ resistor connects the input voltage to the input terminals to the op amps. This protects the OP281 from possible excess current flowing into the input stages of the devices. D1 and D2 are small-signal switching diodes (1N4446 or equivalent), and Q1 is a 2N2222 or equivalent NPN transistor.

