

## OP-07 Low Offset, Low Drift Operational Amplifier

### General Description

The OP-07 has very low input offset voltage (25  $\mu\text{V}$  max. for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current ( $\pm 2$  nA for OP-07A) and high open-loop gain (300 V/mV for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of  $\pm 13\text{V}$  minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variation in temperature is excellent.

The OP-07 is available in TO-99 metal can, ceramic or molded DIP.

For improved specifications, see the LM607.

### Features

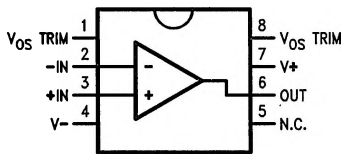
- Low  $V_{OS}$  25  $\mu\text{V}$  Max
- Low  $V_{OS}$  Drift 0.6  $\mu\text{V}/^\circ\text{C}$  Max
- Ultra-Stable vs Time 1.0  $\mu\text{V}/\text{Month}$  Max
- Low Noise 0.6  $\mu\text{Vp-p}$  Max
- Wide Input Voltage Range  $\pm 14\text{V}$
- Wide Supply Voltage Range  $\pm 3\text{V}$  to  $\pm 18\text{V}$
- Fits 725/108A/308A, 741, AD510 Sockets
- Replaces the  $\mu\text{A}714$

### Applications

- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Precision Reference Buffer
- Analog Computing Functions

### Connection Diagrams

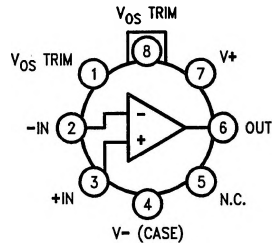
Dual-In-Line Package



TL/H/10550-1

See NS Package Number J08A or N08E

Metal Can Package



TL/H/10550-2

See NS Package Number H08C

### Ordering Information

$T_A = 25^\circ\text{C}$ $V_{OS\text{Max}}$ ( $\mu\text{V}$ )	H08C TO-99	Package J08A CERDIP	N08E Plastic	Operating Temperature Range
25	OP-07AJ*	OP-07AZ*		MIL
75	OP-07EJ	OP-07EZ	OP-07EP	COM
75	OP-07J*	OP-07Z*		MIL
150	OP-07CJ	OP-07CZ	OP-07CP	COM
150	OP-07DJ		OP-07DP	COM

\*For devices processed in total compliance to military specifications refer to RETSOP07X for OP-07.

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 5)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 6)	±22V
Output Short-Circuit Duration	Continuous

### Storage Temperature Range

J and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Lead Temperature (Soldering, 60 sec.)	260°C
Junction Temperature	-65°C to +150°C

## Operating Temperature Range

OP-07A, OP-07,	-55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C

## Electrical Characteristics

Unless otherwise specified,  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ . **Boldface** type refers to limits over  $-55^\circ C \leq T_A \leq +125^\circ C$

Symbol	Parameter	Conditions	OP-07A			OP-07			Units
			Min	Typ	Max	Min	Typ	Max	
$V_{OS}$	Input Offset Voltage	(Note 1) (Note 1)		10 <b>25</b>	25 <b>60</b>		30 <b>60</b>	75 <b>200</b>	$\mu V$
$\Delta V_{OS}/t$	Long-Term Input Offset Voltage Stability	(Note 2)		0.2	1.0		0.2	1.0	$\mu V/Mo$
$I_{OS}$	Input Offset Current			0.3 <b>0.8</b>	2.0 <b>4</b>		0.4 <b>1.2</b>	2.8 <b>5.6</b>	nA
$I_B$	Input Bias Current			$\pm 0.7$ $\pm 1$	$\pm 2.0$ $\pm 4$		$\pm 1.0$ $\pm 2$	$\pm 3.0$ $\pm 6$	nA
$e_{np-p}$	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.35	0.6	$\mu V_{p-p}$
$e_n$	Input Noise Voltage Density	$f_O = 10$ Hz (Note 3) $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
$i_{np-p}$	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		14	30	$pA_{p-p}$
$i_n$	Input Noise Current Density	$f_O = 10$ Hz (Note 3) $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
$R_{IN}$	Input Resistance Differential-Mode	(Note 4)	30	80		20	60		$M\Omega$
$R_{INCM}$	Input Resistance Common-Mode			200			200		$G\Omega$
IVR	Input Voltage Range		$\pm 13.0$ $\pm 13.0$	$\pm 14.0$ $\pm 13.5$		$\pm 13.0$ $\pm 13.0$	$\pm 14.0$ $\pm 13.5$		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	110 <b>106</b>	126 <b>123</b>		110 <b>106</b>	126 <b>123</b>		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		4 <b>5</b>	10 <b>20</b>		4 <b>5</b>	10 <b>20</b>	$\mu V/V$
$A_{VO}$	Large-Signal Voltage Gain	$R_L \geq 2 k\Omega$ , $V_O = \pm 10V$ $R_L \geq 2 k\Omega$ , $V_O = \pm 10V$ $R_L \geq 500\Omega$ , $V_O = \pm 0.5V$ , $V_S = \pm 3V$ (Note 4)	300 <b>200</b> 150	500 <b>400</b> 400		200 <b>150</b> 150	500 <b>400</b> 400		V/mV
$V_O$	Output Voltage Swing	$R_L \geq 10 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 1 k\Omega$	$\pm 12.5$ $\pm 12.0$ $\pm 12.0$ $\pm 10.5$	$\pm 13.0$ $\pm 12.8$ $\pm 12.6$ $\pm 12.0$		$\pm 12.5$ $\pm 12.0$ $\pm 12.0$ $\pm 10.5$	$\pm 13.0$ $\pm 12.8$ $\pm 12.6$ $\pm 12.0$		V

## Electrical Characteristics (Continued)

Unless otherwise specified,  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ . **Boldface** type refers to limits over  $-55^\circ C \leq T_A \leq +125^\circ C$

Symbol	Parameter	Conditions	OP-07A			OP-07			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$R_L \geq 2\text{ k}\Omega$ (Note 3)	0.1	0.3		0.1	0.3		V/ $\mu$ s
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		0.4	0.6		MHz
$R_O$	Open-Loop Output Resistance	$V_O = 0, I_O = 0$		60			60		$\Omega$
$P_d$	Power Consumption	$V_S = \pm 15V$ , No Load $V_S = \pm 3V$ , No Load		75 4	120 6		75 4	120 6	mW
	Offset Adj. Range	$R_P = 20\text{ k}\Omega$		$\pm 4$			$\pm 4$		mV
$TCV_{OS}$	Average Input Offset Voltage Drift Without External Trim	(Note 3)		<b>0.2</b>	<b>0.6</b>		<b>0.3</b>	<b>1.3</b>	$\mu V/^\circ C$
$TCV_{OSn}$	With External Trim	$R_P = 20\text{ k}\Omega$ (Note 4)		<b>0.2</b>	<b>0.6</b>		<b>0.3</b>	<b>1.3</b>	
$TCI_{OS}$	Average Input Offset Current Drift	(Note 3)		<b>5</b>	<b>25</b>		<b>8</b>	<b>50</b>	$\text{pA}/^\circ C$
$TCI_B$	Average Input Bias Drift	(Note 3)		<b>8</b>	<b>25</b>		<b>13</b>	<b>50</b>	$\text{pA}/^\circ C$

**Note 1:** OP-07A grade  $V_{OS}$  is measured approximately one minute after application of power. For all other grades  $V_{OS}$  is measured approximately 0.5 second after application of power.

**Note 2:** Long-Term Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically 2.5  $\mu V$ . Parameter is sample tested.

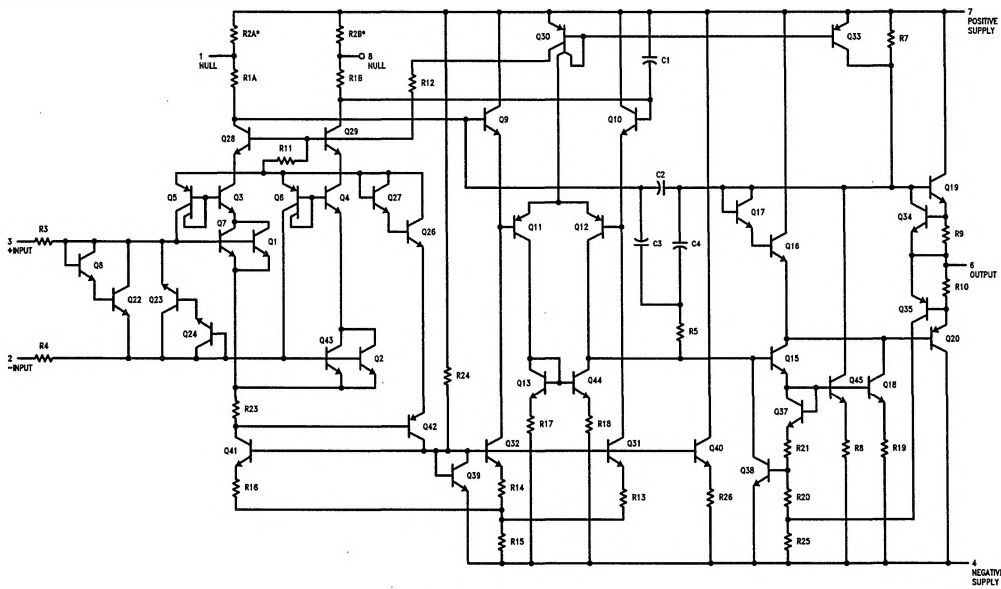
**Note 3:** Sample tested.

**Note 4:** Guaranteed by design.

**Note 5:** The typical  $\theta_{JA}$  of the H08 (TO-99) package is 155 $^\circ C/W$ , the J08 (CERDIP) package is 92 $^\circ C/W$  and the N08 (Molded DIP) is 100 $^\circ C/W$ . The typical  $\theta_{JC}$  of the H08 package is 17.5 $^\circ C/W$ . All numbers apply for packages soldered directly into an etched circuit board.

**Note 6:** For supply voltages of less than  $\pm 22V$ , the maximum input voltage is 0.5V beyond either supply.

## Simplified Schematic



TL/H/10550-3

\*R2A and R2B are electronically trimmed on chip at the factory for minimum offset voltage.

## Electrical Characteristics

Unless otherwise specified,  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ . **Boldface** type refers to limits over  $0^\circ C \leq T_A \leq 70^\circ C$

Symbol	Parameter	Conditions	OP-07E			OP-07C			Units
			Min	Typ	Max	Min	Typ	Max	
$V_{OS}$	Input Offset Voltage	(Note 1)		30 <b>45</b>	75 <b>130</b>		60 <b>85</b>	150 <b>250</b>	$\mu V$
$V_{OS/t}$	Long-Term $V_{OS}$ Stability	(Note 2)		0.3	1.5		0.4	2.0	$\mu V/Mo$
$I_{OS}$	Input Offset Current			0.5 <b>0.9</b>	3.8 <b>5.3</b>		0.8 <b>1.6</b>	6.0 <b>8.0</b>	nA
$I_B$	Input Bias Current			$\pm 1.2$ <b><math>\pm 1.5</math></b>	$\pm 4.0$ <b><math>\pm 5.5</math></b>		$\pm 1.8$ <b><math>\pm 2.2</math></b>	$\pm 7.0$ <b><math>\pm 9.0</math></b>	nA
$e_{np-p}$	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.38	0.65	$\mu V_{p-p}$
$e_n$	Input Noise Voltage Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
$i_{np-p}$	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		15	35	$pA_{p-p}$
$i_n$	Input Noise Current Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
$R_{IN}$	Input Resistance Differential-Mode	(Note 4)	15	50		8	33		$M\Omega$
$R_{INCM}$	Input Resistance Common-Mode			160			120		$G\Omega$
IVR	Input Voltage Range		$\pm 13.0$	$\pm 14.0$		$\pm 13$	$\pm 14$		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	106 <b>103</b>	123 <b>123</b>		100 <b>97</b>	120 <b>120</b>		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$ $V_S = \pm 3V$ to $\pm 18V$		5 <b>7</b>	20 <b>32</b>		7 <b>10</b>	32 <b>51</b>	$\mu V/V$
$A_{VO}$	Large Signal Voltage Gain	$R_L \geq 2$ k $\Omega$ , $V_O = \pm 10V$ $R_L \geq 2$ k $\Omega$ $R_L \geq 500\Omega$ , $V_O = \pm 0.5V$ , $V_S = \pm 3V$ (Note 4)	200 <b>180</b> 150	500 <b>450</b> 400		120 <b>100</b> 100	400 <b>400</b> 400		V/mV
$V_O$	Output Voltage Swing	$R_L \geq 10$ k $\Omega$ $R_L \geq 2$ k $\Omega$ $R_L \geq 2$ k $\Omega$ $R_L \geq 1$ k $\Omega$	$\pm 12.5$ $\pm 12.0$ <b><math>\pm 12.0</math></b> $\pm 10.5$	$\pm 13.0$ $\pm 12.8$ <b><math>\pm 12.6</math></b> $\pm 12.0$		$\pm 12.0$ $\pm 11.5$ <b><math>\pm 11.0</math></b>	$\pm 13.0$ $\pm 12.8$ <b><math>\pm 12.6</math></b> $\pm 12.0$		V
SR	Slew Rate	$R_L \geq 2$ k $\Omega$ (Note 3)	0.1	0.3		0.1	0.3		$V/\mu s$
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		0.4	0.6		MHz
$R_O$	Output Resistance	$V_O = 0$ , $I_O = 0$		60			60		$\Omega$
$P_d$	Power Consumption	$V_S = \pm 15V$ , No Load $V_S = \pm 3V$ , No Load		75 4	120 6		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20$ k $\Omega$		$\pm 4$			$\pm 4$		mV
$TCV_{OS}$	Average Input Offset Voltage Drift Without External Trim	(Note 4)		<b>0.3</b>	<b>1.3</b>		<b>0.5</b>	<b>1.8</b>	$\mu V/^\circ C$
$TCV_{OSn}$	With External Trim	$R_P = 20$ k $\Omega$ (Note 4)		<b>0.3</b>	<b>1.3</b>		<b>0.4</b>	<b>1.6</b>	
$TCI_{OS}$	Average Input Offset Current Drift	(Note 3)		<b>8</b>	<b>35</b>		<b>12</b>	<b>50</b>	$pA/^\circ C$
$TCI_B$	Average Input Bias Current Drift	(Note 3)		<b>13</b>	<b>35</b>		<b>18</b>	<b>50</b>	$pA/^\circ C$

## Electrical Characteristics

Unless otherwise specified,  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ . **Boldface** type refers to limits over  $0^\circ C \leq T_A \leq + 70^\circ C$

Symbol	Parameter	Conditions	OP-07D			Units
			Min	Typ	Max	
$V_{OS}$	Input Offset Voltage	(Note 1)		60 <b>85</b>	150 <b>250</b>	$\mu V$
$V_{OS/t}$	Long-Term $V_{OS}$ Stability	(Note 2)		0.5	3.0	$\mu V/Mo$
$I_{OS}$	Input Offset Current			0.8 <b>1.6</b>	6.0 <b>8.0</b>	nA
$I_B$	Input Bias Current			$\pm 2.0$ $\pm 3.0$	$\pm 12.0$ $\pm 14.0$	nA
$e_{np-p}$	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.38	0.65	$\mu Vp-p$
$e_n$	Input Noise Voltage Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		10.5 10.3 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
$i_{np-p}$	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15	35	$pAp-p$
$i_n$	Input Noise Current Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
$R_{IN}$	Input Resistance Differential-Mode	(Note 4)	7	31		$M\Omega$
$R_{INCM}$	Input Resistance Common-Mode			120		$G\Omega$
IVR	Input Voltage Range		$\pm 13$	$\pm 14$		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	94 <b>94</b>	110 <b>106</b>		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		7 <b>10</b>	32 <b>51</b>	$\mu V/V$
$A_{VO}$	Large Signal Voltage Gain	$R_L \leq 2$ k $\Omega$ , $V_O = \pm 10V$ $R_L = 2$ k $\Omega$ , $V_O = \pm 10V$ $R_L \geq 500\Omega$ , $V_O = \pm 0.5V$ , $V_S \pm 3V$ (Note 4)	120 <b>100</b>	400 <b>400</b> 400		V/mV
$V_O$	Output Voltage Swing	$R_L \geq 10$ k $\Omega$ $R_L \geq 2$ k $\Omega$ $R_L \geq 2$ k $\Omega$ $R_L \geq 1$ k $\Omega$	$\pm 12.0$ $\pm 11.5$ $\pm 11.0$	$\pm 13.0$ $\pm 12.8$ $\pm 12.6$ $\pm 12.0$		V
SR	Slew Rate	$R_L \geq 2$ k $\Omega$ (Note 3)	0.1	0.3		$V/\mu s$
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		MHz
RO	Output Resistance	$V_O = 0$ , $I_O = 0$		60		$\Omega$
$P_d$	Power Consumption	$V_S = \pm 15V$ , No Load $V_S = \pm 3V$ , No Load		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20$ k $\Omega$		$\pm 4$		mV
$TCV_{OS}$	Average Input Offset Voltage Drift Without External Trim	(Note 4)		<b>0.7</b>	<b>2.5</b>	$\mu V/^\circ C$
$TCV_{OSn}$	With External Trim	$R_P = 20$ k $\Omega$ (Note 4)		<b>0.7</b>	<b>2.5</b>	$\mu V/^\circ C$
$TCI_{OS}$	Average Input Offset Current Drift	(Note 3)		<b>12</b>	<b>50</b>	$pA/^\circ C$
$TCI_B$	Average Input Bias Current Drift	(Note 3)		<b>18</b>	<b>50</b>	$pA/^\circ C$

**Note 1:** OP-07A grade  $V_{OS}$  is measured approximately one minute after application of power. For all other grades  $V_{OS}$  is measured approximately 0.5 second after application of power.

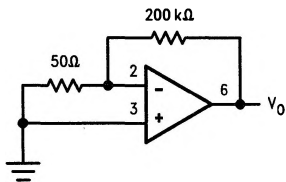
**Note 2:** Long-Term Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically 2.5  $\mu V$ . Parameter is sample tested.

**Note 3:** Sample Tested.

**Note 4:** Guaranteed by design.

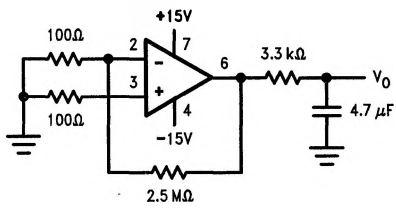
# Test Circuits

### Offset Voltage Test Circuit



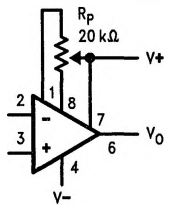
TL/H/10550-4

### Low Frequency Noise Test Circuit



TL/H/10550-5

### Optional Offset Nulling Circuit



TL/H/10550-6