

features

- Multi-Rate Operation from 155 Mbps Up To 2.5 Gbps
- Ultralow Power Consumption
- Input Offset Cancellation
- High Input Dynamic Range
- Output Disable
- Output Polarity Select
- CML Data Outputs

- Single 3.3-V Supply
- Surface Mount Small Footprint 3 mm × 3 mm 16-Pin QFN Package

applications

- SONET/SDH Transmission Systems at OC3, OC12, OC24, OC48
- 1.0625-Gbps and 2.125-Gbps Fibre Channel Receivers
- Gigabit Ethernet Receivers

description

The ONET2511PA is a versatile high-speed limiting amplifier for multiple fiber optic applications with data rates up to 2.5 Gbps.

This device provides a gain of about 50 dB, which ensures a fully differential output swing for input signals as low as 3 mV_{p-p}.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1800 mV_{p-p}.

The ONET2511PA is available in a small footprint 3 mm × 3 mm 16-pin QFN package. The circuit requires a single 3.3-V supply.

This power efficient limiting amplifier is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

ONET2511PA 155-Mbps TO 2.5-Gbps LIMITING AMPLIFIER

SLLS604C – MARCH 2004 – REVISED OCTOBER 2005

block diagram

A simplified block diagram of the ONET2511PA is shown in Figure 1.

This compact, low power 2.5-Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

The limiting amplifier requires a single 3.3-V supply voltage. All circuit parts are described in detail below.

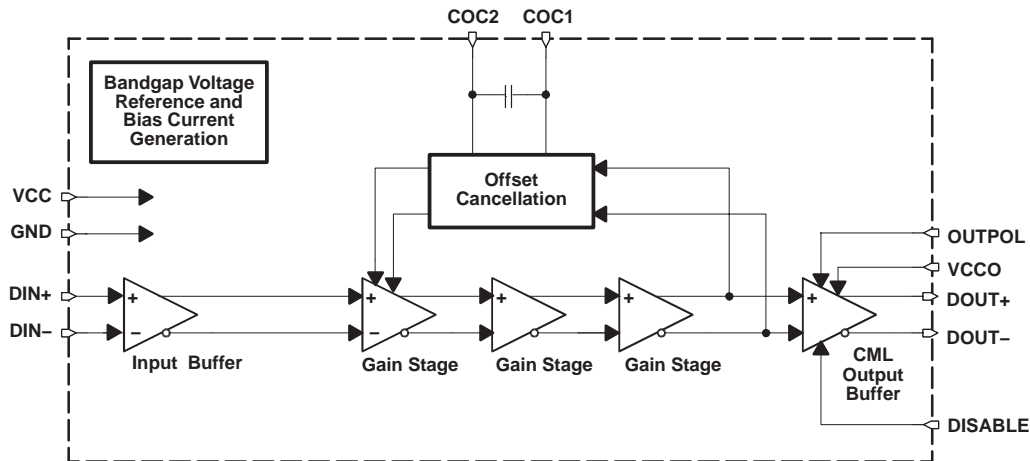


Figure 1. Block Diagram

high-speed data path

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN-. The data path consists of the input stage with $2 \times 50\text{-}\Omega$ on-chip line termination to VCC, three gain stages which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT-, which provide $2 \times 50\text{-}\Omega$ back-termination to VCCO. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input and a disable function, controlled by the signal applied to the DISABLE input pin.

An offset cancellation compensates inevitable internal offset voltages and thus ensures proper operation even for small input data signals.

The low frequency cutoff is as low as 45 kHz with the built-in filter capacitor.

For applications, which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

bandgap voltage and bias generation

The ONET2511PA limiting amplifier is supplied by a single $3.3\text{-V} \pm 10\%$ supply voltage connected to the VCC and VCCO pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuitry generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

package

For the ONET2511PA a small footprint 3 mm × 3 mm 16-pin QFN package is used, with a lead pitch of 0,5 mm. The pinout is shown in Figure 2.

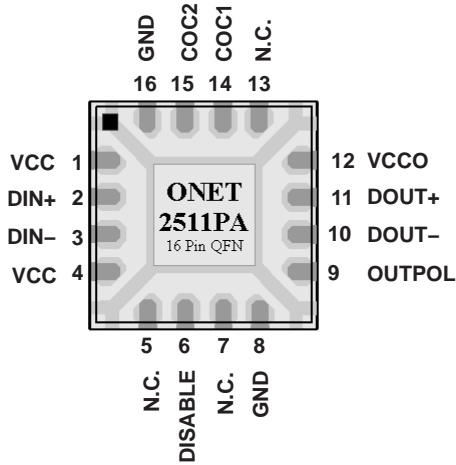


Figure 2. Pinout of ONET2511PA in a 3 mm × 3 mm 16-Pin QFN Package (Top View)

terminal functions

The following table shows a pin description for the ONET2511PA in a 3 mm x 3 mm 16-pin QFN package.

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VCC	1, 4	Supply	3.3-V ±10% supply voltage
DIN+	2	Analog in	Noninverted data input. On-chip 50-Ω terminated to VCC
DIN-	3	Analog in	Inverted data input. On-chip 50-Ω terminated to VCC
N.C.	5, 7, 13		Not connected
DISABLE	6	CMOS in	Disables CML output stage when set to high level
GND	8, 16, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
OUTPUTPOL	9	CMOS in	Output data signal polarity select (internally pulled up): Setting to high level or leaving pin open selects normal polarity. Low level selects inverted polarity.
DOUT-	10	CML out	Inverted data output. On-chip 50-Ω back-terminated to VCCO
DOUT+	11	CML out	Noninverted data output. On-chip 50-Ω back-terminated to VCCO
VCCO	12	Supply	3.3-V ±10% supply voltage for output stage
COC1	14	Analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
COC2	15	Analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

ONET2511PA

155-Mbps TO 2.5-Gbps LIMITING AMPLIFIER

SLLS604C – MARCH 2004 – REVISED OCTOBER 2005

absolute maximum ratings

over operating free-air temperature range unless otherwise noted†

		VALUE	UNIT
V _{CC} , V _{CCO}	Supply voltage, See Note 1	-0.3 to 4	V
V _{DIN+} , V _{DIN-}	Voltage at DIN+, DIN-, See Note 1	0.5 to 4	V
V _{DISABLE} , V _{OUTPOL} , V _{DOUT+} , V _{DOUT-} , V _{COC1} , V _{COC2}	Voltage at TH, DISABLE, OUTPOL, DOUT+, DOUT-, COC1, and COC2, See Note 1	-0.3 to 4	V
V _{COC_DIFF}	Differential voltage between COC1 and COC2	±1	V
V _{DIN_DIFF}	Differential voltage between DIN+ and DIN-	±2.5	V
I _{DIN+} , I _{DIN-} , I _{DOUT+} , I _{DOUT-}	Continuous current at inputs and outputs	-25 to 25	mA
ESD	ESD rating at all pins except V _{CCO}	3	kV (HBM)
	ESD rating at V _{CCO}	1.1	
T _{J(max)}	Maximum junction temperature	125	°C
T _{stg}	Storage temperature range	-65 to 85	°C
T _A	Characterized free-air operating temperature range	-40 to 85	°C
T _L	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V _{CC} , V _{CCO}	3	3.3	3.6	V
Operating free-air temperature, T _A	-40		85	°C

dc electrical characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{CC} , V _{CCO}	Supply voltage	3	3.3	3.6	V
I _{VCC}	Supply current		22	28	mA
V _{OD}	Differential data output voltage swing	DISABLE = high		10	mV _{p-p}
		DISABLE = low		1200	mV _{p-p}
R _{IN} , R _{OUT}	Data input/output resistance	Single ended		50	Ω
V _{IN,MIN}	Data input sensitivity	BER < 10 ⁻¹⁰		3	mV _{p-p}
V _{IN,MAX}	Data input overload			1800	mV _{p-p}
	CMOS input high voltage	2.1			V
	CMOS input low voltage			0.6	V



ac electrical characteristics

over recommended operating conditions (unless otherwise noted), typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency -3-dB bandwidth	$C_{OC} = \text{open}$		45	70	kHz
	$C_{OC} = 100\text{ nF}$		0.8		
Data rate		2.5			Gb/s
VNI Input referred noise				300	μVRMS
DJ Deterministic jitter, See Note 2	K28.5 pattern at 2.5 Gbps		8.5	25	ps _{p-p}
	$2^{23}-1$ PRBS equivalent pattern at 2.5 Gbps		9.3	30	
	$2^{23}-1$ PRBS equivalent pattern at 155 Mbps		25	50	
RJ Random jitter	Input = 5 mV _{pp}		6.5		ps _{RMS}
	Input = 10 mV _{pp}		3		
t_r Output rise time	20% to 80%		60	85	ps
t_f Output fall time	20% to 80%		60	85	ps
PSNR Power supply noise rejection	$f < 2\text{ MHz}$	26			dB
t_{DIS} Disable response time			20		ns

NOTE 2: Deterministic jitter does not include pulse-width distortion due to residual small output offset voltage.

APPLICATION INFORMATION

Figure 3 shows the ONET2511PA connected with an ac-coupled interface to the data signal source as well as to the output load.

The ac-coupling capacitors C_1 through C_4 in the input and output data signal lines are the only required external components. In addition, an optional external filter capacitor (C_{OC}) may be used if a lower cutoff frequency is desired.

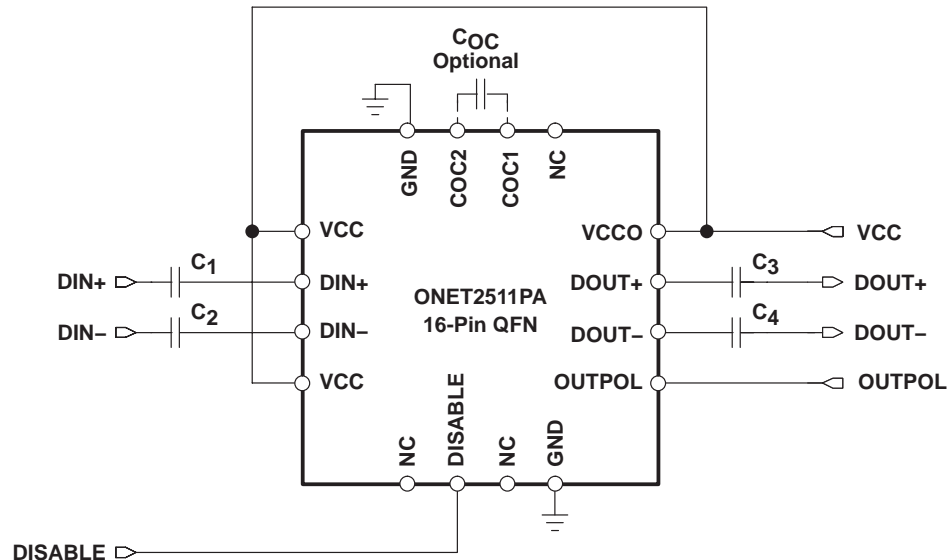


Figure 3. Basic Application Circuit With AC-Coupled I/Os

TYPICAL CHARACTERISTICS

Typical operating condition is at $V_{CC} = V_{CCO} = +3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

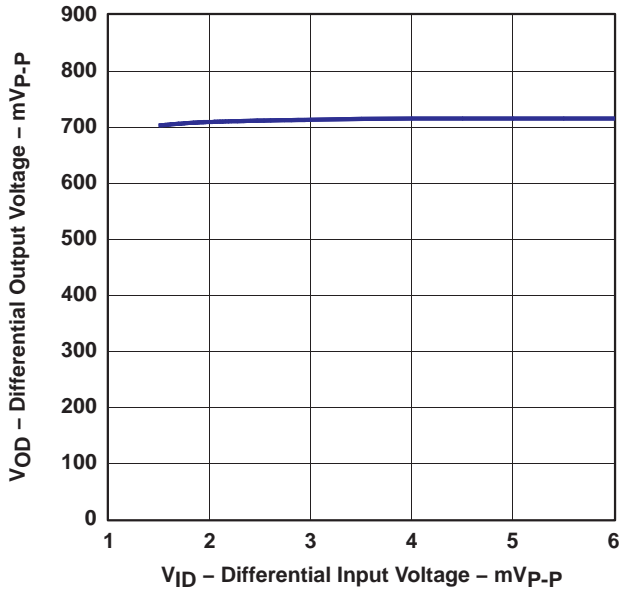


Figure 4

RANDOM JITTER
vs
DIFFERENTIAL INPUT VOLTAGE

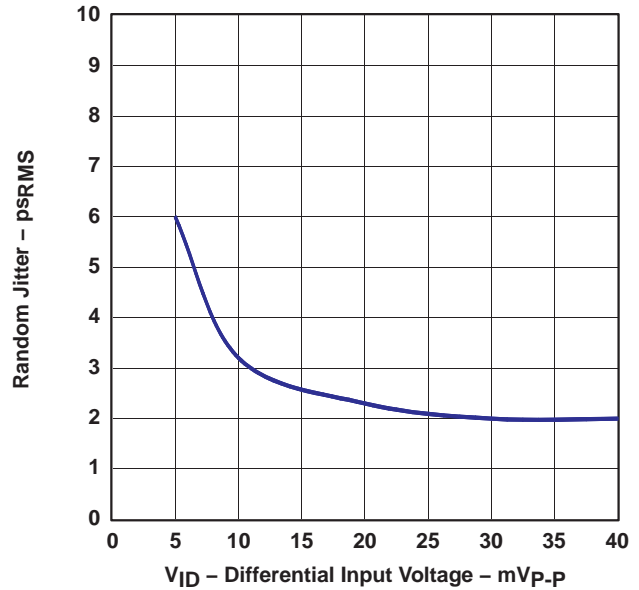


Figure 5

BIT ERROR RATIO
vs
DIFFERENTIAL INPUT VOLTAGE

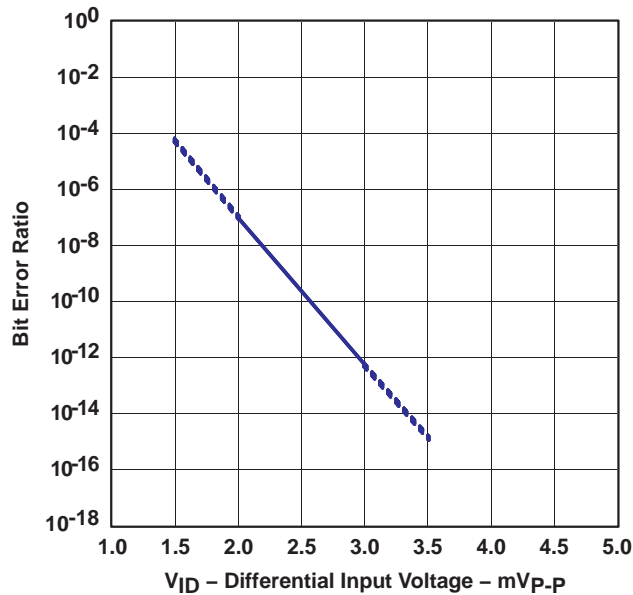
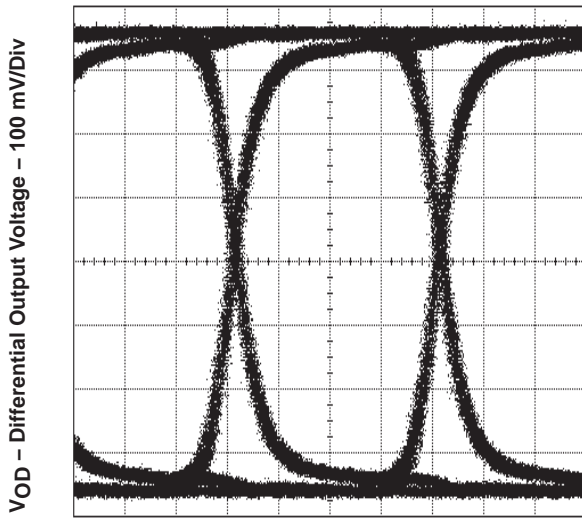


Figure 6

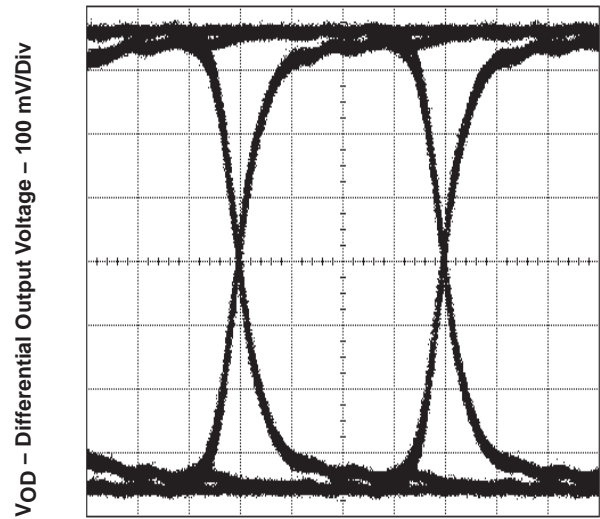
**OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND
 MINIMUM INPUT VOLTAGE (5 mV_{p-p})**



t – Time – 100 ps/Div

Figure 7

**OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND
 MAXIMUM INPUT VOLTAGE (1800 mV_{p-p})**



t – Time – 100 ps/Div

Figure 8

**DIFFERENTIAL INPUT RETURN GAIN
 VS
 FREQUENCY**

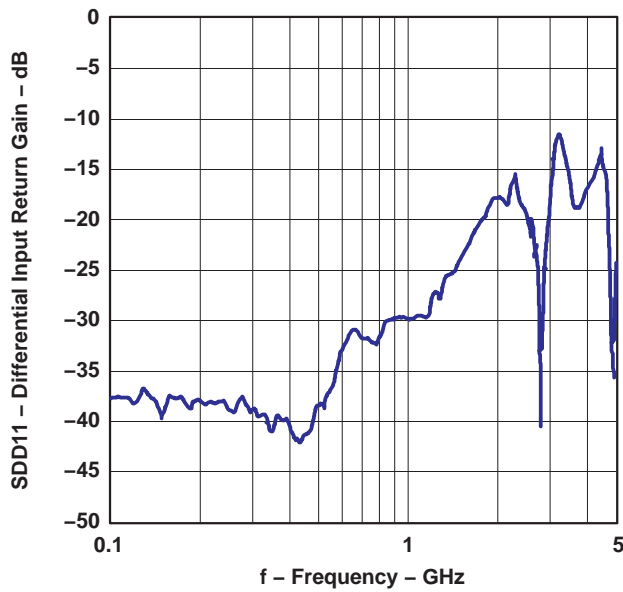


Figure 9

**DIFFERENTIAL OUTPUT RETURN GAIN
 VS
 FREQUENCY**

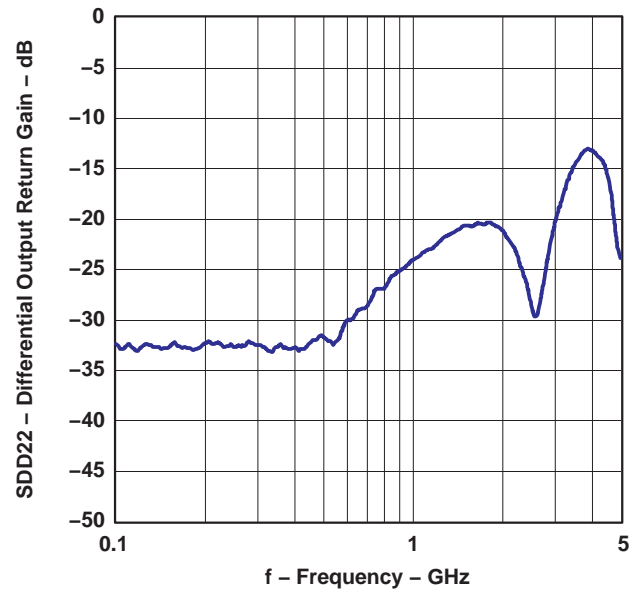


Figure 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ONET2511PARGTR	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85	251P	
ONET2511PARGTRG4	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85		
ONET2511PARGTT	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85	251P	
ONET2511PARGTTG4	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com