



## NMC27C16B 16,384-Bit (2048 x 8) CMOS EPROM

### General Description

The NMC27C16B is a high performance 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

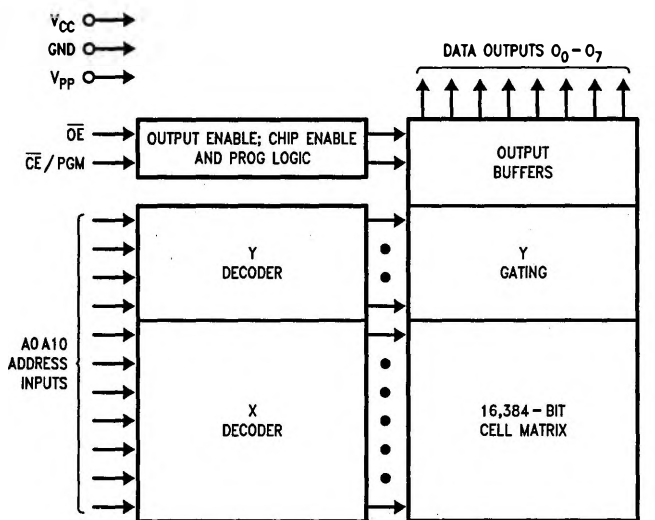
The NMC27C16B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

### Features

- Low CMOS power consumption
  - Active power: 55 mW max
  - Standby power: 0.55 mW max (99% savings)
- Optimal EPROM for total CMOS systems
- Extended temperature range available,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Fast and reliable programming (100  $\mu\text{s}$  for most bytes)
- TTL compatible inputs/outputs
- TRI-STATE<sup>®</sup> output
- Manufacturer's identification code for automatic programming equipment
- High current CMOS level output drivers
- Upgrade for NMOS 2716

### Block Diagram



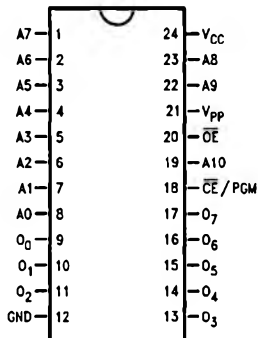
Pin Names

A0-A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
O <sub>0</sub> -O <sub>7</sub>	Outputs
PGM	Program
NC	No Connect

# Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732
V <sub>PP</sub>	V <sub>PP</sub>	V <sub>PP</sub>	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O <sub>0</sub>	O <sub>0</sub>	O <sub>0</sub>	O <sub>0</sub>
O <sub>1</sub>	O <sub>1</sub>	O <sub>1</sub>	O <sub>1</sub>
O <sub>2</sub>	O <sub>2</sub>	O <sub>2</sub>	O <sub>2</sub>
GND	GND	GND	GND

NMC27C16B  
Dual-In-Line Package



27C32 2732	27C64 2764	27C128 27128	27C256 27256
	V <sub>CC</sub> PGM	V <sub>CC</sub> PGM	V <sub>CC</sub>
V <sub>CC</sub>	NC	A13	A14
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
OE/V <sub>PP</sub>	OE	OE	OE
A10	A10	A10	A10
CE	CE	CE	CE
O <sub>7</sub>	O <sub>7</sub>	O <sub>7</sub>	O <sub>7</sub>
O <sub>6</sub>	O <sub>6</sub>	O <sub>6</sub>	O <sub>6</sub>
O <sub>5</sub>	O <sub>5</sub>	O <sub>5</sub>	O <sub>5</sub>
O <sub>4</sub>	O <sub>4</sub>	O <sub>4</sub>	O <sub>4</sub>
O <sub>3</sub>	O <sub>3</sub>	O <sub>3</sub>	O <sub>3</sub>

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## Top View

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16B pins.

Order Number NMC27C16BQ  
See NS Package Number J24AQ

Commercial Temp. Range (0°C to 70°C) V<sub>CC</sub> = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQ150	150
NMC27C16BQ200	200

Extended Temp. Range (-40°C to +85°C) V<sub>CC</sub> = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQE150	150
NMC27C16BQE200	200

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	
Commercial Parts	-10°C to +80°C
Extended Temp. Parts	-40°C to +85°C
Storage Temperature	-65°C to +150°C
V <sub>CC</sub> Supply with	
Respect to Ground	+7.0V to -0.6V
All Input Voltages except A9 with	
Respect to Ground (Note 10)	+6.5V to -0.6V

All Output Voltages with	
Respect to Ground (Note 10)	V <sub>CC</sub> + 1.0V to GND - 0.6V
V <sub>PP</sub> Supply and A9 Voltage	
with Respect to Ground	+14.0V to -0.6V
Power Dissipation	1.0W
Lead Temp. (Soldering, 10 sec.)	300°C

**Operating Conditions** (Note 8)

Temperature Range	
NMC27C16BQ150, 200	0°C to +70°C
NMC27C16BQE150, 200	-40°C to +85°C
V <sub>CC</sub> Power Supply	+5V ±10%

**READ OPERATION****DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ (Note 11)	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IH</sub> = V <sub>CC</sub> or GND		0.1	1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>CC</sub> or GND, $\overline{CE} = V_{IH}$		0.1	1	μA
I <sub>CC1</sub> (Note 3)	V <sub>CC</sub> Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$ , f = 5 MHz Inputs = V <sub>IH</sub> or V <sub>IL</sub> I/O = 0 mA		5	20	mA
I <sub>CC2</sub> (Note 3)	V <sub>CC</sub> Current (Active) CMOS Inputs	$\overline{CE} = \text{GND}$ , f = 5 MHz Inputs = V <sub>CC</sub> or GND, I/O = 0 mA		3	10	mA
I <sub>CCSB1</sub>	V <sub>CC</sub> Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I <sub>CCSB2</sub>	V <sub>CC</sub> Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I <sub>PP</sub>	V <sub>PP</sub> Load Current	V <sub>PP</sub> = 5.5V			10	μA
V <sub>IL</sub>	Input Low Voltage		-0.2		0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> + 1	V
V <sub>OL1</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA			0.45	V
V <sub>OH1</sub>	Output High Voltage	I <sub>OH</sub> = -400 mA	2.4			V
V <sub>OL2</sub>	Output Low Voltage	I <sub>OL</sub> = 10 μA			0.1	V
V <sub>OH2</sub>	Output High Voltage	I <sub>OH</sub> = -10 μA	V <sub>CC</sub> - 0.1			V

**AC Electrical Characteristics**

Symbol	Parameter	Conditions	NMC27C16BQ				Units
			Q150, QE150		Q200, QE200		
			Min	Max	Min	Max	
t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t <sub>CE</sub>	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t <sub>OE</sub>	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60	ns
t <sub>DF</sub>	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t <sub>CF</sub>	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t <sub>OH</sub>	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ , Whichever Occurred First	$\overline{OE} = \overline{CE} = V_{IL}$	0		0		ns

**Capacitance**  $T_A = +25^\circ\text{C}$ ,  $f = 1\text{ MHz}$  (Note 4)

Symbol	Parameter	Conditions	Typ	Max	Units
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	6	12	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	9	12	pF

**AC Test Conditions**Output Load (Note 12) 1 TTL Gate and  $C_L = 100\text{ pF}$ Input Rise and Fall Times  $\leq 5\text{ ns}$ 

Input Pulse Levels 0.45V to 2.4V

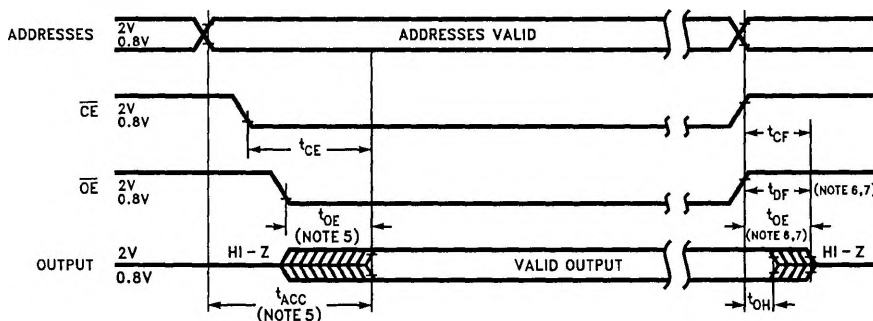
Timing Measurement Reference Level

Inputs

Outputs

0.8V and 2V

0.8V and 2V

**AC Waveforms** (Notes 2 & 9)

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**Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

**Note 3:**  $V_{PP}$  may be connected to  $V_{CC}$  except during programming.  $I_{CC1} \leq$  the sum of the  $I_{CC}$  active and  $I_{PP}$  read currents.

**Note 4:** This parameter is only sampled and is not 100% tested.

**Note 5:**  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .

**Note 6:** The  $t_{DF}$  and  $t_{CF}$  compare level is determined as follows:

High to TRI-STATE, the measured  $V_{OH1}$  (DC) - 0.10V;

Low to TRI-STATE, the measured  $V_{OL1}$  (DC) + 0.10V.

**Note 7:** TRI-STATE may be attained using  $\overline{OE}$  or  $\overline{CE}$ .

**Note 8:** The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1  $\mu\text{F}$  ceramic capacitor be used on every device between  $V_{CC}$  and GND.

**Note 9:** The outputs must be restricted to  $V_{CC} + 1.0\text{V}$  to avoid latch-up and device damage.

**Note 10:** Inputs and outputs can undershoot to  $-2.0\text{V}$  for 20 ns maximum.

**Note 11:** Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltages.

**Note 12:** 1 TTL Gate:  $I_{DL} = 1.6\text{ mA}$ ,  $I_{OH} = 400\text{ }\mu\text{A}$ .

$C_L$ : 100 pF includes fixture capacitance.

## Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{AS}$	Address Setup Time		1			$\mu s$
$t_{OES}$	$\overline{OE}$ Setup Time		1			$\mu s$
$t_{DS}$	Data Setup Time		1			$\mu s$
$t_{VCS}$	$V_{CC}$ Setup Time		1			$\mu s$
$t_{VPS}$	$V_{PP}$ Setup Time		1			$\mu s$
$t_{AH}$	Address Hold Time		0			$\mu s$
$t_{DH}$	Data Hold Time		1			$\mu s$
$t_{DF}$	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		60	ns
$t_{PW}$	Program Pulse Width		95	100	105	$\mu s$
$t_{OE}$	Data Valid from $\overline{OE}$	$\overline{CE}/PGM = V_{IL}$			150	ns
$I_{PP}$	$V_{PP}$ Supply Current During Programming Pulse	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IH}$			30	mA
$I_{CC}$	$V_{CC}$ Supply Current				10	mA
$T_A$	Temperature Ambient		20	25	30	$^{\circ}C$
$V_{CC}$	Power Supply Voltage		6.0	6.25	6.5	V
$V_{PP}$	Programming Supply Voltage		12.5	12.75	13.0	V
$t_{FR}$	Input Rise, Fall Time		5			ns
$V_{IL}$	Input Low Voltage			0.0	0.45	V
$V_{IH}$	Input High Voltage		3.0	4.0		V
$t_{IN}$	Input Timing Reference Voltage		0.8		2.0	V
$t_{OUT}$	Output Timing Reference Voltage		0.8		2.0	V

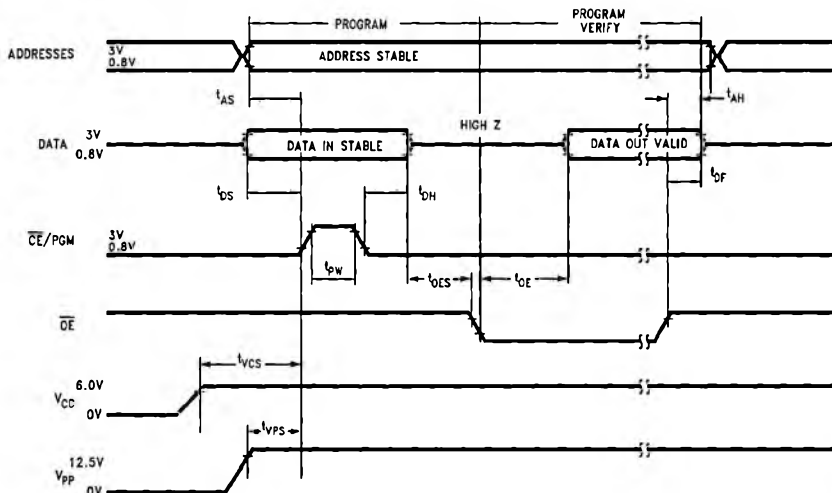
**Note 1:** National's standard product warranty applies only to devices programmed to specifications described herein.

**Note 2:**  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ . The EPROM must not be inserted into or removed from a board with voltage applied to  $V_{PP}$  or  $V_{CC}$ .

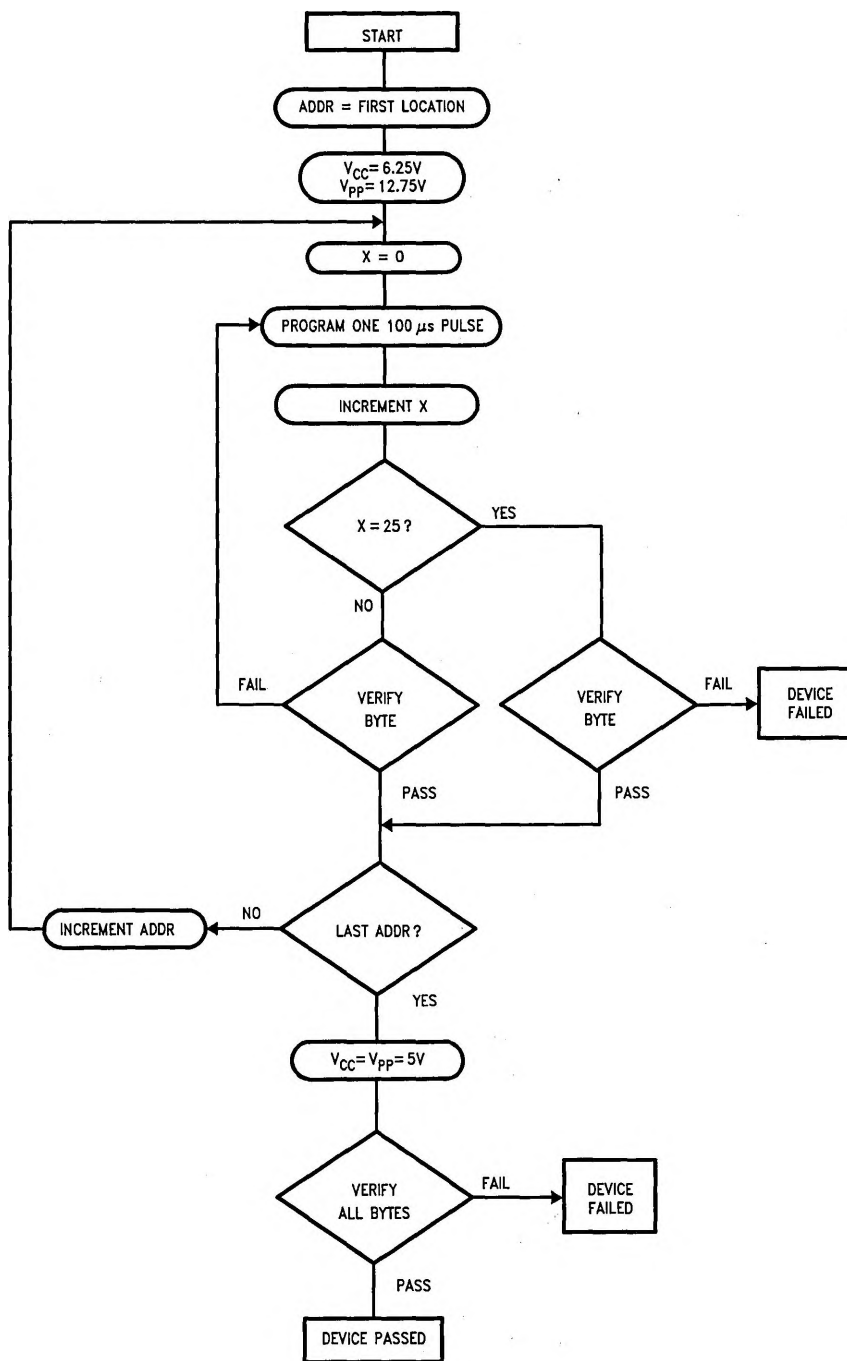
**Note 3:** The maximum absolute allowable voltage which may be applied to the  $V_{PP}$  pin during programming is 14V. Care must be taken when switching the  $V_{PP}$  supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1  $\mu F$  capacitor is required across  $V_{PP}$ ,  $V_{CC}$  to GND to suppress spurious voltage transients which may damage the device.

**Note 4:** Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

## Programming Waveforms



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**Fast Programming Algorithm Flow Chart** (Note 4)**FIGURE 1**

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## Interactive Programming Algorithm Flow Chart (Note 4)

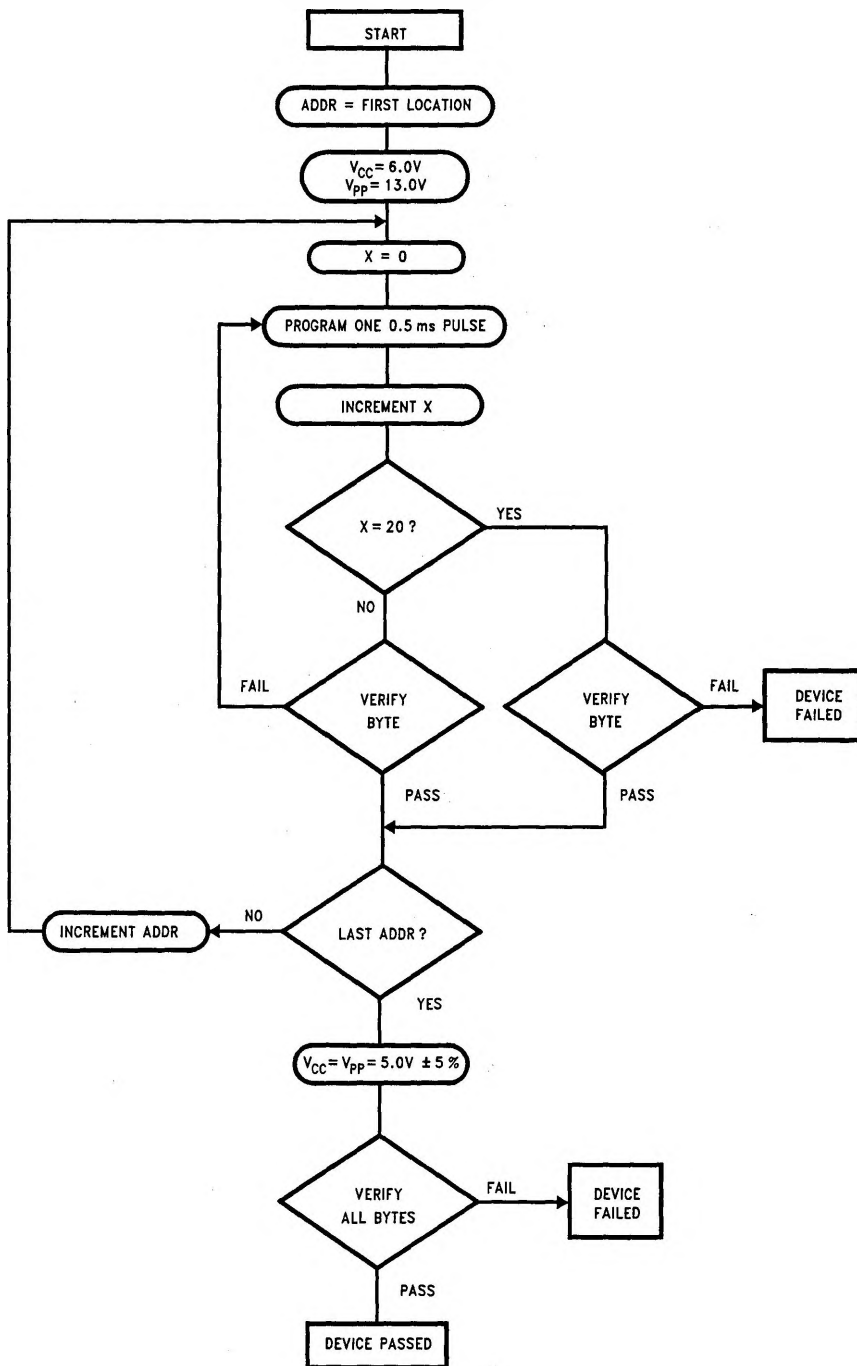


FIGURE 2

TL/D/8180-6

## Functional Description

### DEVICE OPERATION

The six modes of operation of the NMC27C16B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are  $V_{CC}$  and  $V_{pp}$ . The  $V_{pp}$  power supply must be at 12.75V during the three programming modes, and must be at  $V_{CC}$  in the other modes. The  $V_{CC}$  power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

#### Read Mode

The NMC27C16B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been low and addresses have been stable for at least  $t_{ACC} - t_{OE}$ .

The sense amps are clocked for fast access time.  $V_{CC}$  should therefore be maintained at operating voltage during read and verify. If  $V_{CC}$  temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

#### Standby Mode

The NMC27C16B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C16B is placed in the standby mode by applying a CMOS high signal to the  $\overline{CE}$  input. When in standby mode, the outputs are in a high impedance state, independent of the  $\overline{OE}$  input.

#### Output OR-Tying

Because NMC27C16Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

- the lowest possible memory power dissipation, and
- complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that  $\overline{CE}$  (pin 18) be decoded and used as the pri-

mary device selecting function, while  $\overline{OE}$  (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

#### Programming

**CAUTION:** Exceeding 14V on pin 21 ( $V_{pp}$ ) will damage the NMC27C16B.

Initially, and after each erasure, all bits of the NMC27C16B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16B is in the programming mode when the  $V_{pp}$  power supply is at 12.75V and  $\overline{OE}$  is at  $V_{IH}$ . It is required that at least a 0.1  $\mu$ F capacitor be placed across  $V_{pp}$ ,  $V_{CC}$  to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins.

When the address and data are stable, an active high, TTL program pulse is applied to the  $\overline{CE}/\text{PGM}$  input. A program pulse must be applied at each address location to be programmed. The NMC27C16B is programmed with the Fast Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 100  $\mu$ s pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100  $\mu$ s pulse.

**Note:** Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (shown in Figure 2).

The NMC27C16B must not be programmed with a DC signal applied to the  $\overline{CE}/\text{PGM}$  input.

Programming multiple NMC27C16Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16Bs may be connected together when they are programmed with the same data. A high level TTL pulse applied to the  $\overline{CE}/\text{PGM}$  input programs the paralleled NMC27C16Bs.

TABLE I. Mode Selection

Mode	Pins $\overline{CE}/\text{PGM}$ (18)	$\overline{OE}$ (20)	$V_{pp}$ (21)	$V_{CC}$ (24)	Outputs (9-11), (13-17)
Read	$V_{IL}$	$V_{IL}$	$V_{CC}$	5	$D_{OUT}$
Standby	$V_{IH}$	Don't Care	$V_{CC}$	5	Hi-Z
Output Disable	Don't Care	$V_{IH}$	$V_{CC}$	5	Hi-Z
Program	$V_{IH}$	$V_{IH}$	12.75V	6.25	$D_{IN}$
Program Verify	$V_{IL}$	$V_{IL}$	12.75V	6.25	$D_{OUT}$
Program Inhibit	$V_{IL}$	$V_{IH}$	12.75V	6.25	Hi-Z



## Functional Description (Continued)

### Program Inhibit

Programming multiple NMC27C16Bs in parallel with different data is also easily accomplished. Except for  $\overline{CE}/PGM$  all like inputs (including  $\overline{OE}$ ) of the parallel NMC27C16Bs may be common. A TTL high level program pulse applied to an NMC27C16B's  $\overline{CE}/PGM$  input with  $V_{PP}$  at 12.75V will program that NMC27C16B. A TTL low level  $\overline{CE}/PGM$  input inhibits the other NMC27C16Bs from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with  $V_{PP}$  at 12.75V. Except during programming and program verify,  $V_{PP}$  must be at  $V_{CC}$ .

### MANUFACTURER'S IDENTIFICATION CODE

The NMC27C16B has a manufacturer's identification code to aid in programming. The code, shown in Table III, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C16B is, "8F80", where "8F" designates that it is made by National Semiconductor, and "80" designates a 16k part.

The code is accessed by applying  $12.0V \pm 0.5V$  to address pin A9. Addresses A1–A8, A10,  $\overline{CE}$ , and  $\overline{OE}$  are held at  $V_{IL}$ . Address A0 is held at  $V_{IL}$  for the manufacturer's code, and at  $V_{IH}$  for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at  $25^\circ C \pm 5^\circ C$ .

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

### ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms ( $\text{\AA}$ ). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 $\text{\AA}$ –4000 $\text{\AA}$  range. After programming, opaque labels should be placed

over the NMC27C16B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16B is exposure to short wave ultraviolet light which has a wavelength of 2537 $\text{\AA}$ . The integrated dose (i.e., UV intensity  $\times$  exposure time) for erasure should be a minimum of 15 W-sec/cm<sup>2</sup>.

The NMC27C16B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27C16B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

### SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current,  $I_{CC}$ , has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated  $V_{CC}$  transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1  $\mu F$  ceramic capacitor be used on every device between  $V_{CC}$  and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7  $\mu F$  bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27C16B Erasure Time

Light Intensity (Micro-Watts/cm <sup>2</sup> )	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

TABLE III. Manufacturer's Identification Code

Pins	A <sub>0</sub> (8)	O <sub>7</sub> (17)	O <sub>6</sub> (16)	O <sub>5</sub> (15)	O <sub>4</sub> (14)	O <sub>3</sub> (13)	O <sub>2</sub> (11)	O <sub>1</sub> (10)	O <sub>0</sub> (9)	Hex Data
Manufacturer Code	$V_{IL}$	1	0	0	0	1	1	1	1	8F
Device Code	$V_{IH}$	1	0	0	0	0	0	0	0	80