PPRELIMINARY

DOLBY PRO LOGIC SURROUND DECODER

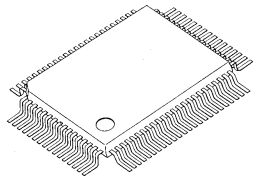
■ GENERAL DESCRIPTION

The **NJW1106** is a surround processor including all of the necessary circuits of Dolby Pro Logic Surround decoder and digital delay.

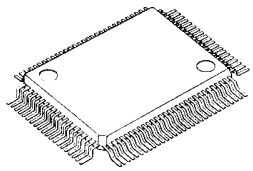
All of internal statuses are controlled by I^2C BUS interface.

In addition to Dolby Pro Logic Surround function, it performs easily other surround function such as Hall, Live, Disco and others.

■ PACKAGE OUTLINE



NJW1106FC2-80



NJW1106FC2

■ FEATURES

- Operating Voltage : V_{CC}=10V(Analog Block), V_{DD}=5V(Digital Block)
- Digital Delay on chip
- I^2C BUS Interface SDA, SCL
- Bi-CMOS Technology
- Package Outline QFP80, QFP100

■ FUNCTION

[Dolby Pro Logic Surround]

- Automatic input balance
- Noise sequencer
- Adaptive matrix
- Center channel control (Wide, Normal, Phantom, Off)
- Modified B-type noise reduction
- 7kHz low-pass filter
- Dolby 3 stereo mode
- Digital time delay (15,20,25,30msec.)

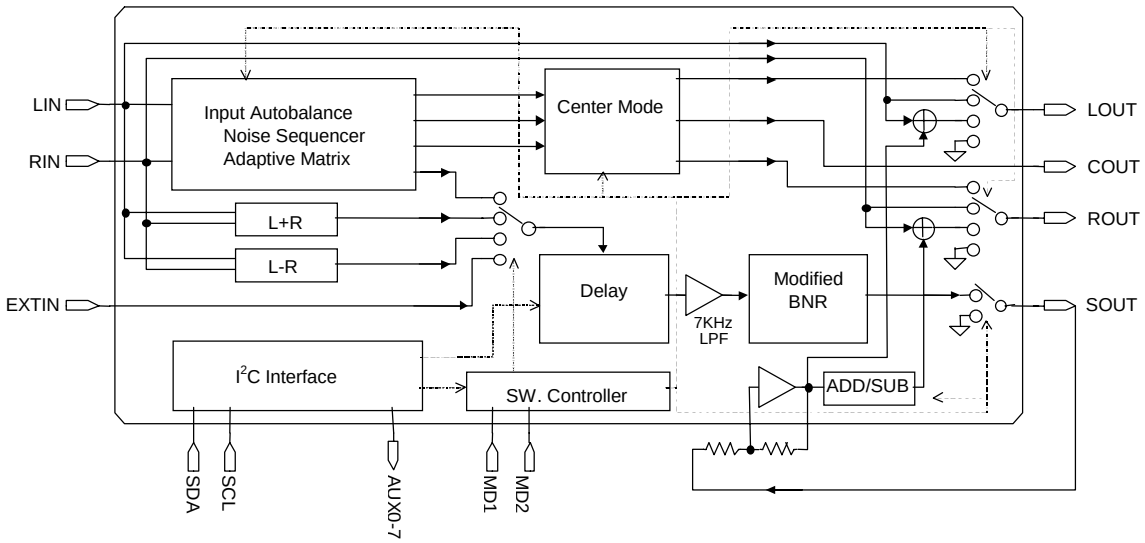
[Other Surround]

- Surround Signal Selector (L+R, L-R, EXTIN)
- Front mixing control
- Digital time delay (15,20,25,30,40,50,60msec.)

[Other Function]

- Digital auxiliary outputs (AUX0-AUX7)

■ SYSTEM BLOCK DIAGRAM



Ver.1.0

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC} V_{DD}	13 6.5	V
Power Dissipation*	P_D	(QFP80) 1.3 (QFP100) 1.3	W
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

*On board

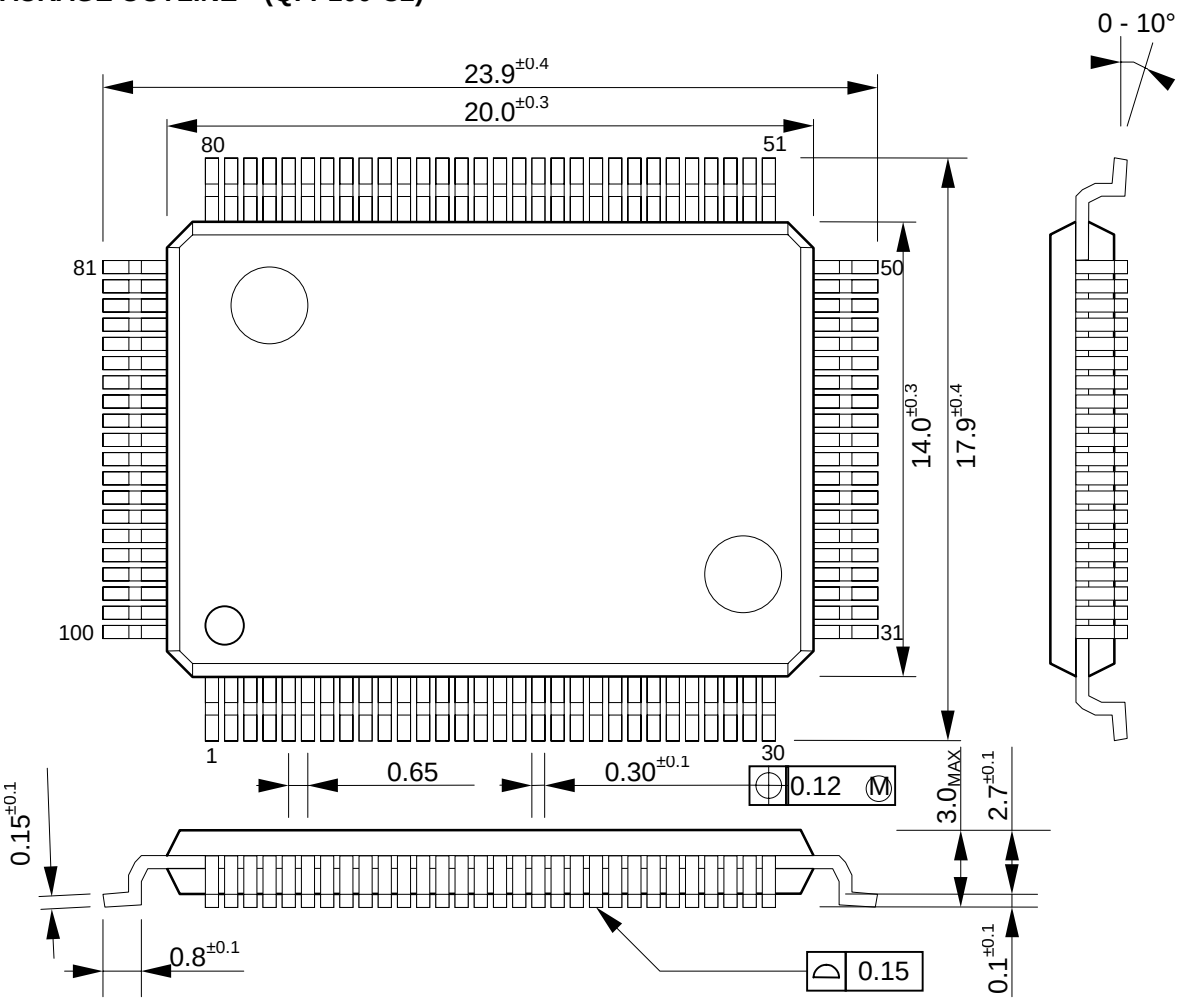
■ ELECTRICAL CHARACTERISTICS (V_{CC}=10V, V_{DD}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
□ OVERALL						
Supply Voltage Range	V_{CC}		9	10	13	V
	V_{DD}		4.5	5	5.5	V
Supply Current	I_{CC}	No Signal	-	37	50	mA
	I_{DD}	No Signal	-	6	10	mA
Reference Voltage	V_{REF}	No Signal	3.6	4.0	4.4	V
Threshold Voltage	V_{thh}	Digital input high level	$0.7V_{DD}$	-	V_{DD}	V
	V_{thl}	Digital input low level	0.0	-	$0.3V_{DD}$	V
□ INPUT AUTO BALANCE						
Capture Range	CPR		-	5	-	
Error Correction	CER		-	4	-	
□ ADAPTIVE MATRIX (0dB=300mVrms, f=1kHz at Cin Cout)						
Output Level Accuracy relative to Cch	ΔVol	L,R,S'ch.out	-0.5	0	0.5	dB
Matrix Rejection relative	MR	L,R,S'ch.out	25	40	-	dB
Headroom	HR-AM	V_{CC}=9V at THD=1%	15	17	-	dB
Total Harmonic Distortion	THD-AM	L,R,C,S'ch.out at 4ch.mode	-	0.05	0.2	%
		L,R,ch.out at 2ch.mode	-	0.002	0.1	%
Signal to Noise Ratio	SNAM	Rg=0,wt:CCIR-ARM at 4ch.mode	75	80	-	dB
		L,R,ch.out at 2ch.mode	93	100	-	dB
□ NOISE SEQUENCER						
Output Noise Level	Vno		-15.0	-12.5	-10.0	dB
Output Noise Level Accuracy relative to Cch	ΔVno	L,R,S'ch.out	-0.5	0.0	0.5	dB
□ MODIFIED B-TYPE NOISE REDUCTION (0dB=300mVrms, f=100Hz at Sin Sout)						
Voltage Gain	GV-NR	Vin=0dBd,f=100Hz	-	9.5	-	dB
Decode Responce1	DEC1	Vin=0dBd,f=1kHz	-1.6	-0.1	1.4	dB
Decode Responce2	DEC2	Vin=-15dBd,f=1.4kHz	-3.0	-1.5	0.0	dB
Decode Responce3	DEC3	Vin=-20dBd,f=1.4kHz	-4.9	-3.4	-1.9	dB
Decode Responce4	DEC4	Vin=-40dBd,f=5kHz	-6.8	-5.3	-3.8	dB
Total Harmonic Distortion	THDNR	Vin=0dBd,f=1kHz	-	0.07	0.3	%
Headroom	HRNR	V_{CC}=9V at THD=1%	15	17	-	dB
Signal to Noise Ratio	SNNR	Rg=0,weightted:CCIR/ARM	73	78	-	dB

■ **ELECTRICAL CHARACTERISTICS (V_{CC}=10V, V_{DD}=5V, Ta=25°C)**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
□ OTHER SURROUND							
Total Harmonic Distortion	THDOS	Vin=0dBd,f=1kHz L+R,L-R output		-	0.05	0.2	dB
Headroom	HROS	V_{CC}=9V at THD=1% L+R,L-R mode		15	17	-	dB
Signal to Noise Ratio	SNOS	Rg=0,weighted:CCIR/ARM L+R,L-R mode		75	80	-	dB
□ DIGITAL TIME DELAY							
Delay Time	Td	f_{OSC}=4MHz		12.4	15.4	18.4	ms
				17.5	20.5	23.5	ms
				22.6	25.6	28.6	ms
				27.7	30.7	33.7	ms
				38.0	41.0	44.0	ms
				48.2	51.2	54.2	ms
				58.4	61.4	64.4	ms
Total Gain	Gv			-3.0	0.0	3.0	dB
Total Harmonic Distortion	THD	Vin=0.3Vrms	Td=15.4ms	-	0.3	0.6	%
		f=1kHz	Td=20.5ms	-	0.3	0.6	%
		30kHz LPF	Td=25.6ms	-	0.4	0.8	%
			Td=30.7ms	-	0.5	1.0	%
			Td=41.0ms	-	0.6	1.2	%
			Td=51.2ms	-	0.7	1.4	%
			Td=61.4ms	-	0.8	1.6	%
Maximum Output Voltage	Vomax	Vin:f=1kHz 30kHz LPF,THD=3%		1.5	1.8	-	Vrms
Output Noise Voltage	No	Rg=600Ω	Td=15.4ms	-	-85	-75	dBV
		Vin=0Vrms	Td=20.5ms	-	-85	-75	dBV
		JIS-A	Td=25.6ms	-	-85	-75	dBV
			Td=30.7ms	-	-80	-70	dBV
			Td=41.0ms	-	-80	-70	dBV
			Td=51.2ms	-	-80	-70	dBV
			Td=61.4ms	-	-75	-65	dBV
□ DIGITAL AUXILIARY OUTPUT							
Low Level Output	VOL	Output Current=-1mA		0.0	-	$0.3V_{DD}$	dB
High Level Output	VOH	Output Current=1mA		$0.7V_{DD}$	-	V_{DD}	dB

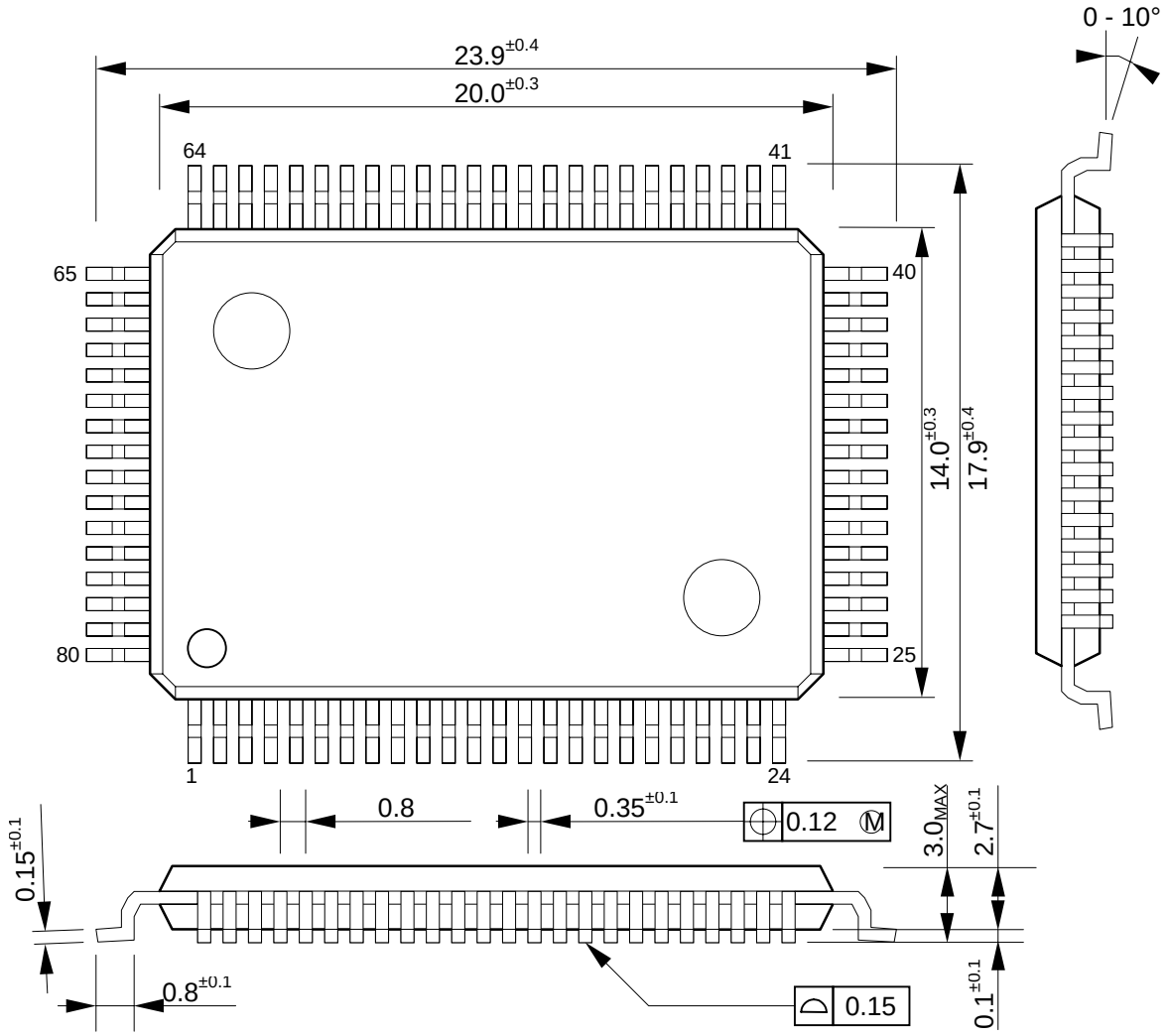
■ **PACKAGE OUTLINE (QFP100-C2)**



■ **PIN CONNECTION**

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	RLC3	26	NC	51	NC	76	DBIN
2	RLC8	27	NC	52	NC	77	DBC1
3	RLC6	28	NC	53	NC	78	DBC2
4	LLI	29	NC	54	NC	79	DBC3
5	LBPF	30	NC	55	NC	80	LOUT
6	RLI	31	VSS	56	NC	81	ROUT
7	RBPF	32	SM0	57	NC	82	COUT
8	LT	33	SM1	58	NC	83	SOUT
9	RT	34	AUX7	59	NC	84	CMC
10	LIN	35	AUX6	60	NC	85	SMRO
11	RIN	36	AUX5	61	NC	86	SMRI
12	HOLDC	37	AUX4	62	VDD	87	EXTIN
13	NGC3	38	AUX3	63	VCC	88	VREF
14	NGC2	39	AUX2	64	SDOUT	89	IREF
15	NGC1	40	AUX1	65	LPF1IN	90	PSC3
16	GND	41	AUX0	66	LPF1OUT	91	PSC6
17	MD1	42	RST	67	OPA1IN	92	PSC2
18	MD2	43	NC	68	OPA1OUT	93	PSC5
19	VSS	44	SDA	69	CC1	94	PSC1
20	NC	45	SCL	70	CC2	95	PSC4
21	NC	46	NC	71	OPA2IN	96	RLC5
22	NC	47	CLK2	72	OPA2OUT	97	RLC2
23	NC	48	CLK1	73	LPF2IN	98	RLC1
24	NC	49	VDD	74	LPF2OUT	99	RLC4
25	NC	50	NC	75	LPFIN	100	RLC7

■ PACKAGE OUTLINE (QFP80-C2)



■ PIN CONNECTION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MD2	21	NC	41	DBC3	61	RLC4
2	MD2	22	VDD	42	LOUT	62	RLC7
3	VSS	23	VCC	43	ROUT	63	RLC3
4	SM0	24	VCC	44	COUT	64	RLC8
5	SM1	25	SDOUT	45	SOUT	65	RLC6
6	AUX7	26	SDOUT	46	CMC	66	LLI
7	AUX6	27	LPF1IN	47	SMRO	67	LBPF
8	AUX5	28	LPF1OUT	48	SMRI	68	RLI
9	AUX4	29	OP1IN	49	EXTIN	69	RBPF
10	AUX3	30	OP1OUT	50	VREF	70	LT
11	AUX2	31	CC1	51	IREF	71	RT
12	AUX1	32	CC2	52	PSC3	72	LIN
13	AUX0	33	OP2IN	53	PSC6	73	RIN
14	RST	34	OP2OUT	54	PSC2	74	HOLDC
15	NC	35	LPF2IN	55	PSC5	75	NGC3
16	SDA	36	LPF2OUT	56	PSC1	76	NGC2
17	SCL	37	LPFIN	57	PSC4	77	NGC1
18	NC	38	DBIN	58	RLC5	78	GND
19	CLK2	39	DBC1	59	RLC2	79	MD1
20	CLK1	40	DBC2	60	RLC1	80	MD1

MEMO