

DUPLEX LCD DRIVER

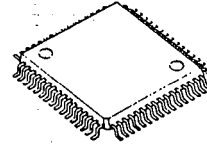
■ GENERAL DESCRIPTION

The NJU6432B is a duplex LCD driver to drive segment type LCD panel.

2-common and 53-segment drivers can drive up to 104 segments.

The NJU6432B is useful for the Digital Tuning System or others segment type display driver.

■ PACKAGE OUTLINE

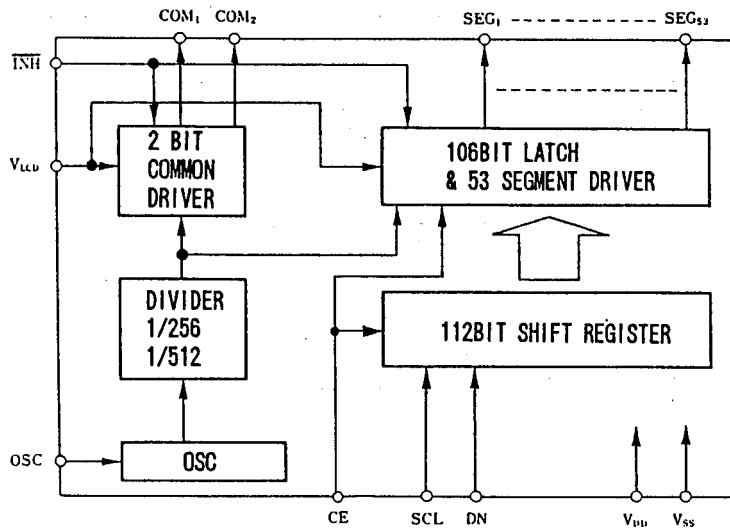


NJU6432BF

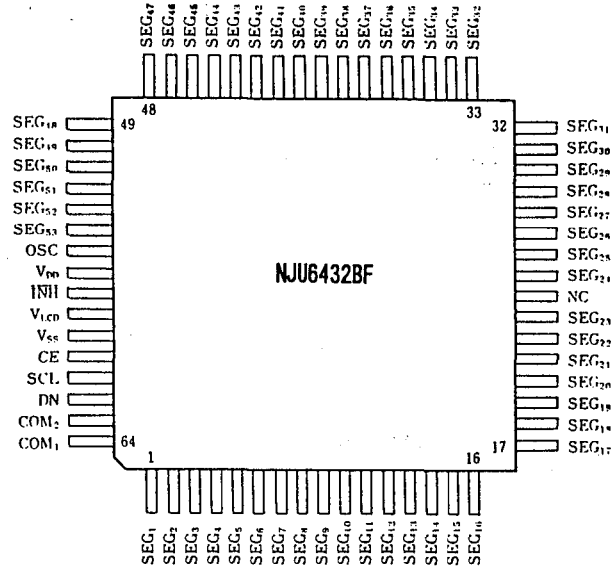
■ FEATURES

- 53 Segment Drivers
- Duty Ratio 1/2 ;104-Segment Drive
- Serial Data Transmission (Shift Clock 2MHz max.)
- Display Off Function (INH Terminal)
- Operating Voltage --- 6.5V Max.
- Package Outline --- QFP 64
- C-MOS Technology

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



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■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1~23 25~53	SEG ₁ ~ SEG ₂₃ SEG ₂₄ ~ SEG ₄₃	Segment Output Terminal
54	SEG ₅₃	Normally On Segment Output Terminal (When the "L" level input to the INH terminal, this segment also turns off.)
55	OSC	Oscillating Terminal
56,59	V _{DD} , V _{SS}	Power Supply
57	INH	Display-Off Control Terminal: When "L" level input to this terminal, all of the display turns off including SEG ₅₃ .
58	V _{LCD}	Power Supply for LCD Driving
60	CE	Chip Enable Terminal
61	SCL	Serial Data Transmission Clock Terminal
62	DN	Serial Data Input Terminal
63 64	COM ₂ COM ₁	Common Output Terminal.
24	NC	Non Connection

(2-3) Input Data Correspond to Segment Terminals

Segment	Data	COM ₁	COM ₂
SEG ₁	D ₁	○	
	D ₂		○
SEG ₂	D ₃	○	
	D ₄		○
SEG ₃	D ₅	○	
	D ₆		○
⋮			
SEG ₂₆	D ₅₁	○	
	D ₅₂		○
SEG ₂₇	D ₅₄	○	
	D ₅₅		○
⋮			
SEG ₄₉	D ₉₈	○	
	D ₉₉		○
SEG ₅₀	D ₁₀₀	○	
	D ₁₀₁		○
SEG ₅₁	D ₁₀₂	○	
	D ₁₀₃		○
SEG ₅₂	D ₁₀₄	○	
	D ₁₀₅		○
SEG ₅₃	ON	○	
	ON		○

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■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage	V _{DD}	- 0.3 ~ + 7.0	V
Operating Voltage	V _{LCD}	- 0.3 ~ V _{DD} +0.3	V
Input Voltage (1)	V _{IN}	- 0.3 ~ + 7.0	V
Input Voltage (2)	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Output Voltage (2)	V _O	- 0.3 ~ V _{DD} +0.3	V
Output Current (3)	I _O	100	μA
Output Current (4)	I _O	1.0	mA
Power Dissipation	P _D	300	mW
Operating Temperature	T _{opr}	- 30 ~ + 85	°C
Storage Temperature	T _{stg}	- 40 ~ + 125	°C

- * 1) CE, SCL, DN Terminals
- * 2) OSC Terminal during OFF-output
- * 3) SEG₁~SEG₅₃ Terminals
- * 4) COM₁, COM₂ Terminals

ELECTRICAL CHARACTERISTICS
DC Characteristics

 (Ta=-30~+85°C. V_{DD}=6.5V, V_{SS}=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{DD}	V _{DD} Terminal	2.5		6.5	V
Supply Voltage	V _{LCD}	V _{LCD} Terminal	2.5		V _{DD}	V
Operating Current	I _{DD}	V _{DD} Terminal			1	mA
Operating Current	I _{LCD}	V _{LCD} Terminal			2	mA
"H" Input Voltage	V _{IH}	T _{NH} Terminal	0.7V _{DD}		6.5	V
"L" Input Voltage	V _{IL}	T _{NH} Terminal	0		0.3V _{DD}	V
"H" Input Voltage	V _{IH}	CE, SCL, DN Terminals	0.8V _{DD}		6.5	V
"L" Input Voltage	V _{IL}	CE, SCL, DN Terminals	0		0.2V _{DD}	V
Oscillator Resistor	R _{osc}	OSC Terminal		51		kΩ
Oscillator Capacitor	C _{osc}	OSC Terminal		680		pF
Oscillator Frequency	f _{osc}	OSC Terminal	25	50	100	kHz
"H" Input Current	I _{IH}	V _{IN} =6.5V, CE, SCL, DN, T _{NH} Terminals			5	μA
"L" Input Current	I _{IL}	V _{IN} =0V, CE, SCL, DN, T _{NH} Terminals			5	μA
"H" Output Voltage	V _{OH}	I _O =-10 μA SEG ₁ ~SEG ₅₃ Terminals	V _{LCD} -1.0			V
"L" Output Voltage	V _{OL}	I _O =10 μA SEG ₁ ~SEG ₅₃ Terminals			1.0	V
"H" Output Voltage	V _{OH}	I _O =-100 μA COM ₁ , COM ₂ Terminals	V _{LCD} -0.6			V
"L" Output Voltage	V _{OL}	I _O =100 μA COM ₁ , COM ₂ Terminals			0.6	V
Middle Level Voltage	V _{MID}	I _O =±100 μA, V _{LCD} =6.5V	2.65	3.25	3.85	V
		I _O =±100 μA, V _{LCD} =3.0V	0.9	1.5	2.1	
Hysteresis Voltage	V _H	V _{DD} =5V, CE, SCL, DN Terminals	0.3			V

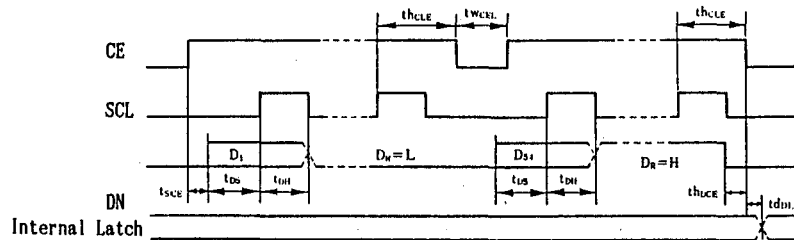
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AC Characteristics

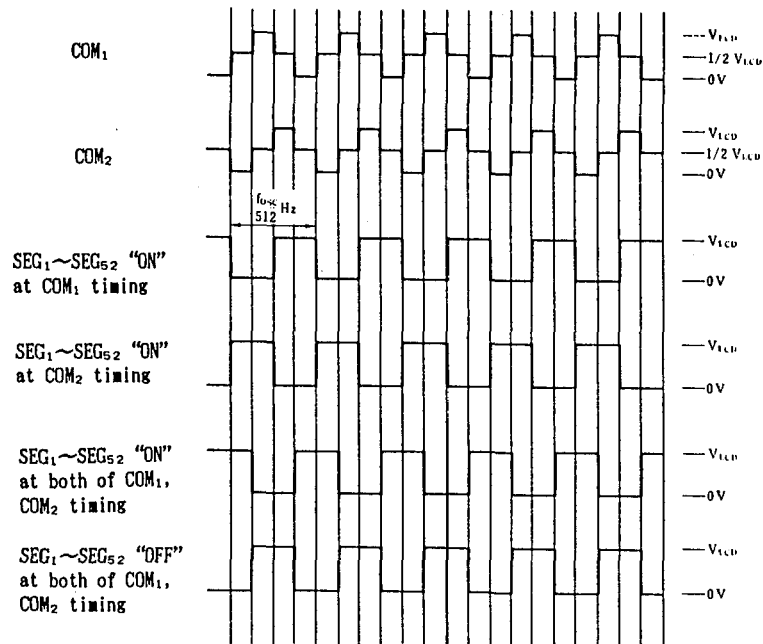
 (Ta=-30~+85°C, V_{DD}=6.5V, V_{SS}=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t _{W_{CLL}}	SCL Terminal	0.25			μs
"H" Clock Pulse Width	t _{W_{CLH}}	SCL Terminal	0.25			μs
Data Set-up Time	t _{DS}	SCL, DN Terminals	0.25			μs
Data Hold Time	t _{DH}	SCL, DN Terminals	0.25			μs
CE Set-up Time	t _{SCE}	CE, DN Terminals	1			μs
CE Hold Time (1)	t _{H_{DCE}}	CE, DN Terminals	1			μs
CE Hold Time (2)	t _{H_{CLE}}	CE, SCL Terminals	1.25			μs
Data Latch Delay Time	t _{d_{DLP}}				1	μs
"L" Clock Enable Pulse Width	t _{W_{CEL}}	CE Terminal	4			μs

• Input Timing Characteristics

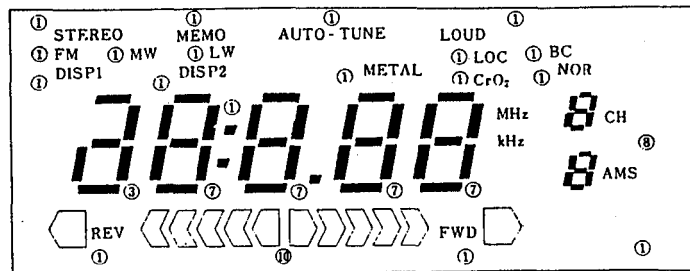

 The data is latched at D_R=H and falling edge of the CE signal condition.

• Output Timing Characteristics



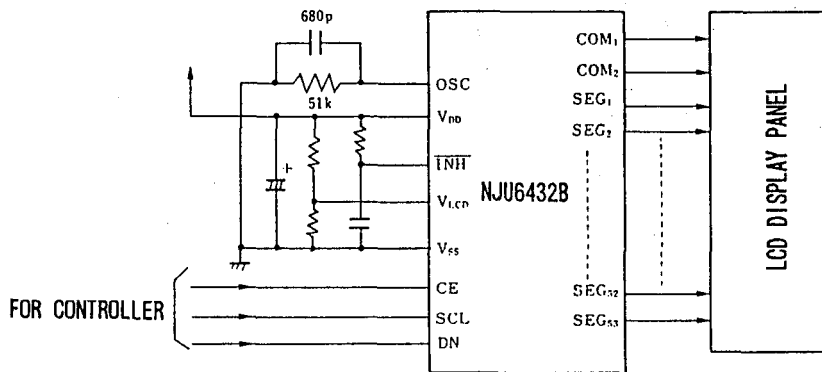
■ DISPLAY EXAMPLE

Example: 71 segments(MAX. 104 segments)

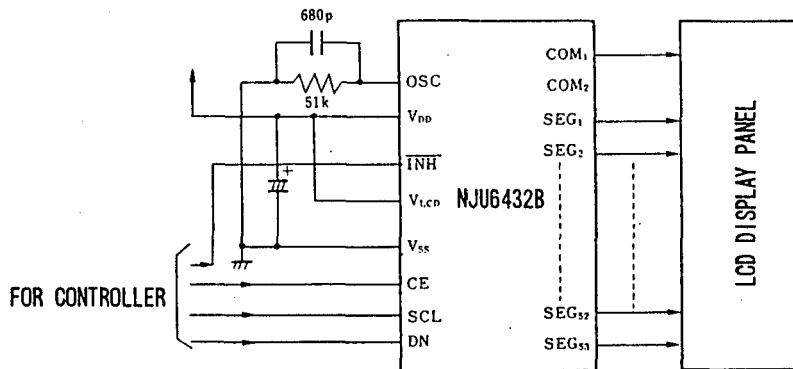


■ APPLICATION CIRCUITS

① In case of $V_{LCD} < V_{DD}$



② In case of $V_{LCD} = V_{DD}$



(Note) After rising edge of V_{DD} voltage, the display data is not guaranteed and which blinking is meaningless display. Therefore, keep \overline{INH} terminal to Low Level by the display data transferred is needed.