# DATA SHEET

## NE/SA572
Programmable analog compandor

Product specification
1987 Oct 7

IC17 Data Handbook

Philips Semiconductors

PHILIPS

# Programmable analog compandor NE/SA572

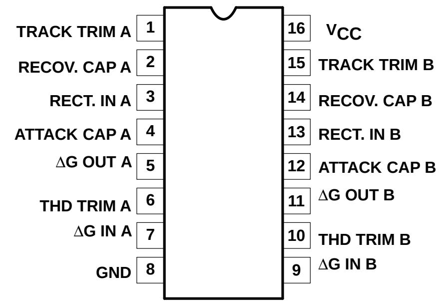
## DESCRIPTION

The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

## PIN CONFIGURATION

**D[1], N, F Packages**




**NOTE:**
1. D package released in large SO (SOL) package only.

*SR00694*

**Figure 1. Pin Configuration**

## FEATURES

- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components

## APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG # |
|---|---|---|---|
| 16-Pin Plastic Small Outline (SO) | 0 to +70°C | NE572D | SOT109-1 |
| 16-Pin Plastic Dual In-Line Package (DIP) | 0 to +70°C | NE572N | SOT38-4 |
| 16-Pin Plastic Small Outline (SO) | –40 to +85°C | SA572D | SOT109-1 |
| 16-Pin Ceramic Dual In-Line Package (Cerdip) | –40 to +85°C | SA572F | 0582B |
| 16-Pin Plastic Dual In-Line Package (DIP) | –40 to +85°C | SA572N | SOT38-4 |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 22 | $V_{DC}$ |
| $T_A$ | Operating temperature range | | |
| | NE572 | 0 to +70 | °C |
| | SA572 | –40 to +85 | |
| $P_D$ | Power dissipation | 500 | mW |

## BLOCK DIAGRAM

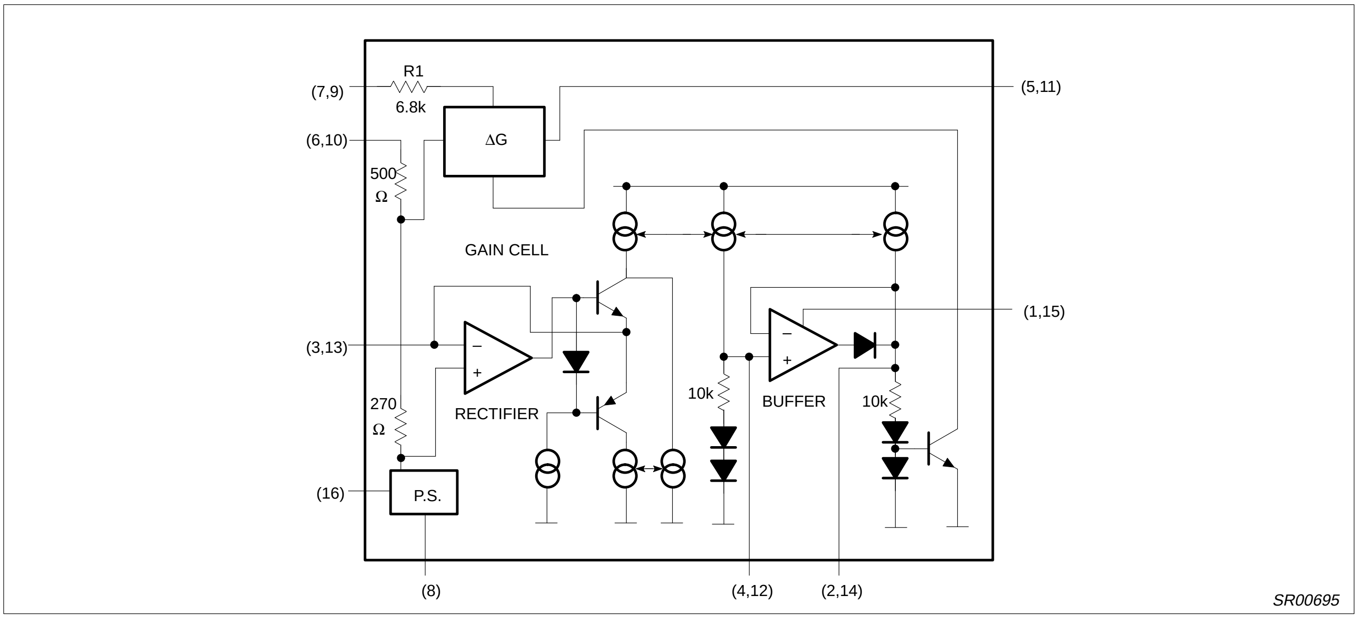



**Figure 2. Block Diagram**

## DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) $V_{CC}$=15V, $T_A$=25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV$_{RMS}$ at 1kHz; $V_1 = V_2$; $R_2$ = 3.3kΩ; $R_3$ = 17.3kΩ.

| SYMBOL | PARAMETER | TEST CONDITIONS | NE572 | | | SA572 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 6 | | 22 | 6 | | 22 | $V_{DC}$ |
| $I_{CC}$ | Supply current | No signal | | | 6 | | | 6.3 | mA |
| $V_R$ | Internal voltage reference | | 2.3 | 2.5 | 2.7 | 2.3 | 2.5 | 2.7 | $V_{DC}$ |
| THD | Total harmonic distortion (untrimmed) | 1kHz $C_A$=1.0µF | | 0.2 | 1.0 | | 0.2 | 1.0 | % |
| THD | Total harmonic distortion (trimmed) | 1kHz $C_R$=10µF | | 0.05 | | | 0.05 | | % |
| THD | Total harmonic distortion (trimmed) | 100Hz | | 0.25 | | | 0.25 | | % |
| | No signal output noise | Input to $V_1$ and $V_2$ grounded (20–20kHz) | | 6 | 25 | | 6 | 25 | µV |
| | DC level shift (untrimmed) | Input change from no signal to 100mV$_{RMS}$ | | ±20 | ±50 | | ±20 | ±50 | mV |
| | Unity gain level | | –1 | 0 | +1 | –1.5 | 0 | +1.5 | dB |
| | Large–signal distortion | $V_1$=$V_2$=400mV | | 0.7 | 3.0 | | 0.7 | 3 | % |
| | Tracking error (measured relative to value at unity gain)= [$V_O$–$V_O$ (unity gain)]dB –$V_2$dB | Rectifier input<br>$V_2$=+6dB $V_1$=0dB<br>$V_2$=–30dB $V_1$=0dB | | ±0.2<br>±0.5 | <br>–1.5<br>+0.8 | | ±0.2<br>±0.5 | <br>–2.5<br>+1.6 | dB |
| | Channel crosstalk | 200mV$_{RMS}$ into channel A, measured output on channel B | 60 | | | 60 | | | dB |
| PSRR | Power supply rejection ratio | 120Hz | | 70 | | | 70 | | dB |

## TEST CIRCUIT

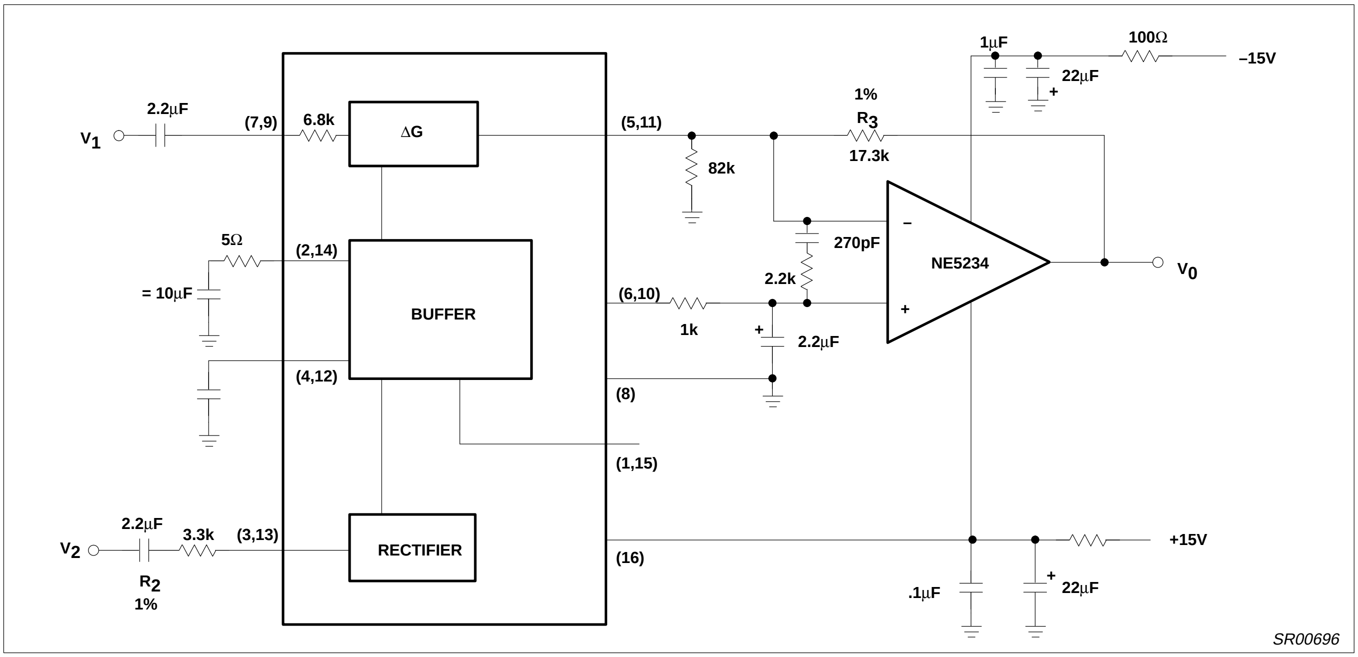



**Figure 3. Test Circuit**

## AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor $C_A$ with an internal 10k resistor $R_A$ defines the attack time $t_A$. The recovery time $t_R$ of a tone burst is defined by a recovery capacitor $C_R$ and an internal 10k resistor $R_R$. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1µF and 1.0µF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7µF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0µF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70 The SA572 is intended for applications from –40°C to +85°C.

## NE572 BASIC APPLICATIONS

### Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

### Gain Cell

Figure 4 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1$-$Q_2$ and $Q_3$-$Q_4$ are both tied to the output and inputs of OPA $A_1$. The negative feedback through $Q_1$ holds the $V_{BE}$ of $Q_1$-$Q_2$ and the $V_{BE}$ of $Q_3$-$Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta_{BE_{Q1Q2}}$$

$$(V_{BE} = V_T \; I_{IN} \; IC/IS)$$

$$V_T I_n \left( \frac{\frac{1}{2} I_G + \frac{1}{2} I_O}{I_S} \right) - V_T I_n \left( \frac{\frac{1}{2} I_G - \frac{1}{2} I_O}{I_S} \right)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

$$V_T I_n \left( \frac{I_1 + I_{IN}}{I_S} \right) - V_T I_n \left( \frac{I_2 - I_1 - I_{IN}}{I_S} \right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

$I_O$ is the differential output current of the gain cell and $I_G$ is the gain control current of the gain cell.

If all transistors $Q_1$ through $Q_4$ are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25µA into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6µV in the audio spectrum (10Hz-20kHz). The output current $I_O$ must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at $V_{REF}$ if the output current $I_O$ is DC coupled.

## Rectifier

The rectifier is a full-wave design as shown in Figure 5. The input voltage is converted to current through the input resistor $R_2$ and turns on either $Q_5$ or $Q_6$ depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block $A_2$. If AC coupling is used, the rectifier error comes only from input bias current of gain block $A_2$. The input bias current is typically about 70nA. Frequency response of the gain block $A_2$ also causes second-order error at high frequency. The collector current of $Q_6$ is mirrored and summed at the collector of $Q_5$ to form the full wave rectified output current $I_R$. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If $V_{IN}$ is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN}(AVG)}{R_2}$$

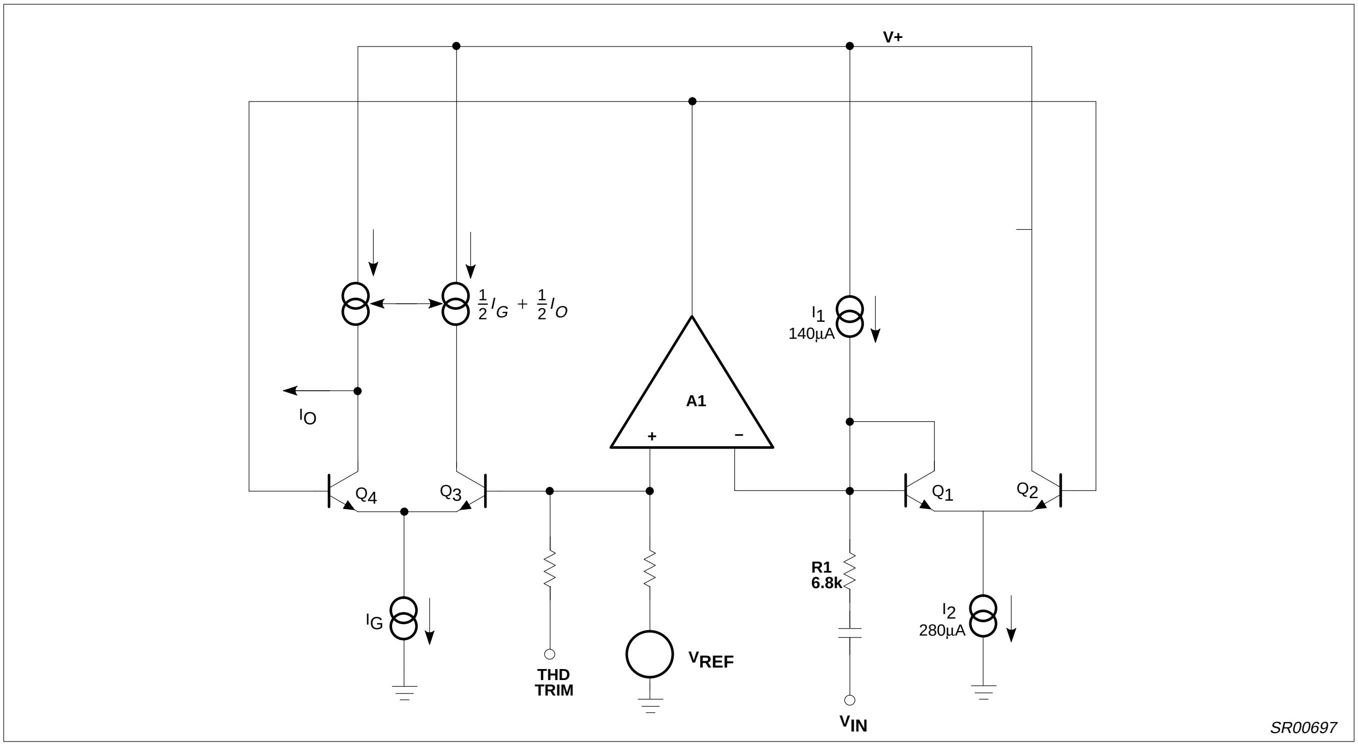



**Figure 4. Basic Gain Cell Schematic**

The internal bias scheme limits the maximum output current $I_R$ to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

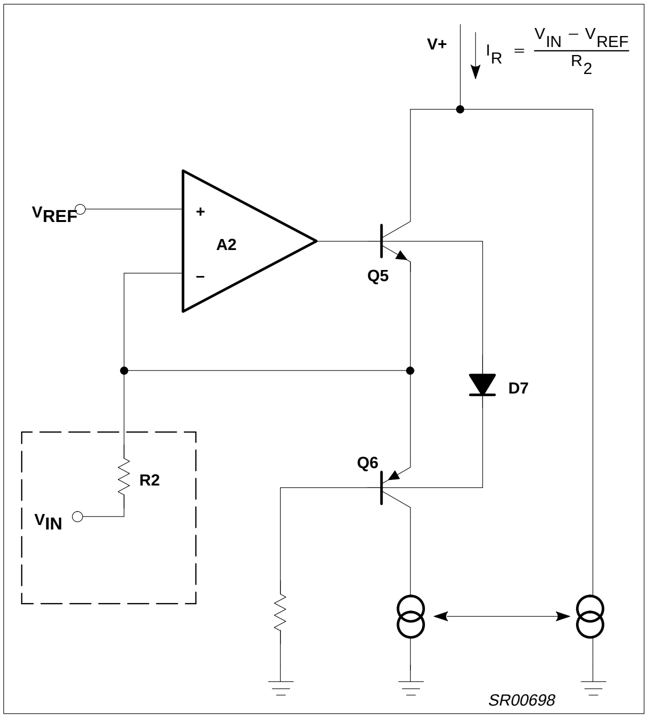



**Figure 5. Simplified Rectifier Schematic**

## Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 6, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier $A_3$ through $Q_8$, $Q_9$ and $Q_{10}$. Diodes $D_{11}$ and $D_{12}$ improve tracking accuracy and provide common-mode bias for $A_3$. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of $A_3$ makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL}\, e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

$Ga_{INT}$=Initial Gain

$Ga_{FNL}$=Final Gain

$\tau_A = R_A \bullet CA = 10k \bullet CA$

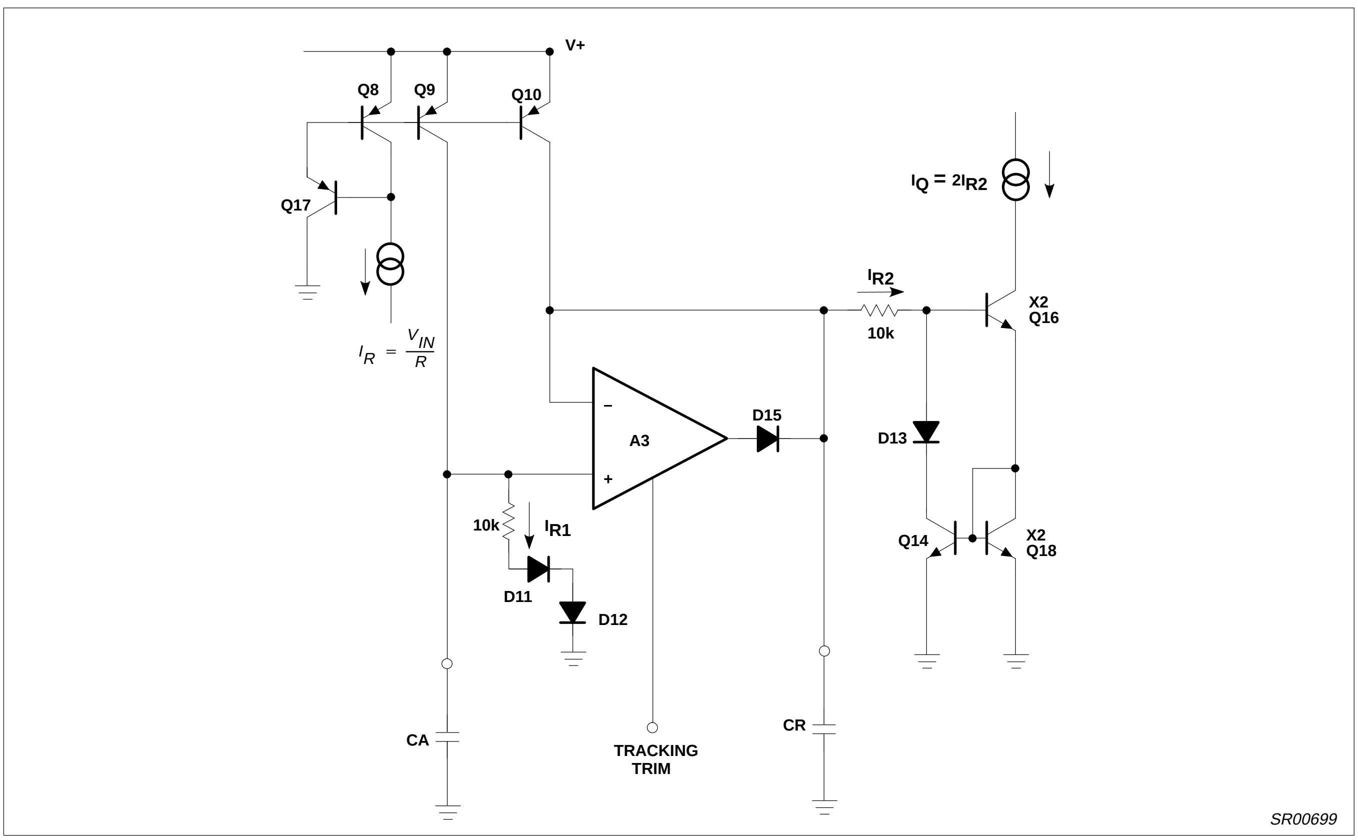



**Figure 6. Buffer Amplifier Schematic**

where $\tau_A$ is the attack time constant and $R_A$ is a 10k internal resistor. Diode $D_{15}$ opens the feedback loop of $A_3$ for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • $R_R$. If the diode impedance is assumed negligible, the dynamic gain $G_R$ (t) for $\Delta G$ is expressed as follows.

$$G_R(t) = (G_{RINT} - G_{RFNL}\, e^{\frac{-t}{\tau_R}} + G_{RFNL}$$

$$G_R(t)=(G_{R\ INT}–G_{R\ FNL})\ e\ +G_{R\ FNL}$$

$$\tau R=R_R \bullet CR=10k \bullet CR$$

where $\tau R$ is the recovery time constant and $R_R$ is a 10k internal resistor. The gain control current is mirrored to the gain cell through $Q_{14}$. The low level gain errors due to input bias current of $A_2$ and $A_3$ can be trimmed through the tracking trim pin into $A_3$ with a current source of ±3µA.

### Basic Expandor

Figure 7 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

$(I_1=140\mu A)$

Both the resistors $R_1$ and $R_2$ are tied to internal summing nodes. $R_1$ is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140µA. This corresponds to a voltage level of 140µA • 6.8k=952mV peak. The input peak current into the rectifier is limited to 300µA by the internal bias system. Note that the value of $R_1$ can be increased to accommodate higher input level. $R_2$ and $R_3$ are external resistors. It is easy to adjust the ratio of $R_3/R_2$ for desirable system voltage and current levels. A small $R_2$ results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer $A_1$ may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA $A_2$. $R_3$ and $A_2$ convert the gain cell output current to the output voltage. In high-performance applications, $A_2$ has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of $A_2$ can be biased at the low noise internal reference Pin 6 or 10. Resistor $R_4$ is used to bias up the output DC level of $A_2$ for maximum swing. The output DC level of $A_2$ is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\,\frac{R_3}{R_4} \qquad (6)$$

$V_B$ can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant. *5COL

### Basic Compressor

Figure 8 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA $A_1$. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}}\right)^{\frac{1}{2}} \qquad (7)$$

$R_{DC1}$, $R_{DC2}$, and CDC form a DC feedback for $A_1$. The output DC level of $A_1$ is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) \qquad (8)$$
$$- V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

The zener diodes $D_1$ and $D_2$ are used for channel overload protection.

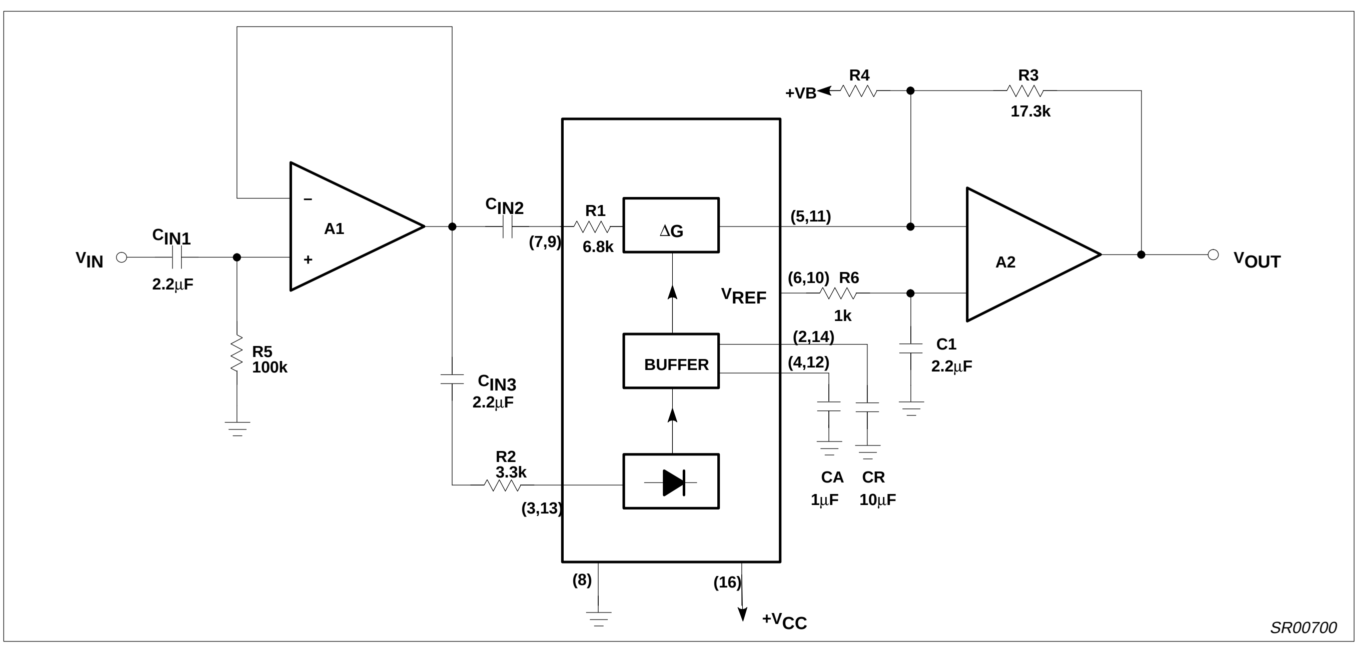



**Figure 7. Basic Expandor Schematic**

## Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 9 shows the system level diagram for reference.

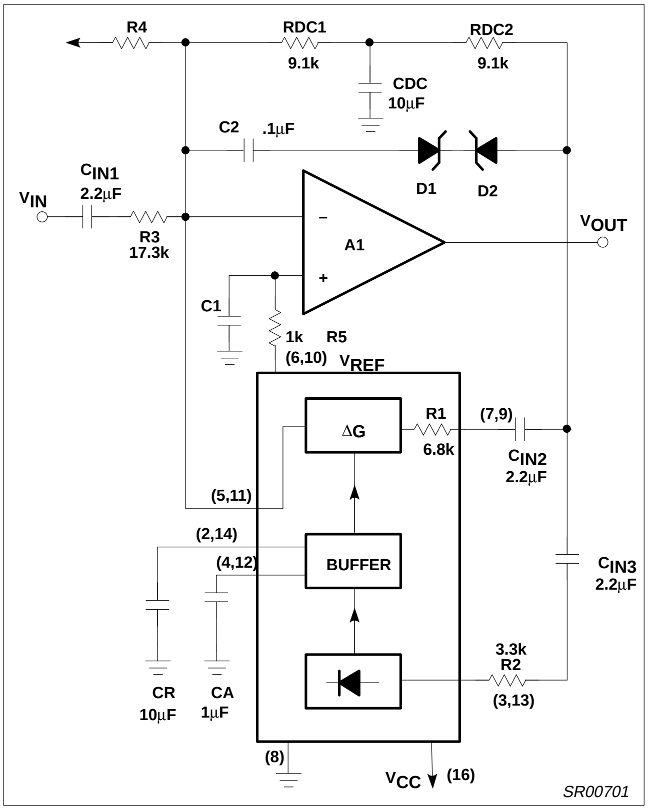



**Figure 8. Basic Compressor Schematic**

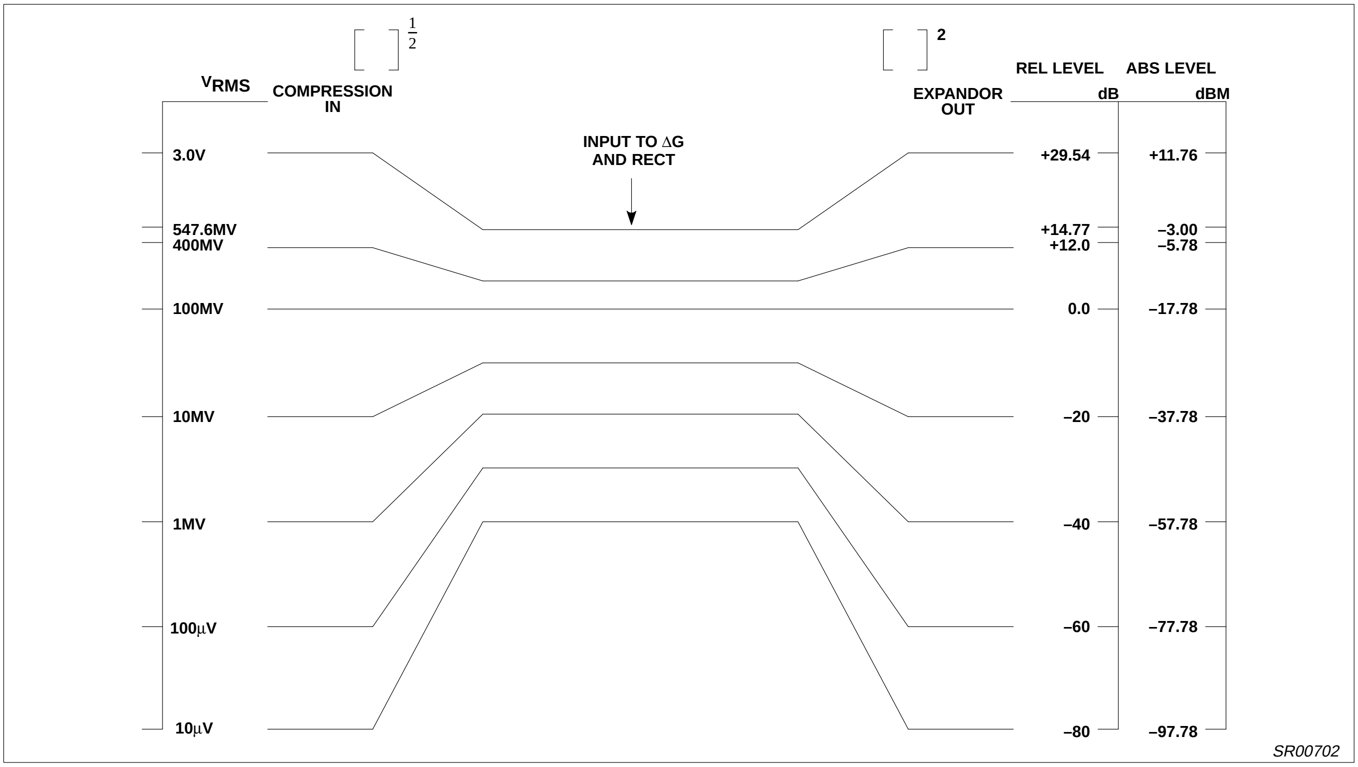
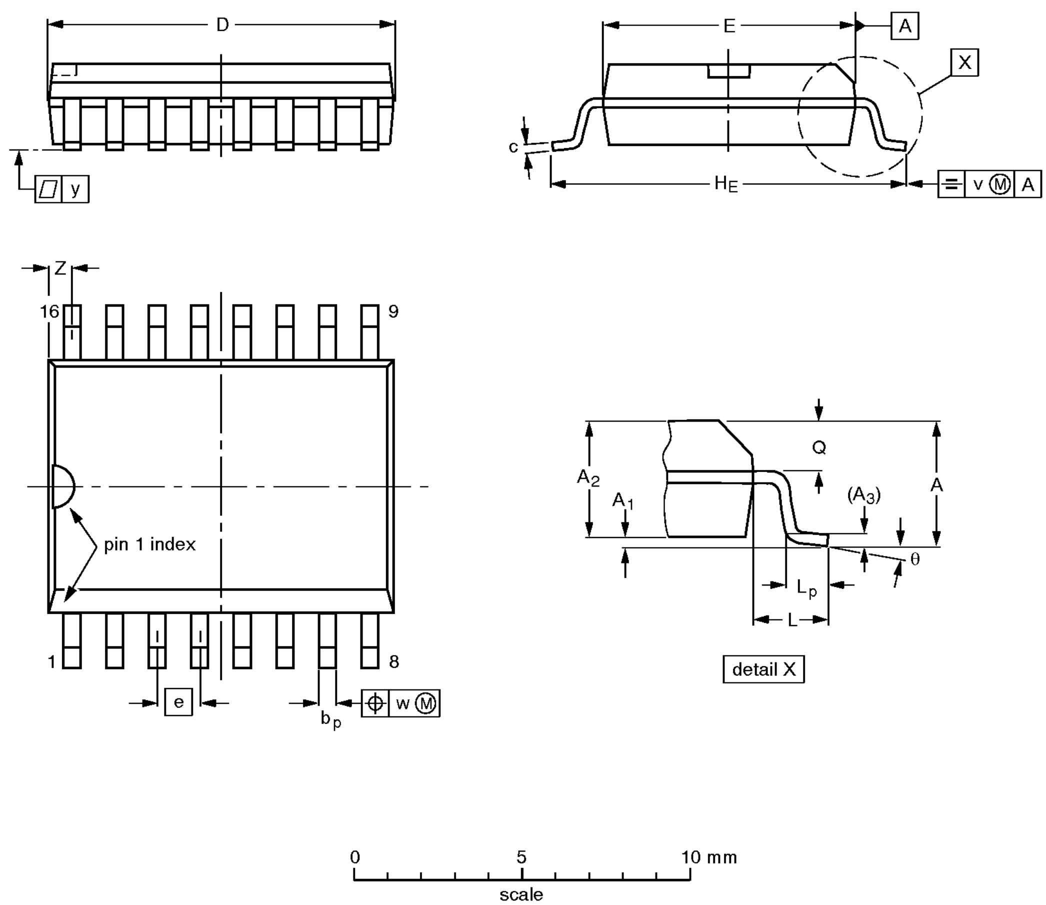



**Figure 9. NE572 System Level**

## SO16: plastic small outline package; 16 leads; body width 7.5 mm SOT162-1




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

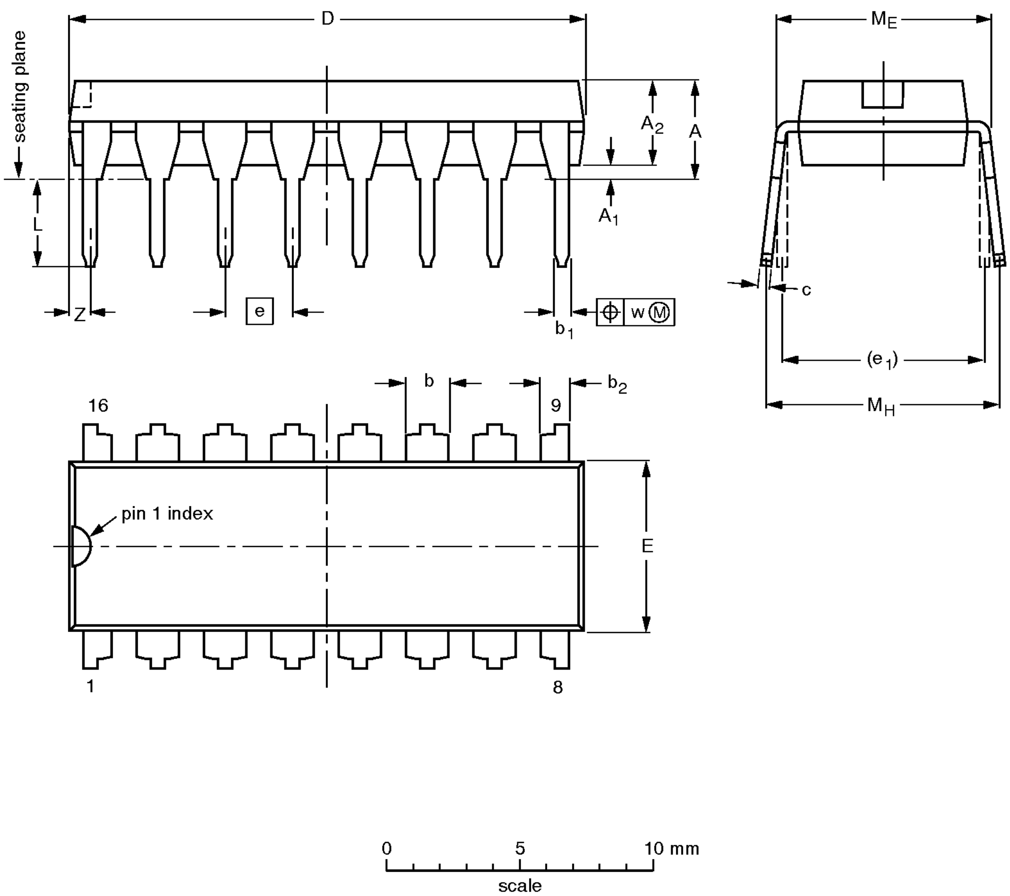
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D [1] | E [1] | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z [1] | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 10.5<br>10.1 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.41<br>0.40 | 0.30<br>0.29 | 0.050 | 0.42<br>0.39 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT162-1 | 075E03 | MS-013AA | | | | ~~92-11-17~~<br>95-01-24 |

## DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.030 |

**Note**

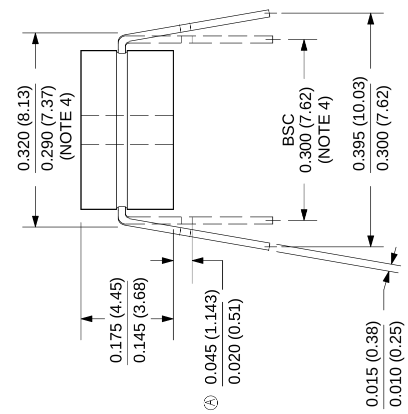
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

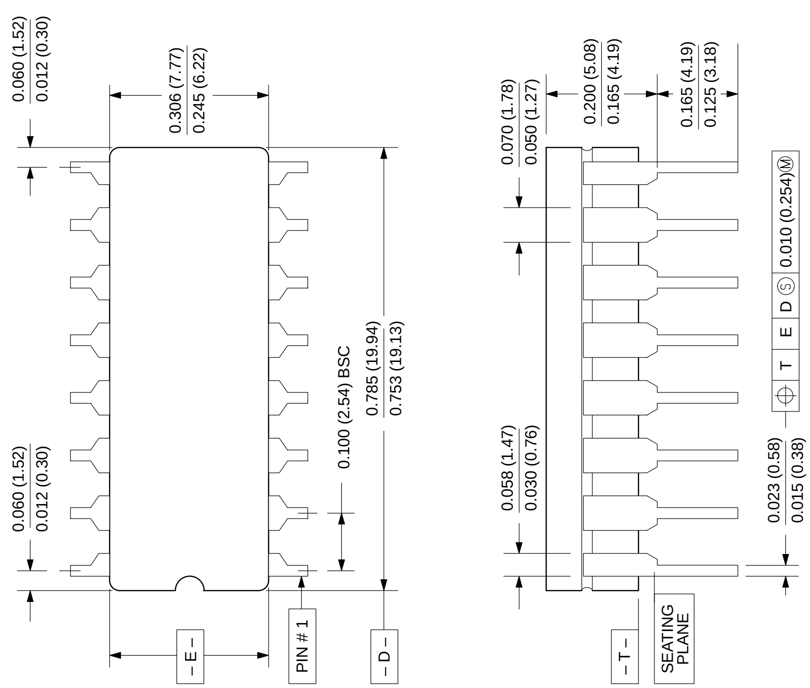
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-4 | | | | | | ~~92-11-17~~<br>95-01-14 |

## 0582B 16-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE

**NOTES:**

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.

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# Programmable analog compandor NE/SA572

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | Full Production | This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product. |



**Philips Semiconductors**
**811 East Arques Avenue**
**P.O. Box 3409**
**Sunnyvale, California 94088–3409**
**Telephone 800-234-7381**



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