

S5486-A,F,W • N7486-A,F

DIGITAL 54/74 TTL SERIES

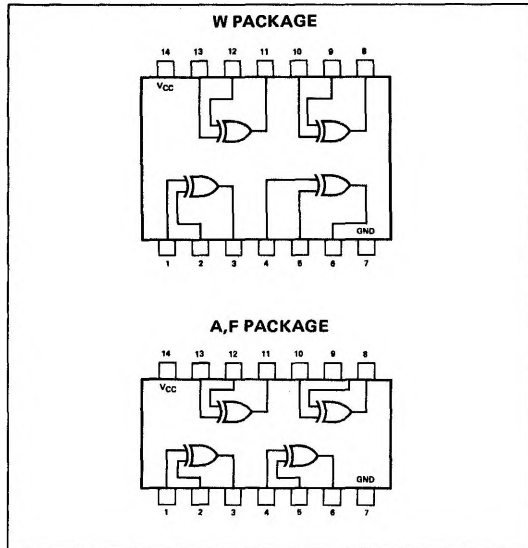
### DESCRIPTION

The 54/7486 Quad 2-Input Exclusive OR Gate is a TTL element providing the function  $\overline{A}B + A\overline{B}$  at the output.

### TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

### PIN CONFIGURATIONS



### RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$	S5486 Circuits	4.5	5	5.5	V
	N7486 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each output, N:	Logical 0			10	
	Logical 1			20	

### ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal $V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal $V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage $V_{CC} = \text{MIN}, V_{in(1)} = 2V,$ $V_{in(0)} = 0.8V, I_{load} = -800 \mu A$	2.4			V
$V_{out(0)}$	Logical 0 output voltage $V_{CC} = \text{MIN}, V_{in(1)} = 2V,$ $V_{in(0)} = 0.8V, I_{sink} = 16mA$			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input) $V_{CC} = \text{MAX}, V_{in} = 2.4V$ $V_{CC} = \text{MAX}, V_{in} = 5.5V$			40 1	$\mu A$ mA
$I_{in(0)}$	Logical 0 level input current (each input) $V_{CC} = \text{MAX}, V_{in} = 0.4V$			-1.6	mA
$I_{OS}$	Short circuit output current† $V_{CC} = \text{MAX}, V_{in(1)} = 4.5V,$ $V_{in(0)} = 0$	-20 -18		-55 -55	mA
$I_{CC}$	Supply current $V_{CC} = \text{MAX}, V_{in} = 4.5V$		30 30	43 50	mA

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SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level (other input low)	$C_L = 15pF$ ,	$R_L = 400$		11	17	ns
$t_{pd1}$	Propagation delay time to logical 1 level (other input low)	$C_L = 15pF$ ,	$R_L = 400$		15	23	ns
$t_{pd0}$	Propagation delay time to logical 0 level (Other input high)	$C_L = 15pF$ ,	$R_L = 400$		13	22	ns
$t_{pd1}$	Propagation delay time to logical 1 level (other input high)	$C_L = 15pF$ ,	$R_L = 400$		18	30	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

+ Not more than one output should be shorted at a time.