

# J-K FLIP-FLOP | S5470 N7470

S5470-A,F,W • N7470-A,F

DIGITAL 54/74 TTL SERIES

## DESCRIPTION

The S5470/N7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and  $\bar{Q}$  outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The S5470/N7470 flip-flop is ideally suited for medium- and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

## TRUTH TABLE

### LOGIC

$J_n$	$K_n$	$Q_{n+1}$	PRESET	CLEAR	Q
0	0	$Q_n$	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\bar{Q}_n$	1	1	Q

$$J = J_1 J_2 J^* \quad K = K_1 K_2 K^*$$

n is time prior to clock

n + 1 is time following clock

† Both outputs in 0 state

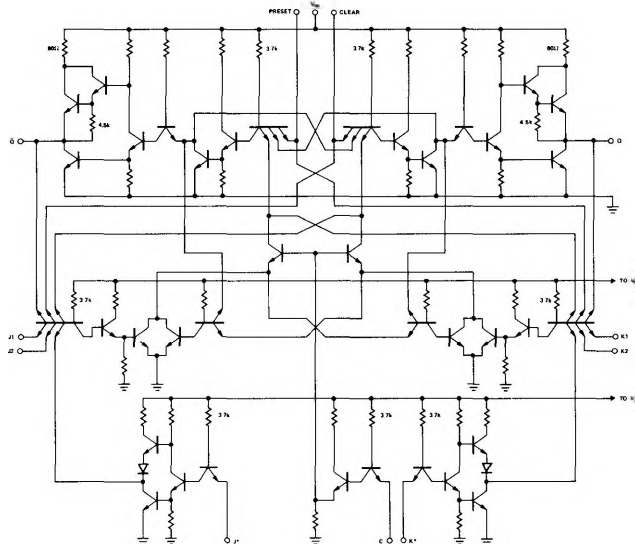
## POSITIVE LOGIC

Low input to preset sets Q to logical 1

Low input to clear sets Q to logical 0

Preset or clear function can occur only when clock input is low.

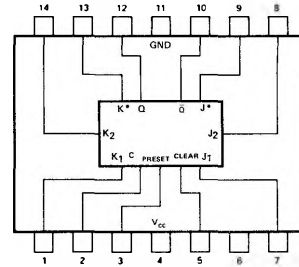
## SCHEMATIC DIAGRAM



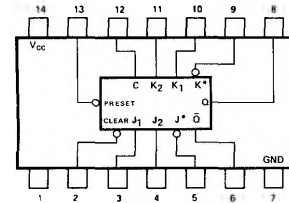
NOTE: Component values are typical.

## PIN CONFIGURATIONS

### W PACKAGE



### A,F PACKAGE



**SIGNETICS DIGITAL 54/74 TTL SERIES – S5470 • N7470**

**RECOMMENDED OPERATING CONDITIONS**

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5470 Circuits	4.5	5	5.5	V
N7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, $T_A$ : S5470 Circuits	-55	25	125	°C
N7470 Circuits	0	25	70	°C
Normalized Fanout from each Output, N			10	
Clock Pulse Transition Time to Logical 1 Level, $t_1$ (clock)	5		150	ns
Width of Clock Pulse, $t_p$ (clock)	20			ns
Width of Preset Pulse, $t_p$ (preset)	25			ns
Width of Clear Pulse, $t_p$ (clear)	25			ns

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	2.4	3.5		V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$		0.22	0.4	V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J*, K1, K2, K*, or clock	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at preset or clear	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	$V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			40 1	$\mu\text{A}$ mA
$I_{in(1)}$ Logical 1 level input current at preset or clear	$V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			80 1	$\mu\text{A}$ mA
$I_{OS}$ Short circuit output current†	$V_{CC} = \text{MAX}$ , $V_{in} = 0$	S5470 N7470		-20 -75 -75	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$		13	26	mA

**SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ , N = 10**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	15	35		MHz
$t_{setup}$ Minimum Input Setup time	$C_L = 15\text{pF}$ , $R_L = 400\Omega$		10	20	ns
$t_{hold}$ Minimum input hold time	$C_L = 15\text{pF}$ , $R_L = 400\Omega$		0	5	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clear or preset to output	$C_L = 15\text{pF}$ , $R_L = 400\Omega$			50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear or preset to output	$C_L = 15\text{pF}$ , $R_L = 400\Omega$			50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	10	27	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	10	18	50	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time.