

# 4-BIT PARALLEL-ACCESS SHIFT REGISTER

# S54195 N74195

S54195-B,F,W • N74195-B, F

DIGITAL 54/74 TTL SERIES

## DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear.

The registers have two modes of operation:

Parallel (Broadside) Load

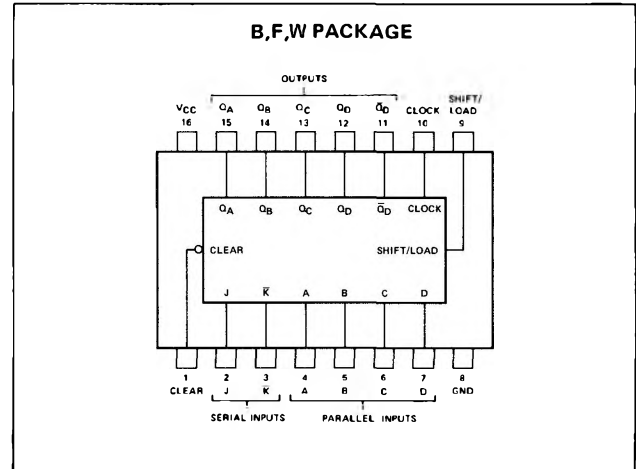
Shift (In direction  $Q_A$  toward  $Q_D$ )

Parallel loading is accomplished by applying the 4 bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode are entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The S54195 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; the N74195 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

## PIN CONFIGURATIONS



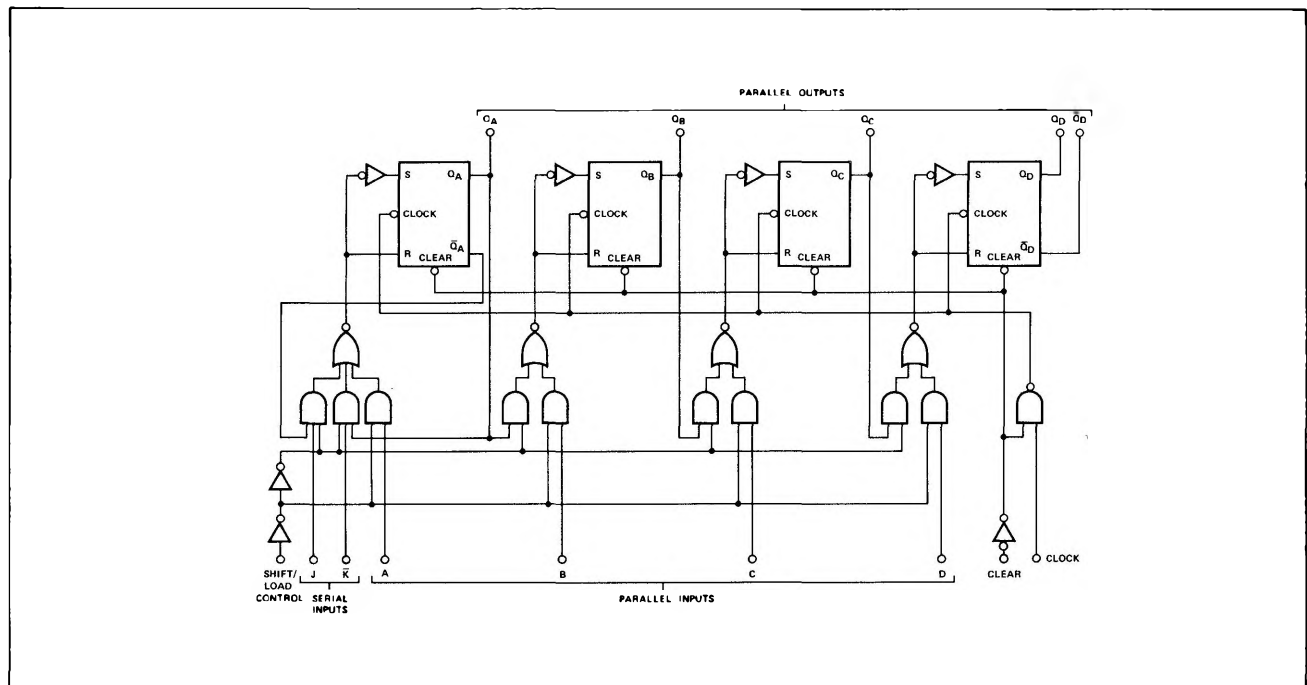
## TRUTH TABLE

Inputs at $t_n$		Outputs at $t_{n+1}$				
J	K	$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\bar{Q}_D$
L	H	$Q_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
L	L	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	L	$\bar{Q}_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$

H = High Level, L = Low Level

- NOTES
- $t_n$  = bit time before clock pulse
  - $t_{n+1}$  = bit time after clock pulse
  - $Q_{An}$  = state of  $Q_A$  at  $t_n$

## LOGIC DIAGRAM



SIGNETICS DIGITAL 54/74 TTL SERIES — S54195 • N74195

RECOMMENDED OPERATING CONDITIONS

	S54195			N74195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level			20			20
	Low logic level			10			10
Input Clock Frequency, $f_{clock}$	0		30	0		30	MHz
Width of Clock Input Pulse, $t_w(\text{clock})$	16			16			ns
Width of Clear Input Pulse, $t_w(\text{clear})$	12			12			ns
Setup Time, $t_{setup}$ :	Shift/load			25			
	Serial and parallel data			15			ns
Clear inactive-state	25			25			
Shift/Load Release Time, $t_{release}$				10			ns
Serial and Parallel Data Hold Time, $t_{hold}$	0			0			ns
Operating Free-Air Temperature, $T_A$	-55			125			°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_I$	Input clamp voltage			-1.5	V
$V_{OH}$	High-level output voltage	2.4			V
$V_{OL}$	Low-level output voltage			0.4	V
$I_I$	Input current at maximum input voltage			1	mA
$I_{IH}$	High-level input current			40	$\mu$ A
$I_{IL}$	Low-level input current			-1.6	mA
$I_{OS}$	Short-circuit output current†				mA
$I_{CC}$	Supply current				mA

$V_{CC} = \text{MIN.}, I_I = -12\text{mA}$   
 $V_{CC} = \text{MIN.}, V_{IH} = 2\text{V}, I_{OH} = -800\mu\text{A}$   
 $V_{CC} = \text{MIN.}, V_{IL} = 0.8\text{V}, V_{IH} = 2\text{V}, I_{OL} = 16\text{mA}$   
 $V_{CC} = \text{MAX.}, V_I = 5.5\text{V}$   
 $V_{CC} = \text{MAX.}, V_I = 2.4\text{V}$   
 $V_{CC} = \text{MAX.}, V_I = 0.4\text{V}$   
 S54195:  $V_{CC} = \text{MAX.}, I_{OS} = -20$   
 N74195:  $V_{CC} = \text{MAX.}, I_{OS} = -18$   
 See Note for  $I_{CC}$

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$	Maximum input clock frequency	30	39		MHz
$t_{PHL}$	Propagation delay time, high-to-low-level output from clear		19	30	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock	6	14	22	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock	7	17	26	ns

$C_L = 15\text{pF}, R_L = 400\Omega$

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time.

NOTE With all outputs open, shift/load grounded, and 4.5V applied to the  $J, \bar{K}$ , and data inputs,  $I_{CC}$  is measured by applying a momentary ground, followed by 4.5V, to clear, and then applying a momentary ground, followed by 4.5V, to clock.