

DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear.

The registers have two modes of operation:

Parallel (Broadside) Load

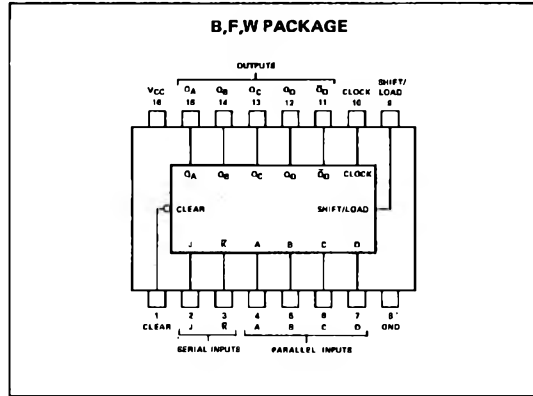
Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the 4 bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode are entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The S54195 is characterized for operation over the full military temperature range of -55°C to 125°C ; the N74195 is characterized for operation from 0°C to 70°C .

PIN CONFIGURATIONS



TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	K	Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	L	\bar{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}

H = High Level, L = Low Level

- NOTES
- A. t_n = bit time before clock pulse
 - B. t_{n+1} = bit time after clock pulse
 - C. Q_{An} = state of Q_A at t_n

LOGIC DIAGRAM

