

MSM6404VS

MSM6404 PIGGY BACK

GENERAL DESCRIPTION

The MSM6404VS is a device whose built-in ROM is replaced by external EPROM using the piggy-back method.

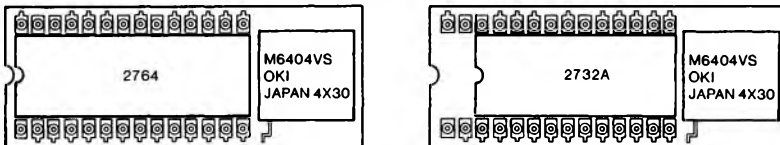
FEATURES

- Supply Voltage: $5V \pm 5\%$
- Frequency: DC ~ 4.2 MHz
- Operating Temperature: $0 \sim 70^{\circ}\text{C}$

Note: There are a few differences in the electrical characteristics of this chip and the evaluation chip. Please refer to next page for the detail.

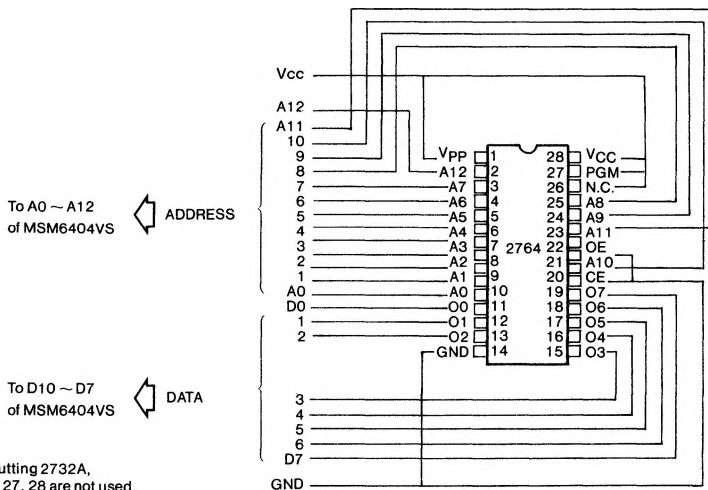
PUTTING METHOD OF ROM

Please refer to drawing below.

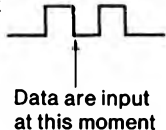
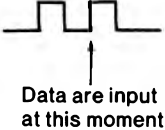
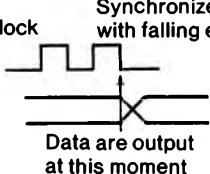
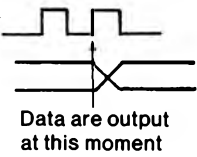
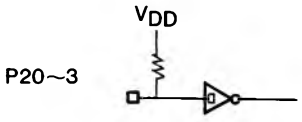
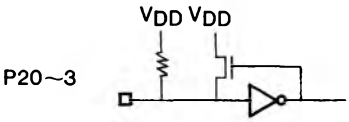


PIN CONFIGURATION

Pin Connection between MSM6404VS and EPROM



DIFFERENCES BETWEEN MSM6404 AND MSM6404 VS (PIGGY-BACK)

Item	6404	6404VS (Piggy-Back)
1. Port initialization during reset	Port P0, 1, 3 are set to "1" and port 2, 4, 5, 6, 7, 8 are reset to "0" directly by signal put into the RESET.	Port P0, 1, 3 are set to "1" and port 2, 4, 5, 6, 7, 8 are reset to "0" during reset cycle being executed.
2. Timer Operation	After being reset, timer stops counting until data are set in it.	It is undecidable whether the timer starts counting or not after being reset. Therefore, the timer should be initialized by software.
3. Shift register	Serial Out F/F (SOF/F) is set to "0" after being reset.	It is undecidable whether Serial Out F/F (SOF/F) is set to "0" or "1" after being reset. Therefore Serial Out F/F should be initialized by software.
4. Port input/output timing	Internal clock 	Internal clock 
	Internal clock 	Internal clock 
5. Port input/output (maracteristics)	TTL F0=1 (I _{OL} = 1.6 mA 0.4V)	LSTTL F0=1 (I _{OL} = 0.4 mA 0.4V)
		
	TTL compatible input P00~P83 (Except P20~3)	CMOS input P00~83 (Except P20~3)
Available ROM capacity	4K byte	Accessible up to 8K byte
IPL call instruction	Not available	Available