OKI semiconductor

MSM28201AS

1M BIT MASK ROM FOR CHINESE-CHARACTER PATTERN

GENERAL DESCRIPTION

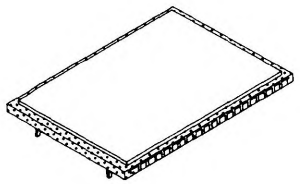
MSM28201 is a 1M-bit mask ROM employing an N-channel silicon gate MOS process, and with 3760 chinese-characters (kanji conforming with JIS no.2 standards) incorporated in a single chip.

With this large capacity, 3760 chinese-character patterns can be generated in a single chip. And by only a single input of JIS chinese-character code via the address pin, 18-row x 16-column dot matrix character forms can be obtained from the data output pin, making this device ideal for construction of functionally versatile chinese-character terminals.

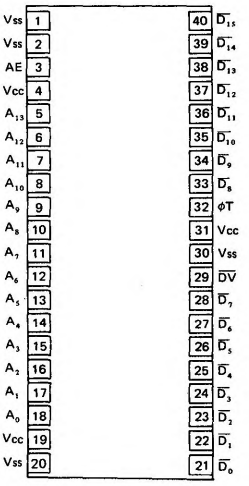
The power supply voltage is 5V single, the input level TTL compatible, outputs are tri-state data out, and data valid is denoted by open collector. The device is mounted in a 40-pin DIP.

FEATURES

- Function . . . . . 18 x 16 chinese-character font output
- Configuration . . . . Duplex configuration employing defect permissible technique
- Storage capacity . . . 1082880 bits
- Number of generated characters . . . . . 3384 characters
- Accommodation character region . . . Chinese-character encoded partitions 48 to 87 for JIS data processing.
- Address input . . . . 14 bits (A_0 to A_{13})
- Data output . . . . . 16 bits ($\overline{D_0}$ to $\overline{D_{15}}$, tristate)
- Output mode . . . . 16 bit x 18 transfers
- Address enable . . . 1 (AE)
- Data valid . . . . . 1 ($\overline{DV}$, open collector output)
- Clock . . . . . 1 (ϕT) DC to 500kHz
- Operating temperature . . . . . Ta=0°C to 70°C
- Access time . . . . . 25us MAX.
- Data transfer rate . . 8MBits/sec.
- Interface . . . . . TTL level
- Power supply voltage 5V single (±5%)
- Power consumption . 500mW TYP
- Package . . . . . Ceramic 40-pin DIP
- Process . . . . . E/D MOS process
- Memory cell . . . . . Multi-gate ROM



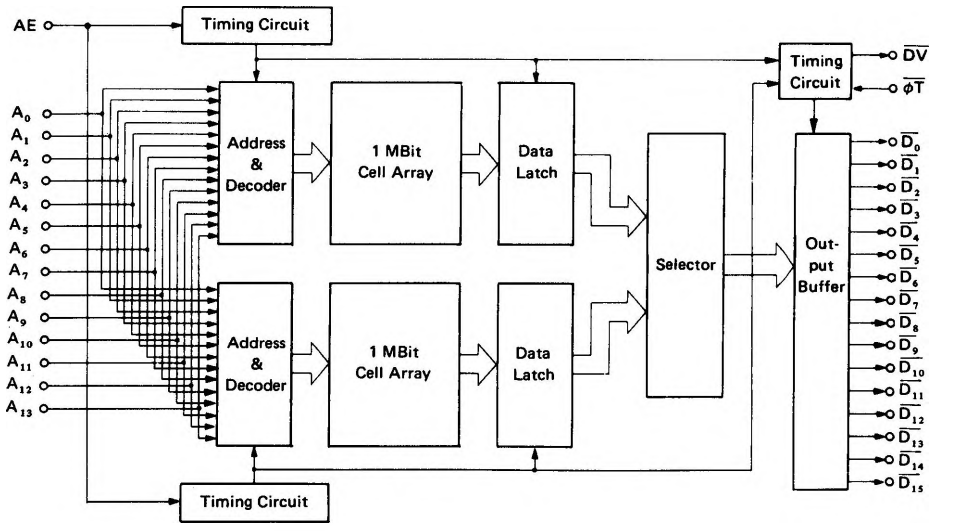
PIN CONFIGURATION



$A_0 \sim A_{13}$: Address inputs
$\overline{D_0} \sim \overline{D_{15}}$: Data outputs
AE : Address enable
$\overline{DV}$: Data valid output
ϕT : Clock input
Vcc : Power supply voltage (5 V)
Vss : GND (0 V)

Note: All Vss pins are to be connected

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	Vcc	Respect to Vss	−0.3~7	V
Input voltage	V_I	Respect to Vss	−0.3~7	V
Output voltage	V_O	Respect to Vss	−0.3~7	V
Permissible loss	P_D		2	W
Operating temperature	Topr		0 ~ 70	°C
Storage temperature	Tstg		−35~125	°C

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Conditions	Range Value			Unit
			MIN	TYP	MAX	
Power supply voltage	Vcc	5 V ± 5%	4.75	5	5.25	V
Power supply voltage	Vss		0	0	0	V
"H" input voltage	V_{IH}	Respect to Vss	2.0	5	6	V
"L" input voltage	V_{IL}	Respect to Vss	−0.3	0	0.8	V
Operating temperature	Topr		0		70	°C

DC CHARACTERISTICS

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Item	Symbol	Conditions	Range Value			Unit
			MIN	TYP	MAX	
"H" output voltage	V_{OH}	I_{OH}=−0.2mA	2.4		Vcc	V
"L" output voltage	V_{OL}	I_{OL}=1.6mA			0.6	V
	V_{OL}	I_{OL}=0.8mA			0.4	V
Input leak current	I_{LI}	V_I=0 ~ Vcc	−10		10	μA
Output leak current	I_{LO}	V_O=0 ~ Vcc V_{AE}=0.8V	−10		10	μA
Average power supply current	I_{CCA}	t_{RC}=61μs, t_C=2μs t_{AE}=500ns			120	mA
Rated power supply current	I_{CCS}	V_{AE}=0.8V			120	mA

AC CHARACTERISTICS

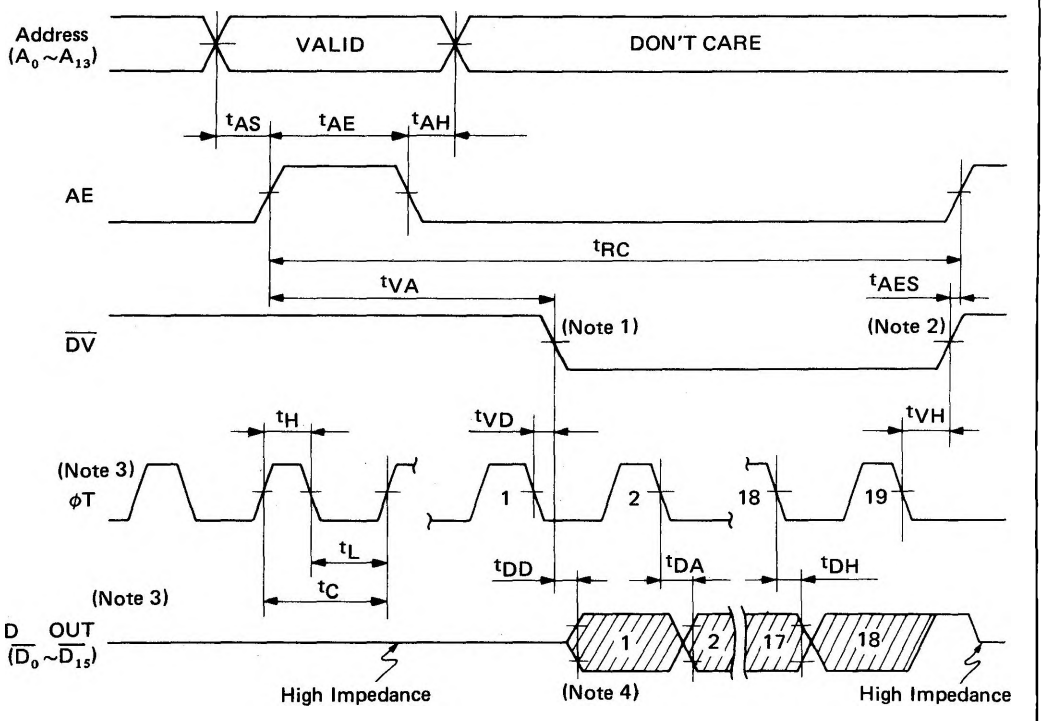
TIMING CONDITIONS

Item	Conditions
Input signal level	V_{IH}=2.0 V, V_{IL}=0.8 V
Input rise/fall time	tr=tf=15ns
Input timing level	1.5V
Output load	C_L=50pF, 1TTL Gate

READ CYCLE

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Item	Symbol	Conditions	Range Value			Unit
			MIN	TYP	MAX	
Read cycle time	t_{RC}		61			μs
Address set-up time	t_{AS}		0			0=ns
AE pulse width	t_{AE}		500			0=ns
Address hold time	t_{AH}		300			0=ns
$\overline{DV}$ access time	t_{VA}				25	μs
$\overline{DV}$ delay time	t_{VD}		400		800	0=ns
$\overline{DV}$ hold time	t_{VH}				900	0=ns
ϕT pulse width	t_H		200			0=ns
ϕT delay time	t_L		1800			0=ns
Output delay time	t_{DD}		0			0=ns
Output access time	t_{DA}				800	0=ns
Output hold time	t_{DH}		400			0=ns
AE set-up time	t_{AES}					0=ns



NOTE:
1. $\overline{DV}$ is determined by the ϕT falling edge.
2. $\overline{DV}$ is changed by the ϕT falling edge.
3. ϕT and DnDATA are repeated 18 times when $\overline{DV}$ is low.
4. $\overline{Dn}$ timing levels of 2.0V and 0.8V.
5. Normal operation may not be possible unless there is at least one AE dummy input after the power is switched on.
6. $\overline{DV}$ denotes open collector output, and $\overline{Dn}$ the tristate output.

INPUT/OUTPUT CAPACITY

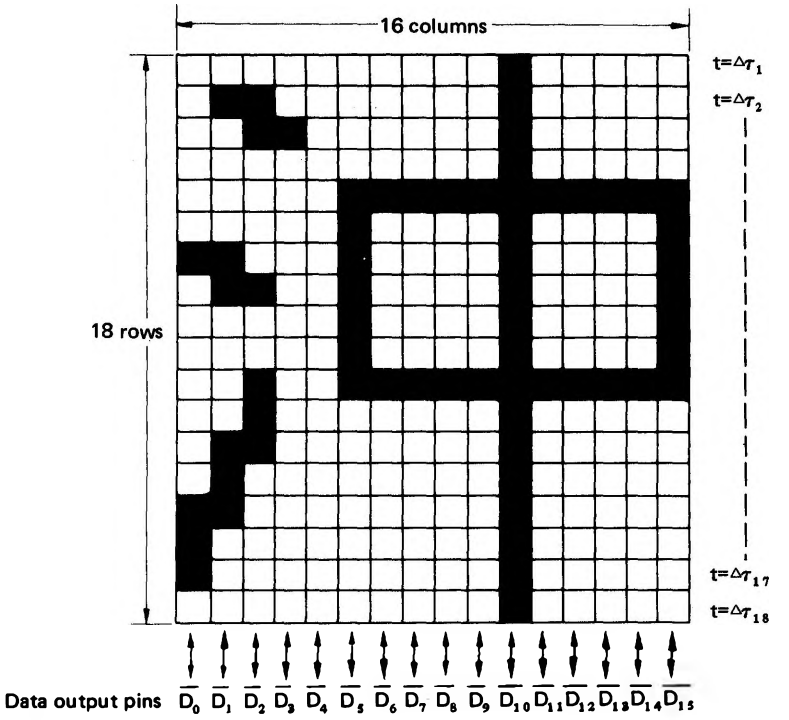
(Ta=25°C, f=1 MHz)

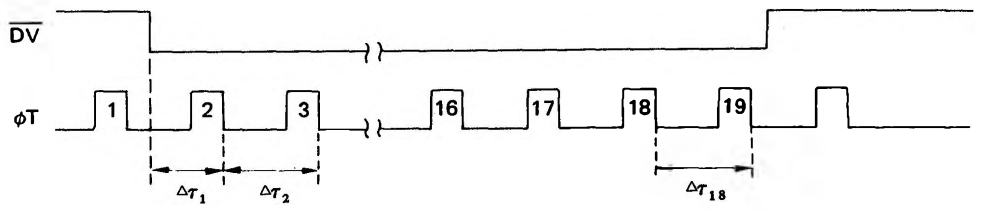
Item	Symbol	Conditions	Range Value			Unit
			MIN	TYP	MAX	
Input capacity (excluding AE)	C_I	V_I=0 V			15	pF
Input capacity (AE pin)	C_I	V_I=0 V			35	pF
Output capacity	C_O	V_O=0 V			10	pF

FUNCTIONAL CHARACTERISTICS

Item	Range	Unit	Remarks
Font format	18-row x 16-column dot matrix		
Output mode	16 bit x 18 transfers		(Note 1)
Number of characters generated	3384	Word	
Character accommodation region	48~87 (JIS No.2 standard)	Partition	(Note 2)

Note 1. The relation between the 18-row x 16-column matrix and the data output pins is outlined below. The output is low (V_{OL}) for the character portion, and high (V_{OH}) for the background area.





Note 2. The address pins are related to the JIS C6226 no.1 and no.2 bytes in the following way.

JIS C 6226	No.2 byte							No.1 bytes						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0