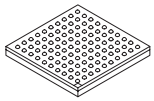
Order Number: MPC9850/D
Rev 1, 04/2003

Product Preview

Clock Generator for PowerQUICC III

MPC9850

MICROPROCESSOR CLOCK GENERATOR



VF SUFFIX
100 MAP PBGA PACKAGE
CASE 1462

The MPC9850 is a PLL based clock generator specifically designed for Motorola Microprocessor And Microcontroller applications including the PowerQUICC III. This device generates a microprocessor input clock plus the 500 MHz Rapid I/O clock. The microprocessor clock is selectable in output frequency to any of the commonly used microprocessor input and bus frequencies. The Rapid I/O outputs are LVDS compatible. The device offers eight low skew clock outputs organized into two output banks, each configurable to support different clock frequencies. The extended temperature range of the MPC9850 supports telecommunication and networking requirements.

Features

- 8 LVCMOS outputs for processor and other circuitry
- 2 differential LVDS outputs for Rapid I/O interface
- Crystal oscillator or external reference input
- 25 or 33 MHz Input reference frequency
- Selectable output frequencies include = 200, 166, 133,125, 111, 100, 83, 66, 50, 33 or 16 MHz
- Buffered reference clock output
- Rapid I/O (LVDS) Output = 500, 250 or 125 MHz
- Low cycle-to-cycle and period jitter
- 100 lead PBGA package
- 3.3V supply with 3.3V or 2.5V (Bank B) output LVCMOS drive
- Supports computing, networking, telecommunications applications
- Ambient temperature range –40°C to +85°C

Functional Description

The MPC9850 uses either a 25 or 33 MHz reference frequency to generate 8 LVCMOS output clocks, of which, the frequency is selectable from 16 MHz to 200 MHz. The reference is applied to the input of a PLL and multiplied to 2 GHz. Output dividers, divide this frequency by 10, 12, 15, 16, 18, 20, 24, 30, 40, 60 or 120 to produce output frequencies of 200, 166, 133, 125, 111, 100, 83 66 50 33 or 16 MHz. The single-ended LVCMOS outputs are divided into two banks of 4 low skew outputs each, for use in driving a microprocessor or microcontroller clock input as well as other system components. The 2 GHz PLL output frequency is also divided to produce a 125, 250 or 500 MHz clock output for Rapid I/O applications such as found on the PowerQUICC III communications processor. The input reference, either crystal or external input is also buffered to a separate output that my be used as the clock source for a Gigabit Ethernet PHY if desired.

The reference clock may be provided by either an external clock input of 25 MHz or 33 MHz. An internal oscillator requiring a 25 MHz crystal for frequency control may also be used. The external clock source my be applied to either of two clock inputs and selected via the CLK_SEL control input. Both single ended LVCMOS and differential LVPECL inputs are available. The crystal oscillator or external clock input is selected via the input pin of REF_SEL. Other than the crystal, no external components are required for crystal oscillator operation. The REF_33MHz configuration pins is used to select between a 33 and 25 MHz input frequency.

The MPC9850 is packaged in a 100 lead MAPBGA package to optimize both performance and board density.

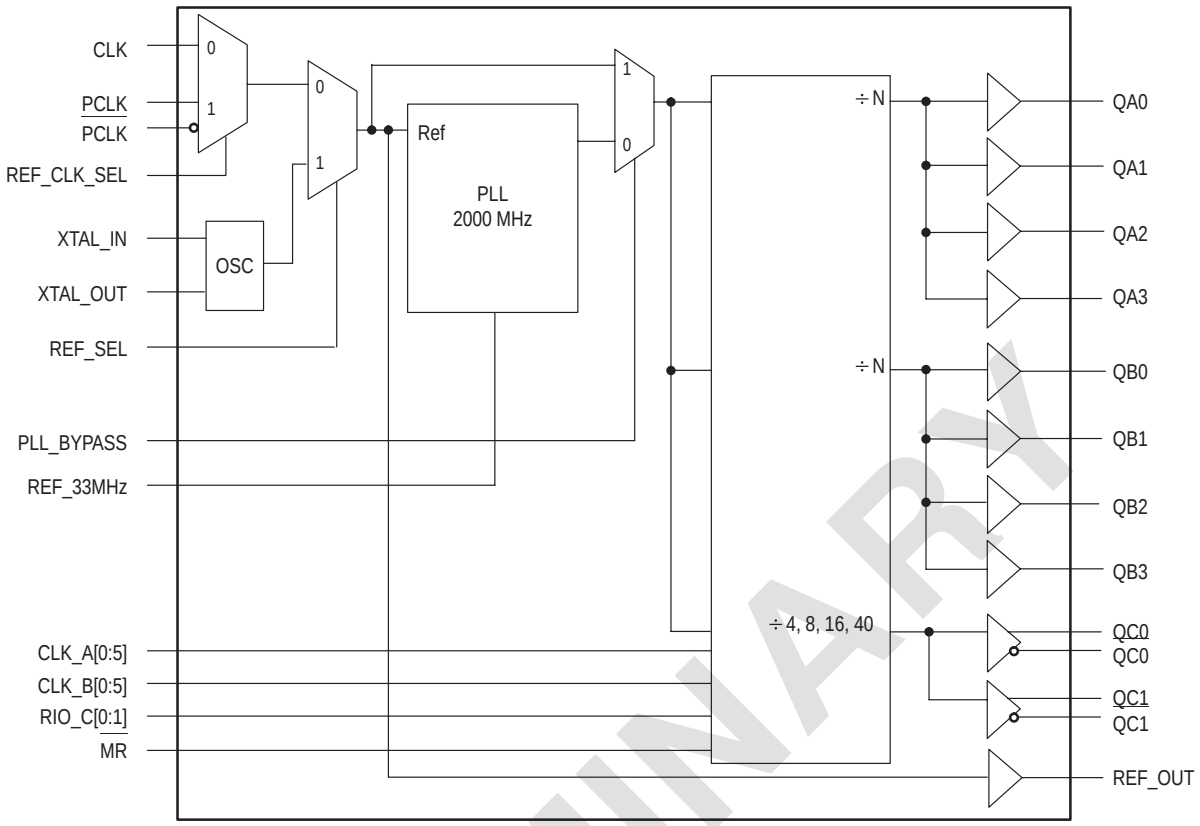


Figure 1. MPC9850 Block Diagram

Table 1. PIN CONFIGURATIONS

Pin	I/O	Type	Function	Supply	Active/State
CLK	Input	LVCMOS	PLL reference clock input (pull–down)	V_{DD}	
PCLK, $\overline{PCLK}$	Input	LVPECL	PLL reference clock input (PCLK – pull–down, PCLK – pull–up and pull–down)	V_{DD}	
QA0, QA1, QA2, QA3	Output	LVCMOS	Bank A Outputs	V_{DDOA}	
QB0, QB1, QB2, QB3	Output	LVCMOS	Bank B Outputs	V_{DD}	
QC0, QC1, $\overline{QC0}$, $\overline{QC1}$	Output	LVDS	Bank C Outputs		
REF_OUT	Output	LVCMOS	Reference Output (25 MHz or 33 MHz)	V_{DD}	
XTAL_IN	Input	LVCMOS	Crystal Oscillator Input Pin	V_{DD}	
XTAL_OUT	Output	LVCMOS	Crystal Oscillator Output Pin	V_{DD}	
REF_CLK_SEL	Input	LVCMOS	Select between CLK and PCLK input (pull–down)	V_{DD}	high
REF_SEL	Input	LVCMOS	Select between External Input and Crystal Oscillator Input (pull–down)	V_{DD}	high
REF_33MHz	Input	LVCMOS	Selects 33MHz input (pull–down)	V_{DD}	high
$\overline{MR}$	Input	LVCMOS	Master Reset (pull–up)	V_{DD}	low
PLL_BYPASS	Input	LVCMOS	Select PLL or static test mode (pull–down)	V_{DD}	high
CLK_A[0:5][a]	Input	LVCMOS	Configures Bank A clock output frequency (pull–up)	V_{DD}	high
CLK_B[0:5][b]	Input	LVCMOS	Configures Bank B clock output frequency (pull–up)	V_{DDOB}	high
RIO_C [0:1]	Input	LVCMOS	Configures Bank C clock output frequency (pull–down)	V_{DD}	
V_{DD}			3.3 V Supply		
V_{DDA}			Analog Supply		
V_{DDOB}			Supply for Output Bank B		
GND			Ground		

a. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)
b. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)
c. PowerPC bit ordering (bit 0 = msb, bit 1 = lsb)

Table 2. FUNCTION TABLE

Control	Default	0	1
REF_CLK_SEL	0	CLK	PCLK
REF_SEL	0	CLK or PCLK	XTAL
PLL_BYPASS	0	Normal	Bypass
REF_33MHz	0	Selects 25MHz Reference	Selects 33MHz Reference
$\overline{MR}$	1	Reset	Normal
CLK_A, CLK_B, and RIO_C control output frequencies. See Table 3 and Table 4 for specific device configuration			

Table 3. OUTPUT CONFIGURATIONS (BANKS A & B)

CLK_x[0:5][a]	CLK_x[0] (msb)	CLK_x[1]	CLK_x[2]	CLK_x[3]	CLK_x[4]	CLK_x[5] (lsb)	N	Frequency (MHz)
111111	1	1	1	1	1	1	126	15.87
111100	1	1	1	1	0	0	120	16.67
101000	1	0	1	0	0	0	80	25.00
011110	0	1	1	1	1	0	60	33.33
010100	0	1	0	1	0	0	40	50.00
001111	0	0	1	1	1	1	30	66.67
001100	0	0	1	1	0	0	24	83.33
001010	0	0	1	0	1	0	20	100.00
001001	0	0	1	0	0	1	18	111.11
001000	0	0	1	0	0	0	16	125.00
000111	0	0	0	1	1	1	15	133.33
000110	0	0	0	1	1	0	12	166.67
000101	0	0	0	1	0	1	10	200.00
000100	0	0	0	1	0	0	8[b]	250

a. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)
b. Minimum value for N

Table 4. OUTPUT CONFIGURATIONS (BANK C)

RIO_C[0:1]	Frequency (MHz)
00	50 (test output)
01	125
10	250
11	500

OPERATION INFORMATION

Output Frequency Configuration

The MPC9850 was designed to provide the commonly used frequencies in PowerQUICC, PowerPC and other microprocessor systems. Table 3 lists the configuration values that will generate those common frequencies. The MPC9850 can generate numerous other frequencies that may be useful in specific applications. The output frequency (fout) of either Bank A or Bank B may be calculated by the following equation.

$$fout = 2000 / N$$

where fout is in MHz and N = 2 * CLK_x[0:5]

This calculation is valid for all values of N from 8 to 126. Note that N = 15 is a modified case of the configuration inputs CLK_x[0:5]. To achieve N = 15 CLK_x[0:5] is configured to 00111 or 7.

Crystal Input Operation

TBD

Power-Up and $\overline{MR}$ Operation

Figure 2 defines the release time and the minumum pulse length for MR pin. The MR release time is based upon the power supply being stable and within V_{DD} specifications. See Table 11 for actual parameter values. The MPC9850 may be configured after release of reset and the outputs will be stable for use after lock indication is obtained.

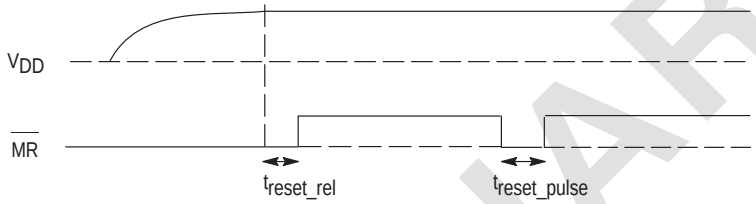


Figure 2. MR operation

Power Supply Bypassing

The MPC9850 is a mixed analog/digital product. The architecture of the MPC9850 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{DD} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

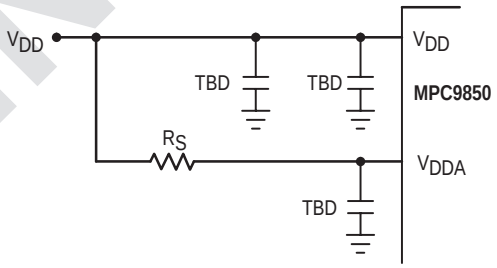


Figure 3. V_{CC} Power Supply Bypass

Table 5. ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage (core)	-0.3	3.8	V	
V_{DDA}	Supply Voltage (Analog Supply Voltage)	-0.3	V_{DD}	V	
V_{DDOB}	Supply Voltage (LVCMOS output for Bank B)	-0.3	V_{DD}	V	
V_{IN}	DC Input Voltage	-0.3	V_{DD}+0.3	V	
V_{OUT}	DC Output Voltage[b]	-0.3	V_{DDx}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

b. V_{DDx} references power supply pin associated with specific output pin.

Table 6. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{DD} \div 2$ $V_{DDOB} \div 2$		V	Bank A output Bank B output
MM	ESD Protection (Machine Model)	TBD			V	
HBM	ESD Protection (Human Body Model)	TBD			V	
CDM	ESD Protection (Charged Device Model)	TBD			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input capacitance		TBD		pF	Inputs
θ_{JC}	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)		TBD		°C/W	
T_A	Ambient Temperature[a]	-40		85	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9850 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9850 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 7. DC CHARACTERISTICS (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for V_{DD}=3.3V±5% and V_{DDOB} = 3.3V±5%						
I_{DD}	Maximum Quiescent Supply Current (Core)		TBD	TBD	mA	V_{DD} pins
I_{DDC}	Maximum Quiescent Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDIN} pins
I_{DDOB}	Maximum Bank B Supply Current		TBD	TBD	mA	V_{DDOB} pins
Supply Current for V_{DD}=3.3V±5% and V_{DDOB} = 2.5V±5%						
I_{DD}	Maximum Quiescent Supply Current (Core)		TBD	TBD	mA	V_{DD} pins
I_{DDC}	Maximum Quiescent Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDIN} pins
I_{DDOB}	Maximum Bank B Supply Current		TBD	TBD	mA	V_{DDOB} pins

Table 8. LVDS DC CHARACTERISTICS (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVDS clock outputs (QC0, $\overline{QC0}$ Cnd QC1, $\overline{QC1}$) for V_{DD}=3.3V±5%						
V_{PP}	Output Differential Voltage[a] (peak-to-peak) (LVDS)	250			mV	
V_{OS}	Output Offset Voltage (LVDS)	1125		1275	mV	

a. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.

Table 9. LVPECL DC CHARACTERISTICS (T_A = –40°C to 85°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVPECL clock inputs (CLK1, $\overline{CLK1}$) for V_{DD}=3.3V±0.5%						
V_{PP}	Differential Voltage[b] (peak-to-peak) (LVPECL)	250			mV	
V_{CMR}	Differential Input Crosspoint Voltage[c] (LVPECL)	1.0		V_{DD} - 0.6	V	

a. AC characteristics are design targets and pending characterization.
b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
c. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

Table 10. LVCMOS I/O DC CHARACTERISTICS (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS for V_{DD}=3.3V±5%						
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[a]			10	µC	V_{IN}=V_{DDL} or GND
LVCMOS for V_{DD}=3.3V±5% and V_{DDOB} = 3.3V±5%						
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 ma
V_{OL}	Output Low Voltage			0.4	V	I_{OL}= 24 ma
Z_{OUT}	Output Impedance		14		Ω	
LVCMOS for V_{DD}=3.3V±5% and V_{DDOB} = 2.5V±5%						
V_{OH}	Output High Voltage	1.9			V	I_{OH}=-15 ma
V_{OL}	Output Low Voltage			0.4	V	I_{OL}= 15 ma
Z_{OUT}	Output Impedance		22		Ω	

a. Inputs have pull-down resistors affecting the input current.

Table 11. AC CHARACTERISTICS (V_{DD}=3.3V±5%, V_{DDOB}=3.3V±5%, T_A= -40°C to +85°C)[a] [b]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Input and output timing specification						
f_{ref}	Input reference frequency (25 MHz input) Input reference frequency (33 MHz input) XTAL Input Input reference frequency in PLL bypass mode[c]	TBD TBD TBD	25 33 25	TBD TBD TBD TBD	MHz MHz MHz	 PLL bypass
f_{VCO}	VCO frequency range[d]		2000		MHz	
f_{MCX}	Output Frequency Bank C output Bank B output Bank C output			TBD TBD TBD	MHz MHz MHz	PLL locked
f_{refPW}	Reference Input Pulse Width	TBD			ps	
f_{refCcc}	Input Frequency Accuracy			100	ppm	
t_r, t_f	Output Rise/Fall Time	TBD		TBD	ns	20% to 80%
DC	Output duty cycle	47.5 45	50 50	52.5 55	%	3.3V operation 2.5V operation
DC_{OSC}	Reference Output for Crystal Input	TBD	50	TBD	%	
PLL specifications						
BW	PLL closed loop bandwidth[e]		TBD		kHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{reset_ref}	MR hold time on power up	TBD			ns	
treset_pulse	MR hold time	TBD			ns	
Skew and jitter specifications						
$t_{sk(O)}$	Output-to-output Skew (within a bank)			50	ps	
$t_{sk(O)}$	Output-to-output Skew (across banks A and B)			100	ps	V_{DDOB} = 3.3V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)[f]			10	ps	
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		TBD		ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)		TBD		ps	
t_r, t_f	Output Rise/Fall Time			TBD	ns	20% to 80%

a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. In bypass mode, the MPC9850 divides the input reference clock.
d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = (f_{VCO} \div M) \cdot N$.
e. -3 dB point of PLL transfer characteristics.
f. See application note AN1934 for a jitter calculation for other confidence factors than 1 σ.

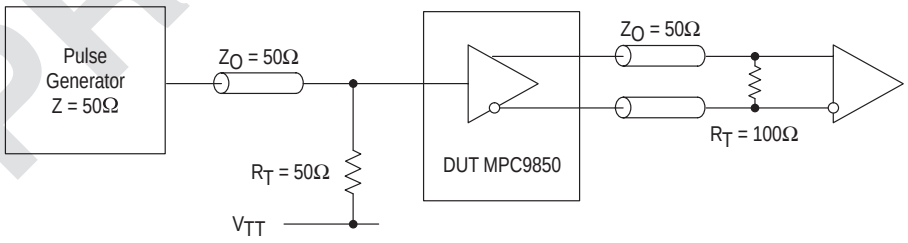


Figure 4. MPC9850 AC test reference (LVDS outputs)

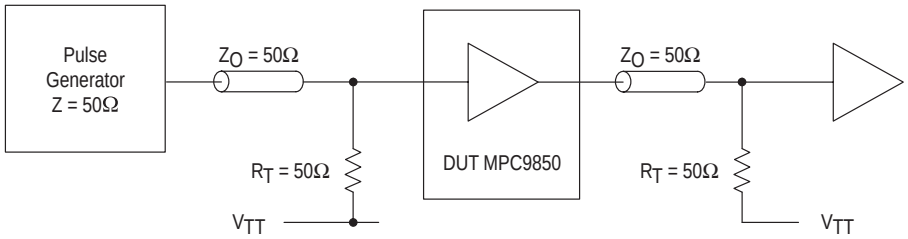


Figure 5. MPC9850 AC test reference (LVCMOS outputs)

Table 12. MPC9850 Pin Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10
A	V_{DDOB}	V_{DDOB}	CLKA[1]	CLKA[3]	CLKA[5]	V_{DD}	QA1	QA2	V_{DDOB}	V_{DDOB}
B	V_{DDOB}	V_{DDOB}	CLKA[0]	CLKA[2]	CLKA[4]	QA0	V_{DD}	QA3	V_{DDOB}	V_{DDOB}
C	RSVD	RSVD	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	REF_OUT
D	V_{DDA}	V_{DDA}	V_{DD}	GND	GND	GND	GND	V_{DD}	$\overline{QC0}$	QC0
E	REF_SEL	CLK	V_{DD}	GND	GND	GND	GND	V_{DD}	V_{DD}	GND
F	PCLK	$\overline{PCLK}$	V_{DD}	GND	GND	GND	GND	V_{DD}	$\overline{QC1}$	QC1
G	REF_CLK_SEL	REF_33MHz	V_{DD}	GND	GND	GND	GND	V_{DD}	PLL_BYPASS	$\overline{MR}$
H	XTAL_IN	XTAL_OUT	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	RIO_C[1]	RIO_C[0]
J	V_{DDOB}	V_{DDOB}	CLKB[0]	CLK[2]	CLK[4]	QB0	V_{DDOB}	QB3	V_{DDOB}	V_{DDOB}
K	V_{DDOB}	V_{DDOB}	CLKB[1]	CLKB[3]	CLKB[5]	V_{DDOB}	QB1	QB2	V_{DDOB}	V_{DDOB}

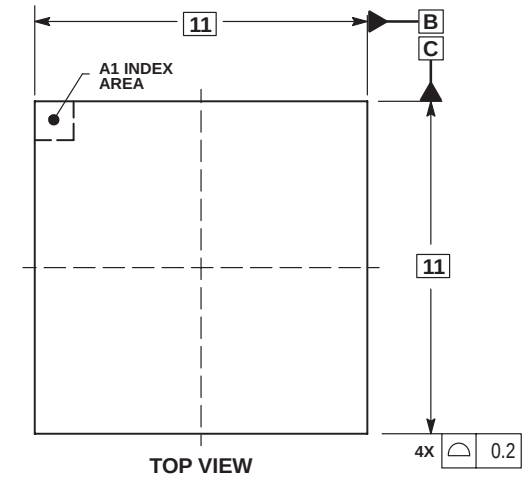
Table 13. MPC9850 Pin List

Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA
V_{DDOB}	A1	RSVD[a]	C1	REF_SEL	E1	REF_CLK_SEL	G1	V_{DDOB}	J1
V_{DDOB}	A2	RSVD[a]	C2	CLK	E2	REF_33MHz	G2	V_{DDOB}	J2
CLKA[1]	A3	V_{DD}	C3	V_{DD}	E3	V_{DD}	G3	CLKB[0]	J3
CLKA[3]	A4	V_{DD}	C4	GND	E4	GND	G4	CLKB[2]	J4
CLKA[5]	A5	V_{DD}	C5	GND	E5	GND	G5	CLKB[4]	J5
V_{DD}	A6	V_{DD}	C6	GND	E6	GND	G6	QB0	J6
QA1	A7	V_{DD}	C7	GND	E7	GND	G7	V_{DDOB}	J7
QA2	A8	V_{DD}	C8	V_{DD}	E8	V_{DD}	G8	QB3	J8
V_{DDOB}	A9	V_{DD}	C9	V_{DD}	E9	PLL_BYPASS	G9	V_{DDOB}	J9
V_{DDOB}	A10	REF_OUT	C10	GND	E10	$\overline{MR}$	G10	V_{DDOB}	J10
V_{DDOB}	B1	V_{DDA}	D1	PCLK	F1	XTAL_IN	H1	V_{DDOB}	K1
V_{DDOB}	B2	V_{DDA}	D2	$\overline{PCLK}$	F2	XTAL_OUT	H2	V_{DDOB}	K2
CLKA[0]	B3	V_{DD}	D3	V_{DD}	F3	V_{DD}	H3	CLKB[1]	K3
CLKA[2]	B4	GND	D4	GND	F4	V_{DD}	H4	CLKB[3]	K4
CLKA[4]	B5	GND	D5	GND	F5	V_{DD}	H5	CLKB[5]	K5
QA0	B6	GND	D6	GND	F6	V_{DD}	H6	V_{DDOB}	K6
V_{DD}	B7	GND	D7	GND	F7	V_{DD}	H7	QB1	K7
QA3	B8	V_{DD}	D8	V_{DD}	F8	V_{DD}	H8	QB2	K8
V_{DDOB}	B9	$\overline{QC0}$	D9	$\overline{QC1}$	F9	RIO_C[1]	H9	V_{DDOB}	K9
V_{DDOB}	B10	QC0	D10	QC1	F10	RIO_C[0]	H10	V_{DDOB}	K10

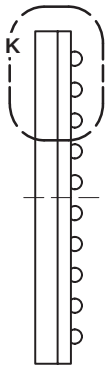
a. RSVD pins must be left open.

OUTLINE DIMENSIONS

VF SUFFIX
100 MAP PBGA PACKAGE
CASE 1462-01
ISSUE O

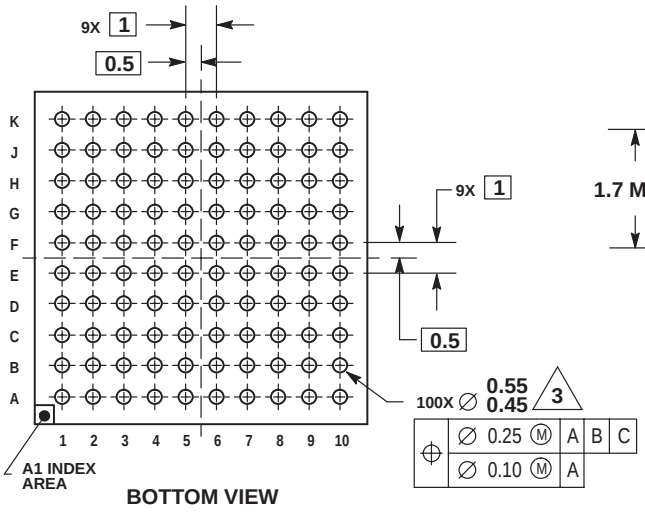


TOP VIEW

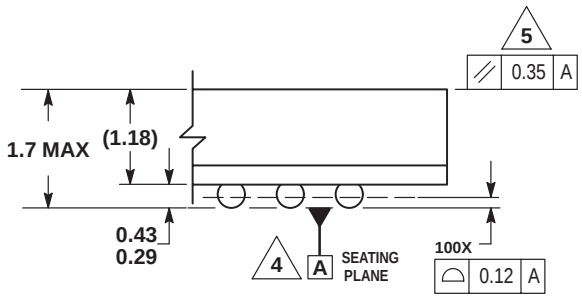


SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGING



BOTTOM VIEW



DETAIL K
ROTATED 90 °CLOCKWISE

NOTES

NOTES

HOW TO REACH US:

USA / EUROPE / LOCATIONS NOT LISTED:

TECHNICAL INFORMATION CENTER:
1–800–521–6274 or 480–768–2130

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center,
3–20–1, Minami–Azabu, Minato–ku, Tokyo 106–8573 Japan
81–3–3440–3569

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
852–26668334

HOME PAGE: http://motorola.com/semiconductors