Advance Information

MPC8245RZUPNS/D
Rev. 0, 3/2002

MPC8245 Part Number Specification for the XPC8245RZUnnnx Series

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Motorola Part Numbers Affected:

XPC8245RZU400B

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC8245 Integrated Processor Hardware Specifications* (order # MPC8245EC/D).

Specifications provided in this document supersede those in the *MPC8245 Integrated Processor Hardware Specifications*, Rev.0.5 or later, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to http://www.motorola.com/semiconductors or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table A. For more detailed ordering information see Section 1.9, “Ordering Information.”

Table A. Part Numbers Addressed by this Data Sheet

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	V_{DD}	T_J (°C)	
XPC8245RZU400B	400 MHz	2.1 ± 100 mV	0 to 85	Modified voltage and temperature Specifications to achieve 400 MHz

Note: The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.2 Features

This section summarizes changes to the features of the MPC8245 described in the *MPC8245 Integrated Processor Hardware Specifications*.

- Power management
  - — 2.1-V processor core

1.3 General Parameters

This section summarizes changes to the general parameters of the MPC8245 described in the *MPC8245 Integrated Processor Hardware Specifications*.

- Core power supply 2.1 V ± 100 mV DC nominal

1.4.1.2 DC Electrical Characteristics

Table 2 provides the recommended operating conditions for the MPC8245 part numbers described herein.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit
Supply voltage	V_{DD}	2.1 V ± 100 mV	V
CPU PLL supply voltage	AV_{DD}	2.1 V ± 100 mV	V
PLL supply voltage - Peripheral Logic	AV_{DD2}	2.1 V ± 100 mV	V
Die-junction temperature	T_j	0 to 85	°C

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

1.4.1.5 Power Characteristics

The AC electrical characteristics and AC timing for all parts described herein are unaffected and comply with the *MPC8245 Integrated Processor Hardware Specifications*.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock / Memory Bus Clock CPU Clock Frequency (MHz)		Units	Notes
	33/ 132/ 396	40/ 100/ 400		
Typical	2.2	2.3	W	1, 5
Max - FP	2.8	2.9	W	1, 2
Max - INT	2.4	2.5	W	1, 3
Doze	1.6	1.7	W	1, 4, 6
Nap	0.6	0.7	W	1, 4, 6
Sleep	0.2	0.4	W	1, 4, 6
I/O Power Supplies[10]				
Mode	**Range**		**Units**	**Notes**
Typ-OVdd	200 - 500	200 - 500	mW	7,8
Typ-GVdd	300 - 700	300 - 700	mW	7,9

Notes:

1. The values include Vdd, AVdd, and AVdd2 but do not include I/O Supply Power, see Section 1.7.2, “Power Supply Sizing,” for information on OVdd and GVdd supply power. Values shown in parenthesis () indicate power consumption at Vdd/AVdd/AVdd2 = 2.1 V.
2. Maximum - FP power is measured at Vdd = 2.1 V with dynamic power management enabled while running an entirely cache-resident, looping, floating point multiplication instruction.
3. Maximum - INT power is measured at Vdd = 2.1 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at Vdd = 2.1 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at Vdd = AVdd = 2.1 V, OVdd = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeroes on 64 bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. The typical minimum I/O power values were results of the MPC8245 performing cache resident integer operations at the slowest frequency combination of 33:66:200 (PCI:Mem:CPU) MHz.
8. The typical maximum OVdd value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes to PCI memory.
9. The typical maximum GVdd value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes on 64 bit boundaries to local memory.
10. Power consumption of PLL supply pins (AVdd and AVdd2) < 15 mW. Guaranteed by design and is not tested.

1.6 PLL Configuration

The MPC8245 internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the Peripheral Logic/Memory Bus PLL (VCO) frequency of operation for the PCI-to-Memory frequency multiplying and the 603e CPU PLL (VCO) frequency of operation for Memory-to-CPU frequency multiplying. The PLL configurations for the MPC8245 is shown in Table 1.

Table 1. MPC8245 PLL Configurations for the 400 MHz Part Offering

Ref	PLL_CFG [0:4][10,13]	400 MHz Part[9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range[1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
0	00000[12]	25 - 44[2]	75 - 132	188 - 330	3 (2)	2.5 (2)
1	00001[12]	25 - 44[5]	75 - 132	225 - 396	3 (2)	3 (2)
2	00010[11]	50[17] - 66[1]	50 - 66	225 - 297	1 (4)	4.5 (2)
3	00011[11,14]	50[16] - 66[1]	50 - 66	100 - 133	1(Bypass)	2 (4)
4	00100[12]	25 - 46[4]	50 - 92	100 - 184	2 (4)	2 (4)
6	00110[15]	Bypass			Bypass	Bypass
7	00111[14]	60[6] - 66[1]	60 - 66	180 - 198	1(Bypass)	3 (2)
8	01000[12]	60[6] - 66[1]	60 - 66	180 - 198	1 (4)	3 (2)
9	01001[18]	45[6] - 66[1]	90 - 132	180 - 264	2 (2)	2 (2)
A	01010[12]	25 - 44[5]	50 - 88	225 - 396	2 (4)	4.5 (2)
B	01011[18]	45[3] - 66[1]	68 - 99	204 - 297	1.5 (2)	3 (2)
C	01100[12]	36[6] - 46[4]	72 - 92	180 - 230	2 (4)	2.5 (2)
D	01101[18]	45[3] - 66[1]	68 - 99	238 - 347	1.5 (2)	3.5 (2)
E	01110[12]	30[6] - 46[4]	60 - 92	180 - 276	2 (4)	3 (2)
F	01111[18]	25 - 38[5]	75 - 114	263 - 399	3(2)	3.5(2)
10	10000[12]	30[6] - 44[2]	60 - 132	180 - 264	3 (2)	2 (2)
11	10001[18]	25 - 33[2]	100 - 132	250 - 330	4(2)	2.5(2)
12	10010[12]	60[6] - 66[1]	90 - 99	180 - 198	1.5 (2)	2 (2)
13	10011[18]	25 - 33[5]	100 - 132	300 - 396	4(2)	3(2)
14	10100[12]	26[6] - 47[4]	52 - 94	182 - 329	2 (4)	3.5 (2)
15	10101[18]	27[3] - 40[5]	68 - 100	272 - 400	2.5 (2)	4 (2)
16	10110[12]	25 - 46[4]	50 - 92	200 - 368	2 (4)	4 (2)

Table 1. MPC8245 PLL Configurations for the 400 MHz Part Offering (Continued)

Ref	PLL_ CFG [0:4][10,13]	400 MHz Part[9]			Multipliers	
		PCI Clock Input (PCI_ SYNC_IN) Range[1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
17	10111[18]	25 - 33[2]	100 - 132	200 - 264	4 (2)	2 (2)
18	11000[12]	27[3] - 53[5]	68 - 132	204 - 396	2.5 (2)	3 (2)
19	11001[18]	36[6] - 66[1]	72 - 132	180 - 330	2 (2)	2.5 (2)
1A	11010[12]	50[17] - 66[1]	50 - 66	200 - 264	1 (4)	4 (2)
1B	11011[18]	33[6] - 66[1]	66 - 132	198 - 396	2 (2)	3 (2)
1C	11100[12]	44[6] - 66[1]	66 - 99	198 - 297	1.5 (2)	3 (2)
1D	11101[12]	48[6] - 66[1]	72 - 99	180 - 248	1.5 (2)	2.5(2)
1E	11110[8]	Not Usable			Off	Off
1F	11111[8]	Not Usable			Off	Off

Notes:
1. Limited by maximum PCI input frequency (66 MHz).
2. Limited by maximum system memory interface operating frequency (133 MHz).
3. Limited by minimum memory VCO frequency. (133 MHz)
4. Limited due to maximum memory VCO frequency. (372 MHz)
5. Limited by maximum CPU operating frequency. (400 MHz)
6. Limited by minimum CPU VCO frequency. (360 MHz)
7. Limited by maximum CPU VCO frequency. (800)
8. In Clock Off mode, no clocking occurs inside the MPC8245 regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings not listed (01011, 01101, 01111, 10001, 10011, 10101, 11001, and 11011) are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting are different from the MPC8240 and are not backwards compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting is different from the MPC8240 and may not be fully backwards compatible.
13. Bits 7– 4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL Bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL Bypass mode.
15. In Dual PLL Bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in Dual PLL Bypass mode.
16. Limited by minimum CPU operating frequency.(100 MHz)
17. Limited by minimum memory bus frequency. (50 MHz)

18. PCI_SYNC_IN range for this PLL_CFG[0:4] setting does not exist on the MPC8240 and may not be fully backwards compatible.

1.9 Ordering Information

This section provides the part numbering nomenclature for the MPC8245. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office.

Figure provides the Motorola part numbering nomenclature for the MPC8245. In addition to the processor frequency, the part numbering scheme also consists of an application modifier. The application modifier may specify special application conditions such as specific temperature or voltage ranges. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

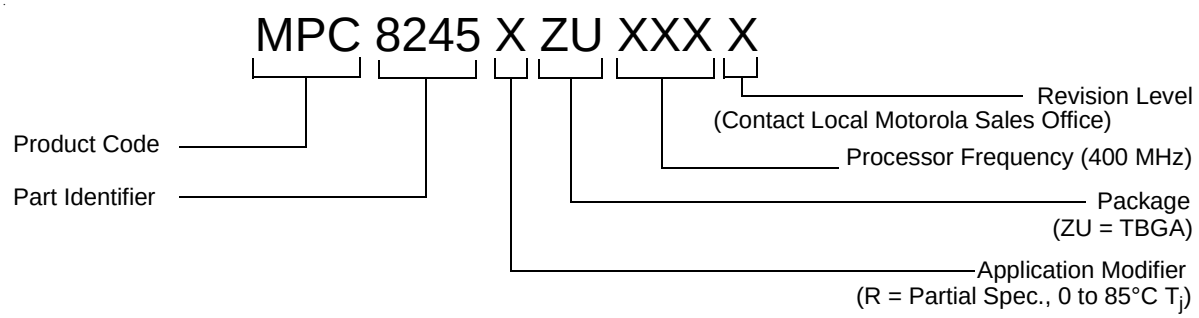

Figure 33. Motorola Part Number Key

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