MN838850

Source Driver for LCD Panel Drive

■ Overview

The MN838850 converts digital display data from a personal computer or an engineering workstation to analog signal voltages to allow those signals to be displayed on a color TFT LCD panel.

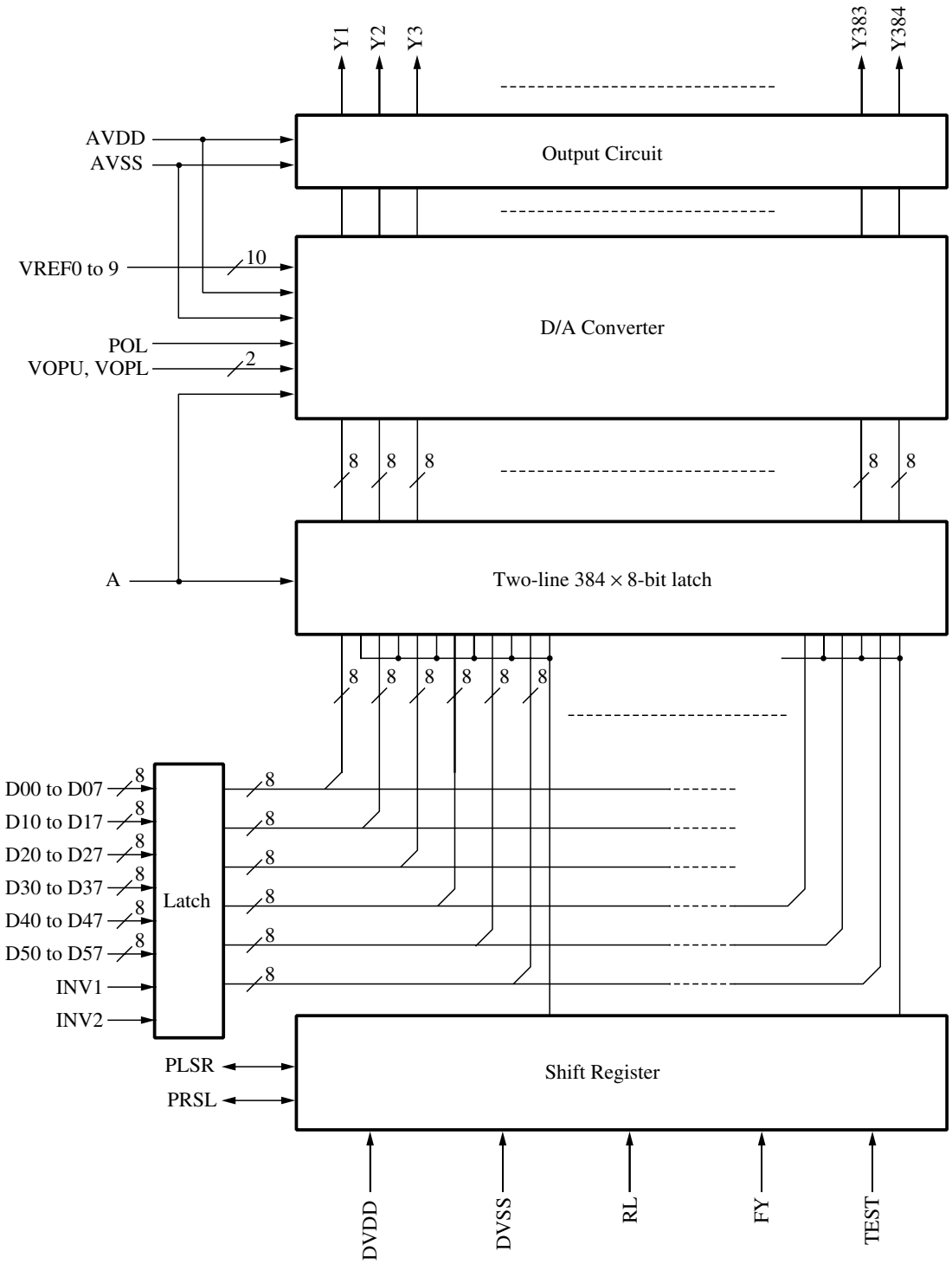
■ Features

- Includes a built-in D/A converter and accepts 8-bit digital input data for 16.7-million color display.
- Output dynamic range: 14.6 V_{P-P} (when AVDD = 15 V)
- Supports both dot inversion drive and source inversion drive schemes.
- Number of drive outputs: 384
- Input data bus: acquires two pixels at the same time
- Supports control of data inversion at each clock cycle.
- Supports γ correction.
- Adopts a drive scheme that does not require precharging.
- Allows serial cascade connection.
- The clock is automatically stopped after the acquisition of a fixed amount of data.
- The shift register shift direction can be set to be either left-to-right or right-to-left.
- Digital circuit block features low-voltage operation:
  2.7 to 3.6 V
- Maximum operating clock frequency:
  50 MHz (3.1 to 3.6 V), 40 MHz (2.7 to 3.6 V)

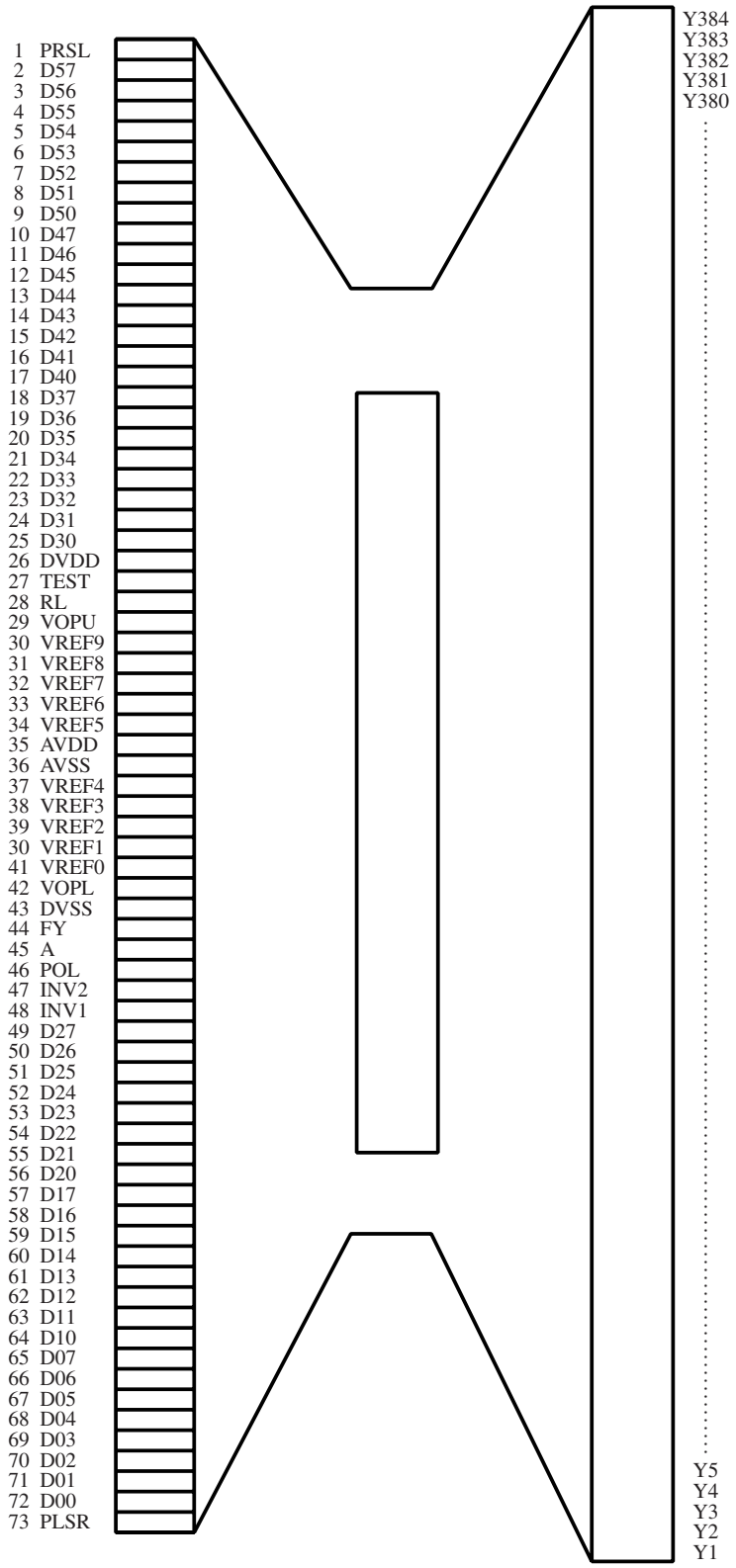
■ Applications

- TFT LCD panels

■ Block Diagram



■ Pin Arrangement



Cu Foil Surface Top View

■ Pin Descriptions

<table>
<tr><th>Pin No.</th><th>I/O</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>D00 to D07
D10 to D17
D20 to D27
D30 to D37
D40 to D47
D50 to D57</td><td>I</td><td>Image data input</td><td>Image data input pins.
The R, G, and B image signals are input using these pins.
D07, D17, D27, D37, D47, D57 : MSB
D00, D10, D20, D30, D40, D50 : LSB</td></tr>
<tr><td>Y1 to Y384</td><td>O</td><td>Image signal output</td><td>Analog image signal output pins.</td></tr>
<tr><td>PLSR
PRSL</td><td>I/O</td><td>Start pulse input and output</td><td>Internal shift register start pulse input and output pins.
<table>
<tr><th></th><th>RL = "H"</th><th>RL = "L"</th></tr>
<tr><td>PLSR</td><td>Right shift input</td><td>Left shift output</td></tr>
<tr><td>PRSL</td><td>Right shift output</td><td>Left shift input</td></tr>
</table></td></tr>
<tr><td>RL</td><td>I</td><td>Shift direction selection signal input</td><td>Input signal that selects the shift direction.
High: Right shift (Y1 to Y384)
Low: Left shift (Y384 to Y1)</td></tr>
<tr><td>FY</td><td>I</td><td>Clock input</td><td>Data acquisition clock input pin.</td></tr>
<tr><td>A</td><td>I</td><td>Analog output control</td><td>Controls the analog voltage output.</td></tr>
<tr><td>POL</td><td>I</td><td>Output polarity reversal control input</td><td>Switches the reference voltage for odd and even outputs.</td></tr>
<tr><td>INV1
INV2</td><td>I</td><td>Data inversion control input</td><td>Controls inversion of the input image signal.
INV1: Used for D2(7 : 0), D1(7 : 0), D0(7 : 0)
INV2: Used for D5(7 : 0), D4(7 : 0), D3(7 : 0)</td></tr>
<tr><td>VREF0 to 9</td><td>I</td><td>γ correction voltage input</td><td>Inputs the γ correction voltage used by the D/A converter.</td></tr>
<tr><td>VOPU, VOPL</td><td>I</td><td>Analog reference voltage</td><td>Provides the reference voltage that determines the analog circuit operating point.
VOPU: Reference voltage for the high side output
VOPL : Reference voltage for the low side output</td></tr>
<tr><td>AVDD
AVSS</td><td>I</td><td>Analog system power supply</td><td>Provides the power for the analog circuits.</td></tr>
<tr><td>DVDD
DVSS</td><td>I</td><td>Digital system power supply</td><td>Provides the power for the digital circuits.</td></tr>
<tr><td>TEST</td><td>I</td><td>Test
(Pull-down resistor: 100 kΩ)</td><td>Used for device testing.
This pin must be left open during normal operation.</td></tr>
</table>

■ Functional Description

• Relationship between the data input and the analog output pins

The input mode used by this IC is a two-pixel mode in which the data for two pixels is input in parallel from the D0(7:0), D1(7:0), D2(7:0), D3(7:0), D4(7:0), and D5(7:0) input ports.

The correspondence between the data input ports and the output pins is as follows.

Y(6n−5) = D00 to D07　　Y(6n−2) = D30 to D37
Y(6n−4) = D10 to D17　　Y(6n−1) = D40 to D47
Y(6n−3) = D20 to D27　　Y(6n) = D50 to D57　(n = 1, 2, ·····, 64)

Figure 1 shows an example of color data and pin connections when RL is high.

This example shows the case where the pixels are in the order R, B, G starting at the left edge of the LCD panel.

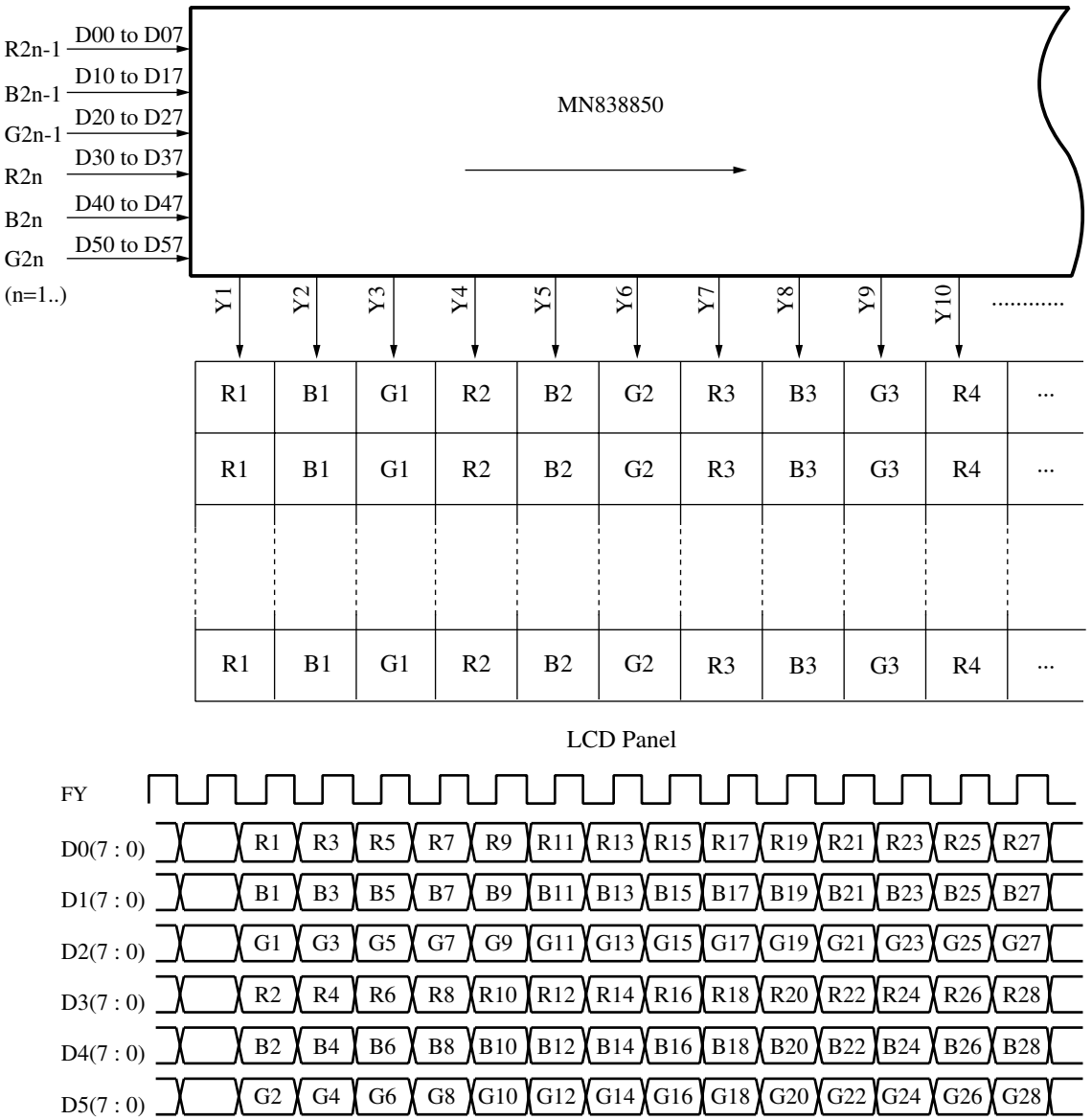


Figure 1　Relationship between Input and Output Pins (When RL is high and the shift direction is Y1 to Y384)

■ Functional Description (continued)

• Relationship between the data input and the analog output pins (continued)

The following presents the case with the same LCD panel color arrangement as figure 1 but with RL low.

In figure 2, R1 corresponds to Y384, B1 to Y383, and G1 to Y382. Note that the relationship between the color data and the data ports here differs from that in figure 1.

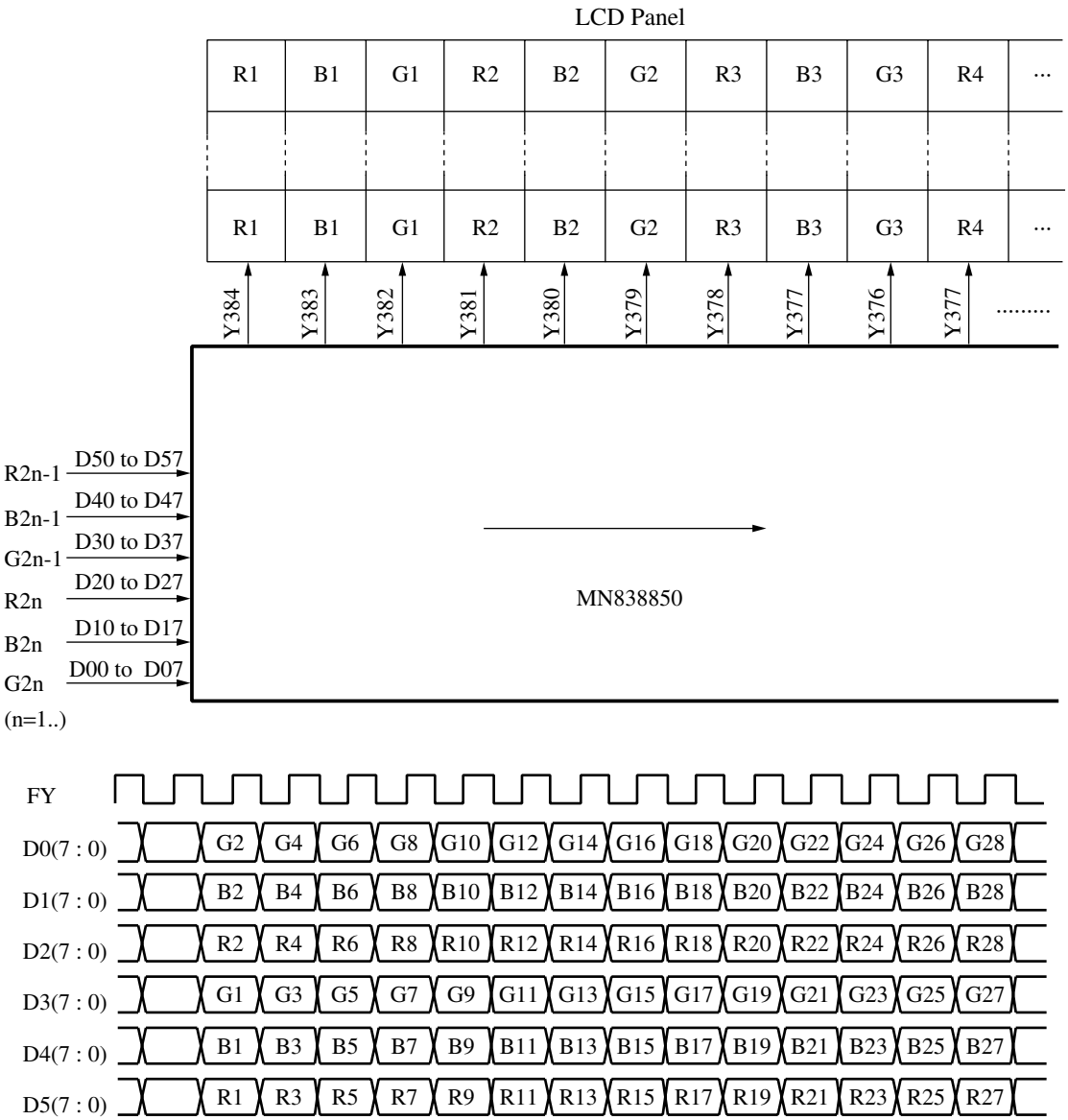


Figure 2 Relationship between Input and Output Pins (When RL is low and the shift direction is Y384 to Y1)

■ Functional Description (continued)

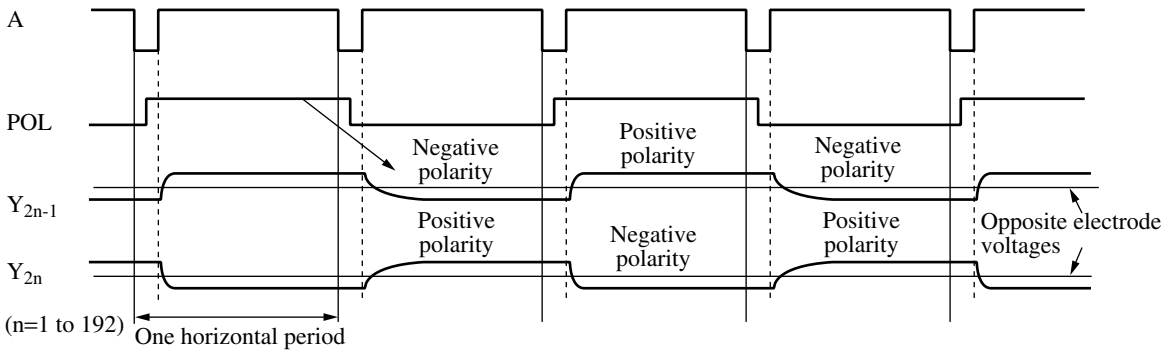
• Dot inversion drive

Since dot inversion drive is used, the analog output voltages with respect to the opposite electrode voltage differ in polarity for each of the odd and even numbered output pins. This output voltage polarity is controlled by POL. The table below lists the correspondence between the POL polarity setting, the analog output polarity and the VREF used.

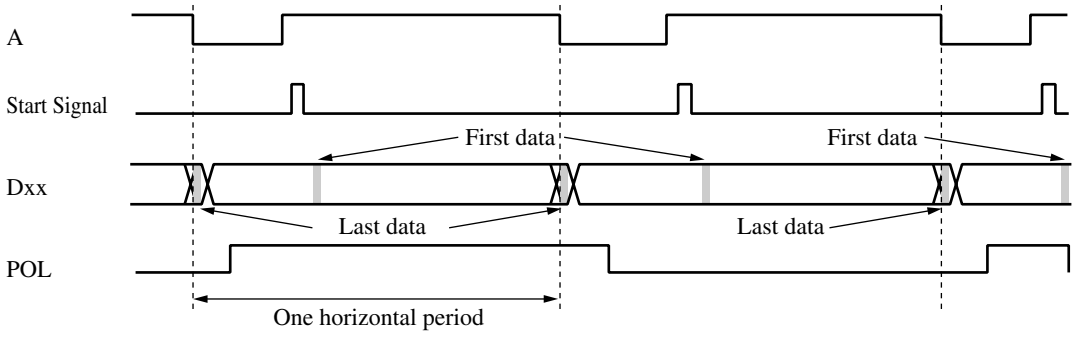
POL	Y2n-1	Y2n
"L"	Positive polarity VREF9 to 5	Negative polarity VREF4 to 0
"H"	Negative polarity VREF4 to 0	Positive polarity VREF9 to 5

The POL switching timing is presented below.

POL should be switched during the period when A is low, after the last data has been input, and before the next start signal has been input. The POL signal level is acquired by the device internally on the falling edge of the A signal. The output polarity is determined by the acquired signal level.



POL Switching Timing



Details of the POL Switching Timing

■ Functional Description (continued)

• Dot inversion drive (continued)

Next we describe dot inversion drive operation.

The symbol "+" here means a voltage that is positive with respect to the voltage on the opposite electrode, and "−" means a voltage that is negative with respect to the voltage on the opposite electrode.

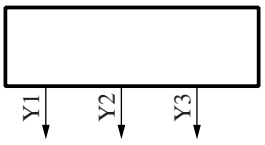
The figure below shows the dot inversion drive operation.

Since POL is low in the first line of the first field, Y1 will be + and Y2 will be −, that is, odd-numbered output pins will have positive polarity and even-numbered output pins will have negative polarity.

Since POL is switched to high for the second line, odd-numbered output pins will have negative polarity and even-numbered output pins will have positive polarity.

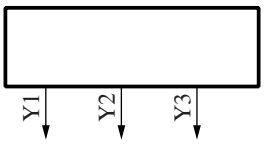
Thereafter, the polarity of the output voltages is determined by the POL polarity.

In the second field, the POL polarity will be the opposite of what it was for the first field, so the output voltage polarities will be reversed.



		Y1	Y2	Y3	POL
Field 1	Line 1	+	−	+	"L"
	Line 2	−	+	−	"H"
	Line 3	+	−	+	"L"
	Line 4	−	+	−	"H"
	⋮	⋮	⋮	⋮	
Field 2	Line 1	−	+	−	"H"
	Line 2	+	−	+	"L"
	Line 3	−	+	−	"H"

Note that if POL is inverted not every line, but only every field, the output polarities will be as shown below.



		Y1	Y2	Y3	POL
Field 1	Line 1	+	−	+	"L"
	Line 2	+	−	+	"L"
	Line 3	+	−	+	"L"
	⋮	⋮	⋮	⋮	
Field 2	Line 1	−	+	−	"H"
	Line 2	−	+	−	"H"
	Line 3	−	+	−	"H"

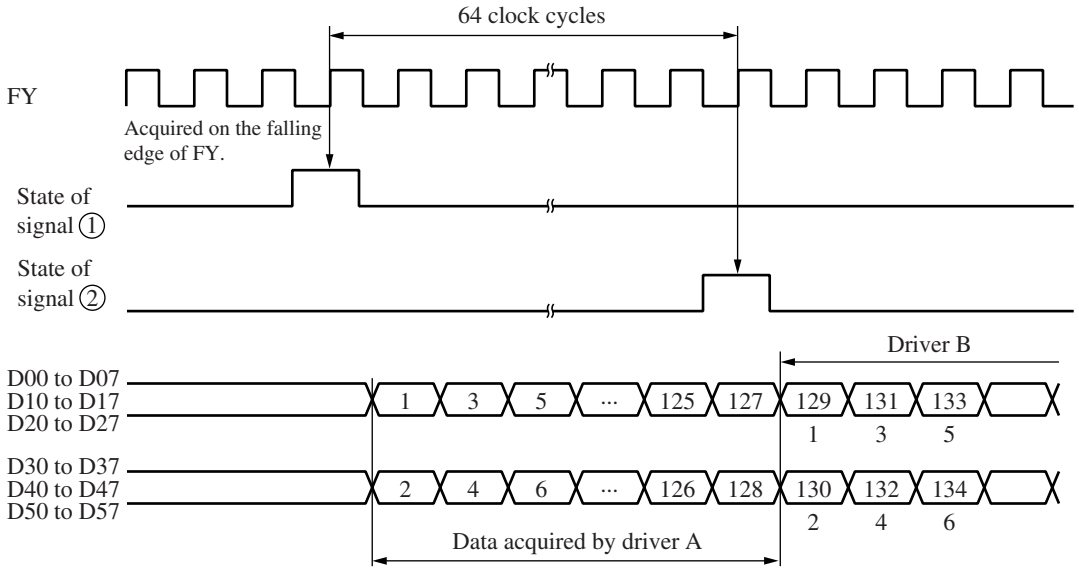
■ Functional Description (continued)

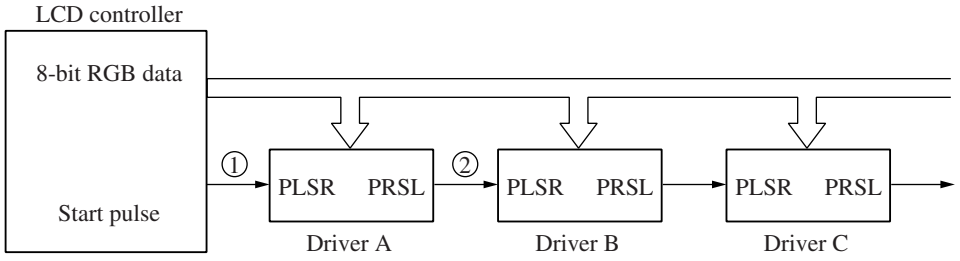
• Operation when Connected in Cascade

When RL is high:

Driver A acquires the PLSR start pulse on the rising edge of FY and starts acquiring data on the next FY rising edge. The PRSL (carry) output will go high 64 clock pulses after the start pulse input and data acquisition will stop one clock cycle later.

Driver B receives the driver A PRSL rising edge and starts accepting data one clock cycle later.

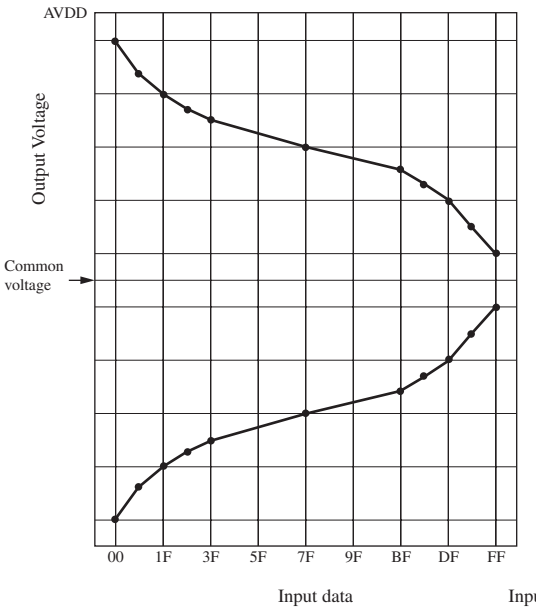




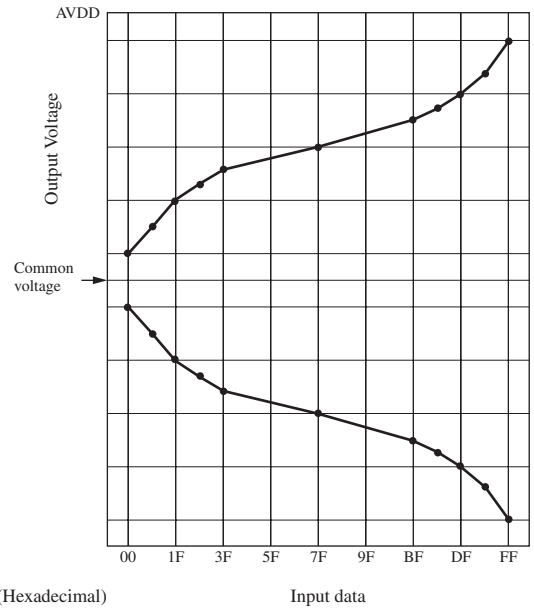
■ Functional Description (continued)

• Relationship between input data values and output voltages

The IC outputs voltages with discrete values and differing polarities for the odd and even output pins with respect to the common electrode. The output voltage is determined by the input data value, the γ correction voltages (VREF0 to VREF9), VOPL, VOPU, and POL.



Relationship between Input Data and Output Voltage
(VREF0 > VREF1 > VREF2 > VREF3 > VREF4,
VREF5 > VREF6 > VREF7 > VREF8 > VREF9)



Input data (Hexadecimal)

Relationship between Input Data and Output Voltage
(VREF0 < VREF1 < VREF2 < VREF3 < VREF4,
VREF5 < VREF6 < VREF7 < VREF8 < VREF9)

■ Functional Description (continued)

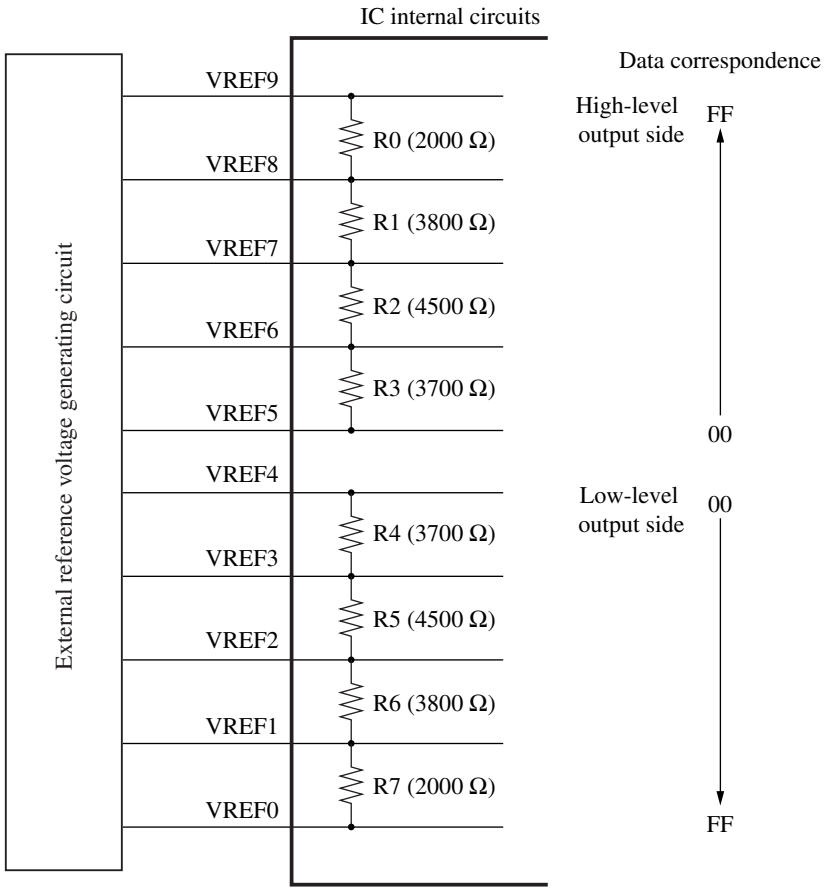
• Relationship between input data values and output voltages (continued)

Apply the voltages for the γ correction to the pins VREF0 to VREF9.

The γ correction voltage input pins are divided into two groups: the high-level output control group and the low-level output control group, and each group is connected in series with resistors. Each of these resistor series has a total typical value of 14 kΩ.

This structure is shown in the figure. The typical values of the resistors are shown in parentheses.

Note that since these voltages are resistor divided internally, the voltages applied to the VREF pins should be applied through a low-impedance circuit. If the voltages are directly applied by the resistor divider, the desired output voltages may not result.



■ Functional Description (continued)

• Table 1 Relationship between VREF Voltages and Analog Output Voltages (High-level side) (Values are examples)
VREF5 = 9.200, VREF6 = 10.635, VREF7 = 12.380, VREF8 = 13.854, VREF9 = 14.630, VOPU = 11.250

Display data	Logical expression	Voltage level	Voltage level difference
00	VOPU × 63/31– (42 × VREF8+1238 × VREF9) /1240	7.787	0.026
01	VOPU × 63/31– (84 × VREF8+1196 × VREF9) /1240	7.813	0.026
02	VOPU × 63/31– (126 × VREF8+1154 × VREF9) /1240	7.839	0.026
⋮			
0D	VOPU × 63/31– (588 × VREF8+692 × VREF9) /1240	8.128	0.026
0E	VOPU × 63/31– (630 × VREF8+650 × VREF9) /1240	8.155	0.026
0F	VOPU × 63/31– (672 × VREF8+608 × VREF9) /1240	8.181	0.023
10	VOPU × 63/31– (710 × VREF8+570 × VREF9) /1240	8.205	0.023
11	VOPU × 63/31– (748 × VREF8+532 × VREF9) /1240	8.228	0.023
12	VOPU × 63/31– (786 × VREF8+494 × VREF9) /1240	8.252	0.023
⋮			
1D	VOPU × 63/31– (1204 × VREF8+76 × VREF9) /1240	8.514	0.023
1E	VOPU × 63/31– (1242 × VREF8+38 × VREF9) /1240	8.537	0.023
1F	VOPU × 63/31– (1280 × VREF8+0 × VREF9) /1240	8.561	0.020
20	VOPU × 63/31– (32 × VREF7+2400 × VREF8) /2356	8.581	0.020
21	VOPU × 63/31– (64 × VREF7+2368 × VREF8) /2356	8.601	0.020
22	VOPU × 63/31– (96 × VREF7+2336 × VREF8) /2356	8.621	0.020
⋮			
2D	VOPU × 63/31– (448 × VREF7+1984 × VREF8) /2356	8.841	0.020
2E	VOPU × 63/31– (480 × VREF7+1952 × VREF8) /2356	8.861	0.020
2F	VOPU × 63/31– (512 × VREF7+1920 × VREF8) /2356	8.882	0.016
30	VOPU × 63/31– (538 × VREF7+1894 × VREF8) /2356	8.898	0.016
31	VOPU × 63/31– (564 × VREF7+1868 × VREF8) /2356	8.914	0.016
32	VOPU × 63/31– (590 × VREF7+1842 × VREF8) /2356	8.930	0.016
⋮			
3D	VOPU × 63/31– (876 × VREF7+1556 × VREF8) /2356	9.109	0.016
3E	VOPU × 63/31– (902 × VREF7+1530 × VREF8) /2356	9.125	0.016
3F	VOPU × 63/31– (928 × VREF7+1504 × VREF8) /2356	9.142	0.015
40	VOPU × 63/31– (953 × VREF7+1479 × VREF8) /2356	9.157	0.015
41	VOPU × 63/31– (978 × VREF7+1454 × VREF8) /2356	9.173	0.015
42	VOPU × 63/31– (1003 × VREF7+1429 × VREF8) /2356	9.189	0.015
⋮			
4D	VOPU × 63/31– (1278 × VREF7+1154 × VREF8) /2356	9.361	0.015
4E	VOPU × 63/31– (1303 × VREF7+1129 × VREF8) /2356	9.376	0.015
4F	VOPU × 63/31– (1328 × VREF7+1104 × VREF8) /2356	9.392	0.015

■ Functional Description (continued)

• Table 1 (continued) Relationship between VREF Voltages and Analog Output Voltages (High-level side) (Values are examples)
VREF5 = 9.200, VREF6 = 10.635, VREF7 = 12.380, VREF8 = 13.854, VREF9 = 14.630, VOPU = 11.250

Display data	Logical expression	Voltage level	Voltage level difference
50	VOPU × 63/31– (1353 × VREF7+1079 × VREF8) /2356	9.408	0.015
51	VOPU × 63/31– (1378 × VREF7+1054 × VREF8) /2356	9.423	0.015
52	VOPU × 63/31– (1403 × VREF7+1029 × VREF8) /2356	9.439	0.015
⋮			
5D	VOPU × 63/31– (1678 × VREF7+754 × VREF8) /2356	9.611	0.015
5E	VOPU × 63/31– (1703 × VREF7+729 × VREF8) /2356	9.627	0.015
5F	VOPU × 63/31– (1728 × VREF7+704 × VREF8) /2356	9.642	0.013
60	VOPU × 63/31– (1750 × VREF7+682 × VREF8) /2356	9.656	0.013
61	VOPU × 63/31– (1772 × VREF7+660 × VREF8) /2356	9.670	0.013
62	VOPU × 63/31– (1794 × VREF7+638 × VREF8) /2356	9.683	0.013
⋮			
6D	VOPU × 63/31– (2036 × VREF7+396 × VREF8) /2356	9.835	0.013
6E	VOPU × 63/31– (2058 × VREF7+374 × VREF8) /2356	9.849	0.013
6F	VOPU × 63/31– (2080 × VREF7+352 × VREF8) /2356	9.862	0.013
70	VOPU × 63/31– (2102 × VREF7+330 × VREF8) /2356	9.876	0.013
71	VOPU × 63/31– (2124 × VREF7+308 × VREF8) /2356	9.890	0.013
72	VOPU × 63/31– (2146 × VREF7+286 × VREF8) /2356	9.904	0.013
⋮			
7D	VOPU × 63/31– (2388 × VREF7+44 × VREF8) /2356	10.055	0.013
7E	VOPU × 63/31– (2410 × VREF7+22 × VREF8) /2356	10.069	0.013
7F	VOPU × 63/31– (2432 × VREF7+0 × VREF8) /2356	10.083	0.013
80	VOPU × 63/31– (11 × VREF6+1429 × VREF7) /1395	10.096	0.013
81	VOPU × 63/31– (22 × VREF6+1418 × VREF7) /1395	10.110	0.013
82	VOPU × 63/31– (33 × VREF6+1407 × VREF7) /1395	10.124	0.013
⋮			
8D	VOPU × 63/31– (154 × VREF6+1286 × VREF7) /1395	10.275	0.013
8E	VOPU × 63/31– (165 × VREF6+1275 × VREF7) /1395	10.289	0.013
8F	VOPU × 63/31– (176 × VREF6+1264 × VREF7) /1395	10.303	0.013
90	VOPU × 63/31– (187 × VREF6+1253 × VREF7) /1395	10.317	0.013
91	VOPU × 63/31– (198 × VREF6+1242 × VREF7) /1395	10.330	0.013
92	VOPU × 63/31– (209 × VREF6+1231 × VREF7) /1395	10.344	0.013
⋮			
9D	VOPU × 63/31– (330 × VREF6+1110 × VREF7) /1395	10.495	0.013
9E	VOPU × 63/31– (341 × VREF6+1099 × VREF7) /1395	10.509	0.013
9F	VOPU × 63/31– (352 × VREF6+1088 × VREF7) /1395	10.523	0.016

■ Functional Description (continued)

• Table 1 (continued) Relationship between VREF Voltages and Analog Output Voltages (High-level side) (Values are examples)
VREF5 = 9.200, VREF6 = 10.635, VREF7 = 12.380, VREF8 = 13.854, VREF9 = 14.630, VOPU = 11.250

Display data	Logical expression	Voltage level	Voltage level difference
A0	VOPU × 63/31– (365 × VREF6+1075 × VREF7) /1395	10.539	0.016
A1	VOPU × 63/31– (378 × VREF6+1062 × VREF7) /1395	10.556	0.016
A2	VOPU × 63/31– (391 × VREF6+1049 × VREF7) /1395	10.572	0.016
⋮			
AD	VOPU × 63/31– (534 × VREF6+906 × VREF7) /1395	10.751	0.016
AE	VOPU × 63/31– (547 × VREF6+893 × VREF7) /1395	10.767	0.016
AF	VOPU × 63/31– (560 × VREF6+880 × VREF7) /1395	10.783	0.016
B0	VOPU × 63/31– (573 × VREF6+867 × VREF7) /1395	10.800	0.016
B1	VOPU × 63/31– (586 × VREF6+854 × VREF7) /1395	10.816	0.016
B2	VOPU × 63/31– (599 × VREF6+841 × VREF7) /1395	10.832	0.016
⋮			
BD	VOPU × 63/31– (742 × VREF6+698 × VREF7) /1395	11.011	0.016
BE	VOPU × 63/31– (755 × VREF6+685 × VREF7) /1395	11.027	0.016
BF	VOPU × 63/31– (768 × VREF6+672 × VREF7) /1395	11.043	0.022
C0	VOPU × 63/31– (786 × VREF6+654 × VREF7) /1395	11.066	0.022
C1	VOPU × 63/31– (804 × VREF6+636 × VREF7) /1395	11.089	0.022
C2	VOPU × 63/31– (822 × VREF6+618 × VREF7) /1395	11.111	0.022
⋮			
CD	VOPU × 63/31– (1020 × VREF6+420 × VREF7) /1395	11.359	0.022
CE	VOPU × 63/31– (1038 × VREF6+402 × VREF7) /1395	11.381	0.022
CF	VOPU × 63/31– (1056 × VREF6+384 × VREF7) /1395	11.404	0.030
D0	VOPU × 63/31– (1080 × VREF6+360 × VREF7) /1395	11.434	0.030
D1	VOPU × 63/31– (1104 × VREF6+336 × VREF7) /1395	11.464	0.030
D2	VOPU × 63/31– (1128 × VREF6+312 × VREF7) /1395	11.494	0.030
⋮			
DD	VOPU × 63/31– (1392 × VREF6+48 × VREF7) /1395	11.824	0.030
DE	VOPU × 63/31– (1416 × VREF6+24 × VREF7) /1395	11.854	0.030
DF	VOPU × 63/31– (1440 × VREF6+0 × VREF7) /1395	11.884	0.041
E0	VOPU × 63/31– (66 × VREF5+2302 × VREF6) /2294	11.926	0.041
E1	VOPU × 63/31– (132 × VREF5+2236 × VREF6) /2294	11.967	0.041
E2	VOPU × 63/31– (198 × VREF5+2170 × VREF6) /2294	12.008	0.041
⋮			
ED	VOPU × 63/31– (924 × VREF5+1444 × VREF6) /2294	12.462	0.041
EE	VOPU × 63/31– (990 × VREF5+1378 × VREF6) /2294	12.504	0.041
EF	VOPU × 63/31– (1056 × VREF5+1312 × VREF6) /2294	12.545	0.051

■ Functional Description (continued)

• Table 1 (continued) Relationship between VREF Voltages and Analog Output Voltages (High-level side) (Values are examples)
VREF5 = 9.200, VREF6 = 10.635, VREF7 = 12.380, VREF8 = 13.854, VREF9 = 14.630, VOPU = 11.250

Display data	Logical expression	Voltage level	Voltage level difference
F0	VOPU × 63/31– (1138 × VREF5+1230 × VREF6) /2294	12.596	0.051
F1	VOPU × 63/31– (1220 × VREF5+1148 × VREF6) /2294	12.647	0.051
F2	VOPU × 63/31– (1302 × VREF5+1066 × VREF6) /2294	12.699	0.051
⋮			
FD	VOPU × 63/31– (2204 × VREF5+164 × VREF6) /2294	13.263	0.051
FE	VOPU × 63/31– (2286 × VREF5+82 × VREF6) /2294	13.314	0.051
FF	VOPU × 63/31– (2368 × VREF5+0 × VREF6) /2294	13.366	

• Table 2 Relationship between VREF Voltages and Analog Output Voltages (Low-level side) (Values are examples)
VREF0 = 1.760, VREF1 = 2.536, VREF2 = 4.010, VREF3 = 5.755, VREF4 = 7.190, VOPL = 3.750

Display data	Logical expression	Voltage level	Voltage level difference
00	VOPL × 63/31– (42 × VREF1+1238 × VREF0) /1240	5.777	0.026
01	VOPL × 63/31– (84 × VREF1+1196 × VREF0) /1240	5.751	0.026
02	VOPL × 63/31– (126 × VREF1+1154 × VREF0) /1240	5.725	0.026
⋮			
0D	VOPL × 63/31– (588 × VREF1+692 × VREF0) /1240	5.436	0.026
0E	VOPL × 63/31– (630 × VREF1+650 × VREF0) /1240	5.410	0.026
0F	VOPL × 63/31– (672 × VREF1+608 × VREF0) /1240	5.383	0.023
10	VOPL × 63/31– (710 × VREF1+570 × VREF0) /1240	5.360	0.023
11	VOPL × 63/31– (748 × VREF1+532 × VREF0) /1240	5.336	0.023
12	VOPL × 63/31– (786 × VREF1+494 × VREF0) /1240	5.312	0.023
⋮			
1D	VOPL × 63/31– (1204 × VREF1+76 × VREF0) /1240	5.051	0.023
1E	VOPL × 63/31– (1242 × VREF1+38 × VREF0) /1240	5.027	0.023
1F	VOPL × 63/31– (1280 × VREF1+0 × VREF0) /1240	5.003	0.020
20	VOPL × 63/31– (32 × VREF2+2400 × VREF1) /2356	4.983	0.020
21	VOPL × 63/31– (64 × VREF2+2368 × VREF1) /2356	4.963	0.020
22	VOPL × 63/31– (96 × VREF2+2336 × VREF1) /2356	4.943	0.020
⋮			
2D	VOPL × 63/31– (448 × VREF2+1984 × VREF1) /2356	4.723	0.020
2E	VOPL × 63/31– (480 × VREF2+1952 × VREF1) /2356	4.703	0.020
2F	VOPL × 63/31– (512 × VREF2+1920 × VREF1) /2356	4.683	0.016

■ Functional Description (continued)

• Table 2 (continued) Relationship between VREF Voltages and Analog Output Voltages (Low-level side) (Values are examples)
VREF0 = 1.760, VREF1 = 2.536, VREF2 = 4.010, VREF3 = 5.755, VREF4 = 7.190, VOPL = 3.750

Display data	Logical expression	Voltage level	Voltage level difference
30	VOPL × 63/31– (538 × VREF2+1894 × VREF1) /2356	4.666	0.016
31	VOPL × 63/31– (564 × VREF2+1868 × VREF1) /2356	4.650	0.016
32	VOPL × 63/31– (590 × VREF2+1842 × VREF1) /2356	4.634	0.016
⋮			
3D	VOPL × 63/31– (876 × VREF2+1556 × VREF1) /2356	4.455	0.016
3E	VOPL × 63/31– (902 × VREF2+1530 × VREF1) /2356	4.439	0.016
3F	VOPL × 63/31– (928 × VREF2+1504 × VREF1) /2356	4.422	0.015
40	VOPL × 63/31– (953 × VREF2+1479 × VREF1) /2356	4.407	0.015
41	VOPL × 63/31– (978 × VREF2+1454 × VREF1) /2356	4.391	0.015
42	VOPL × 63/31– (1003 × VREF2+1429 × VREF1) /2356	4.376	0.015
⋮			
4D	VOPL × 63/31– (1278 × VREF2+1154 × VREF1) /2356	4.203	0.015
4E	VOPL × 63/31– (1303 × VREF2+1129 × VREF1) /2356	4.188	0.015
4F	VOPL × 63/31– (1328 × VREF2+1104 × VREF1) /2356	4.172	0.015
50	VOPL × 63/31– (1353 × VREF2+1079 × VREF1) /2356	4.157	0.015
51	VOPL × 63/31– (1378 × VREF2+1054 × VREF1) /2356	4.141	0.015
52	VOPL × 63/31– (1403 × VREF2+1029 × VREF1) /2356	4.125	0.015
⋮			
5D	VOPL × 63/31– (1678 × VREF2+754 × VREF1) /2356	3.953	0.015
5E	VOPL × 63/31– (1703 × VREF2+729 × VREF1) /2356	3.938	0.015
5F	VOPL × 63/31– (1728 × VREF2+704 × VREF1) /2356	3.922	0.013
60	VOPL × 63/31– (1750 × VREF2+682 × VREF1) /2356	3.908	0.013
61	VOPL × 63/31– (1772 × VREF2+660 × VREF1) /2356	3.894	0.013
62	VOPL × 63/31– (1794 × VREF2+638 × VREF1) /2356	3.881	0.013
⋮			
6D	VOPL × 63/31– (2036 × VREF2+396 × VREF1) /2356	3.729	0.013
6E	VOPL × 63/31– (2058 × VREF2+374 × VREF1) /2356	3.716	0.013
6F	VOPL × 63/31– (2080 × VREF2+352 × VREF1) /2356	3.702	0.013
70	VOPL × 63/31– (2102 × VREF2+330 × VREF1) /2356	3.688	0.013
71	VOPL × 63/31– (2124 × VREF2+308 × VREF1) /2356	3.674	0.013
72	VOPL × 63/31– (2146 × VREF2+286 × VREF1) /2356	3.660	0.013
⋮			
7D	VOPL × 63/31– (2388 × VREF2+44 × VREF1) /2356	3.509	0.013
7E	VOPL × 63/31– (2410 × VREF2+22 × VREF1) /2356	3.495	0.013
7F	VOPL × 63/31– (2432 × VREF2+0 × VREF1) /2356	3.482	0.013

■ Functional Description (continued)

• Table 2 (continued) Relationship between VREF Voltages and Analog Output Voltages (Low-level side) (Values are examples)
VREF0 = 1.760, VREF1 = 2.536, VREF2 = 4.010, VREF3 = 5.755, VREF4 = 7.190, VOPL = 3.750

Display data	Logical expression	Voltage level	Voltage level difference
80	VOPL × 63/31− (11 × VREF3+1429 × VREF2) /1395	3.468	0.013
81	VOPL × 63/31− (22 × VREF3+1418 × VREF2) /1395	3.454	0.013
82	VOPL × 63/31− (33 × VREF3+1407 × VREF2) /1395	3.440	0.013
⋮			
8D	VOPL × 63/31− (154 × VREF3+1286 × VREF2) /1395	3.289	0.013
8E	VOPL × 63/31− (165 × VREF3+1275 × VREF2) /1395	3.275	0.013
8F	VOPL × 63/31− (176 × VREF3+1264 × VREF2) /1395	3.261	0.013
90	VOPL × 63/31− (187 × VREF3+1253 × VREF2) /1395	3.248	0.013
91	VOPL × 63/31− (198 × VREF3+1242 × VREF2) /1395	3.234	0.013
92	VOPL × 63/31− (209 × VREF3+1231 × VREF2) /1395	3.220	0.013
⋮			
9D	VOPL × 63/31− (330 × VREF3+1110 × VREF2) /1395	3.069	0.013
9E	VOPL × 63/31− (341 × VREF3+1099 × VREF2) /1395	3.055	0.013
9F	VOPL × 63/31− (352 × VREF3+1088 × VREF2) /1395	3.041	0.016
A0	VOPL × 63/31− (365 × VREF3+1075 × VREF2) /1395	3.025	0.016
A1	VOPL × 63/31− (378 × VREF3+1062 × VREF2) /1395	3.009	0.016
A2	VOPL × 63/31− (391 × VREF3+1049 × VREF2) /1395	2.992	0.016
⋮			
AD	VOPL × 63/31− (534 × VREF3+906 × VREF2) /1395	2.813	0.016
AE	VOPL × 63/31− (547 × VREF3+893 × VREF2) /1395	2.797	0.016
AF	VOPL × 63/31− (560 × VREF3+880 × VREF2) /1395	2.781	0.016
B0	VOPL × 63/31− (573 × VREF3+867 × VREF2) /1395	2.765	0.016
B1	VOPL × 63/31− (586 × VREF3+854 × VREF2) /1395	2.748	0.016
B2	VOPL × 63/31− (599 × VREF3+841 × VREF2) /1395	2.732	0.016
⋮			
BD	VOPL × 63/31− (742 × VREF3+698 × VREF2) /1395	2.553	0.016
BE	VOPL × 63/31− (755 × VREF3+685 × VREF2) /1395	2.537	0.016
BF	VOPL × 63/31− (768 × VREF3+672 × VREF2) /1395	2.521	0.022
C0	VOPL × 63/31− (786 × VREF3+654 × VREF2) /1395	2.498	0.022
C1	VOPL × 63/31− (804 × VREF3+636 × VREF2) /1395	2.476	0.022
C2	VOPL × 63/31− (822 × VREF3+618 × VREF2) /1395	2.453	0.022
⋮			
CD	VOPL × 63/31− (1020 × VREF3+420 × VREF2) /1395	2.205	0.022
CE	VOPL × 63/31− (1038 × VREF3+402 × VREF2) /1395	2.183	0.022
CF	VOPL × 63/31− (1056 × VREF3+384 × VREF2) /1395	2.160	0.030

■ Functional Description (continued)

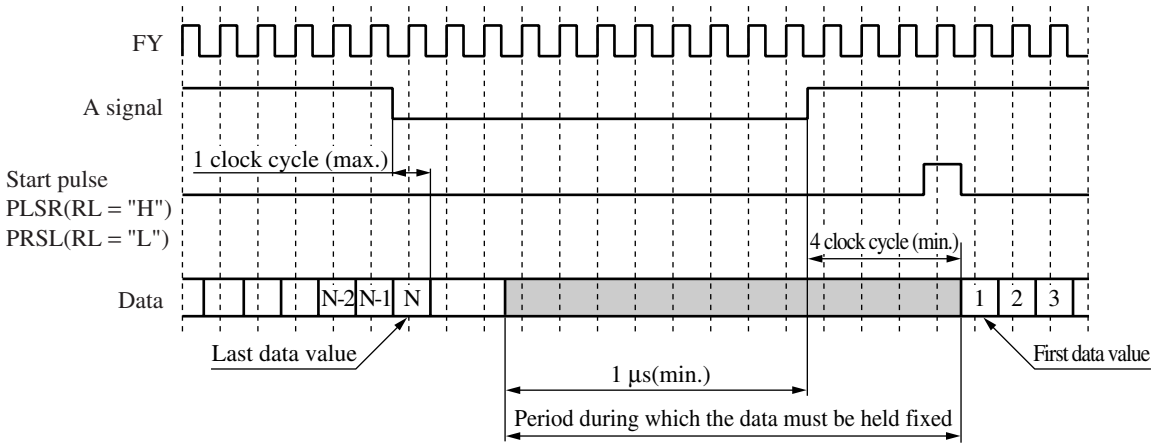
• Table 2 (continued) Relationship between VREF Voltages and Analog Output Voltages (Low-level side) (Values are examples)
VREF0 = 1.760, VREF1 = 2.536, VREF2 = 4.010, VREF3 = 5.755, VREF4 = 7.190, VOPL = 3.750

Display data	Logical expression	Voltage level	Voltage level difference
D0	VOPL × 63/31− (1080 × VREF3+360 × VREF2) /1395	2.130	0.030
D1	VOPL × 63/31− (1104 × VREF3+336 × VREF2) /1395	2.100	0.030
D2	VOPL × 63/31− (1128 × VREF3+312 × VREF2) /1395	2.070	0.030
⋮			
DD	VOPL × 63/31− (1392 × VREF3+48 × VREF2) /1395	1.740	0.030
DE	VOPL × 63/31− (1416 × VREF3+24 × VREF2) /1395	1.710	0.030
DF	VOPL × 63/31− (1440 × VREF3+0 × VREF2) /1395	1.680	0.041
E0	VOPL × 63/31− (66 × VREF4+2302 × VREF3) /2294	1.639	0.041
E1	VOPL × 63/31− (132 × VREF4+2236 × VREF3) /2294	1.597	0.041
E2	VOPL × 63/31− (198 × VREF4+2170 × VREF3) /2294	1.556	0.041
⋮			
ED	VOPL × 63/31− (924 × VREF4+1444 × VREF3) /2294	1.102	0.041
EE	VOPL × 63/31− (990 × VREF4+1378 × VREF3) /2294	1.061	0.041
EF	VOPL × 63/31− (1056 × VREF4+1312 × VREF3) /2294	1.019	0.051
F0	VOPL × 63/31− (1138 × VREF4+1230 × VREF3) /2294	0.968	0.051
F1	VOPL × 63/31− (1220 × VREF4+1148 × VREF3) /2294	0.917	0.051
F2	VOPL × 63/31− (1302 × VREF4+1066 × VREF3) /2294	0.865	0.051
⋮			
FD	VOPL × 63/31− (2204 × VREF4+164 × VREF3) /2294	0.301	0.051
FE	VOPL × 63/31− (2286 × VREF4+82 × VREF3) /2294	0.250	0.051
FF	VOPL × 63/31− (2368 × VREF4+0 × VREF3) /2294	0.199	

■ Functional Description (continued)

• Relationship between the A signal, the image input timing, and the start pulse

The figure below shows the relationship between the A signal, the image data input timing, and the start pulse. The last data of the image should be input within one clock cycle of the fall of the A signal. Data input two or more clock cycles later will not be transmitted to the analog outputs and the IC will not be able to output the correct analog voltage. And also hold the levels of the data bus fixed from 1 µs before the rise of the A signal until 4 clock cycles after the rise of the A signal. The output analog voltages may be displaced or shifted if the data bus levels are changed with that timing.



■ Functional Description (continued)

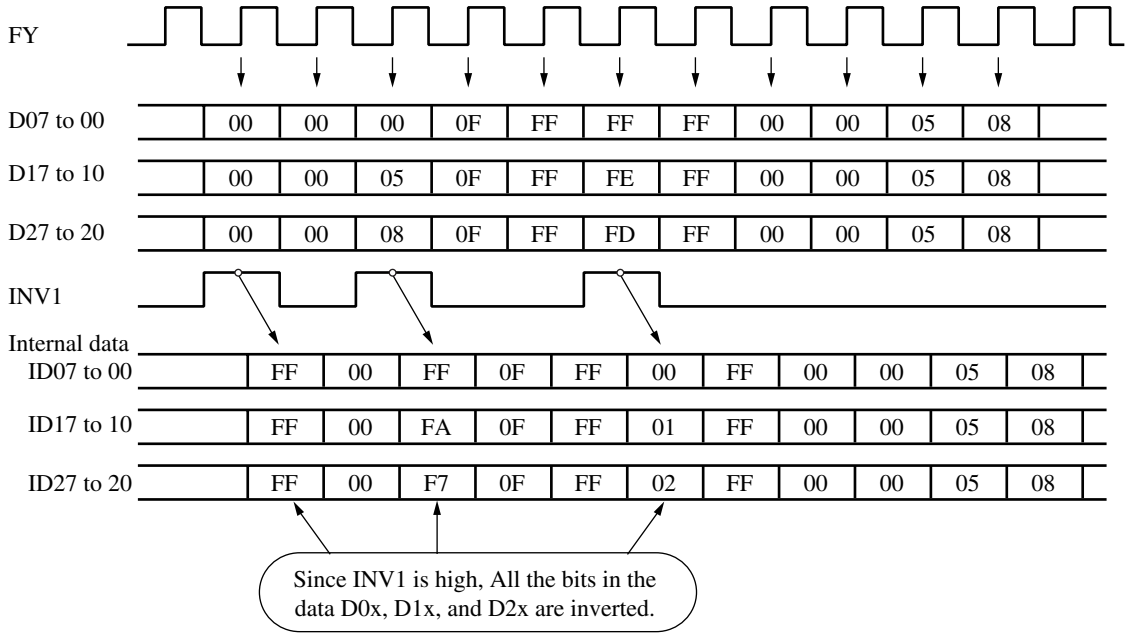
• Data inversion control function

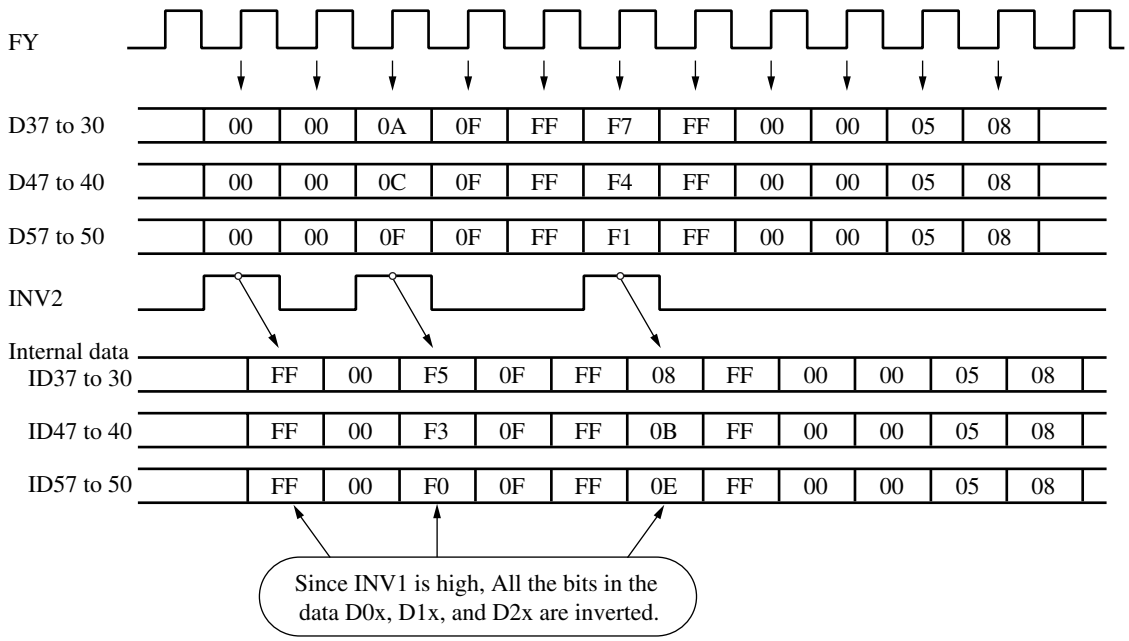
All the bits in the input image data can be inverted at the same time, thus creating new data values to be used by controlling the INV1 and INV2 pins.

INV1 inverts the D0(7:0), D1(7:0), and D2(7:0) data and INV2 inverts the D3(7:0), D4(7:0), and D5(7:0) data.

The figure below shows the inversion control provided by INV1 and INV2 for the input image data.

The input image data and the INV1 and INV2 states are acquired on the same clock cycle, and the data is controlled by the INV1 and INV2 logic states at that time.





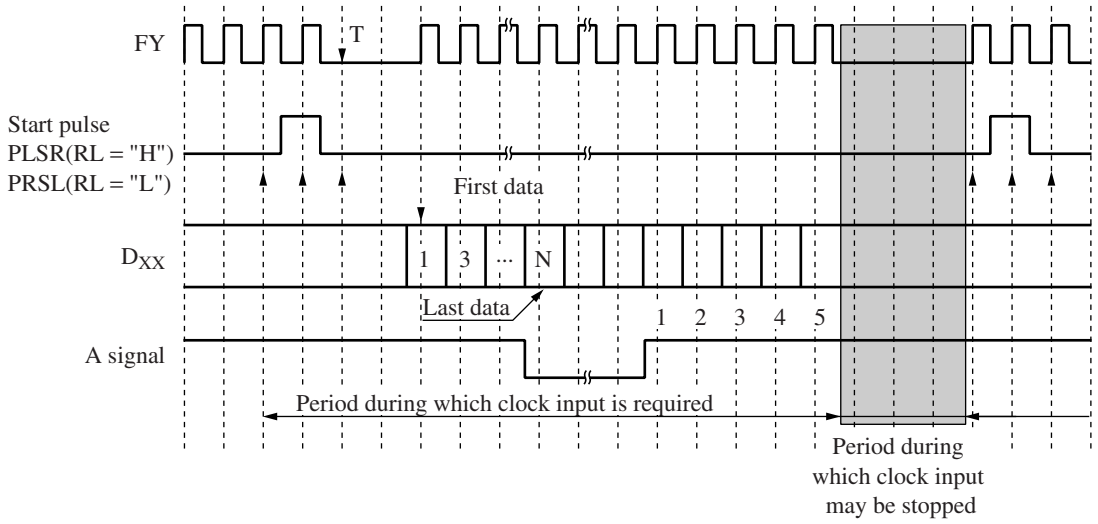
■ Functional Description (continued)

• Possible periods of the clock stop

The possible periods of the clock stop in which clock has been stopped are shown below.

The clock signal must be provided during the period starting one clock cycle before the start pulse input and ending 5 clock cycles after the rise of the A signal.

However, if it is not the case that the first data is input with the next clock timing (T) after the input of the start pulse, the clock may be stopped during the period between the start pulse input and the start of data input. The clock signal may be stopped at either the high or low level.



■ Electrical Characteristics

1. Absolute Maximum Ratings at A_{VSS} = 0 V, D_{VSS} = 0 V

Parameter	Symbol	Rating	Unit
Digital system supply voltage	D_{VDD}	– 0.3 to +7.0	V
Analog system supply voltage	A_{VDD}	– 0.3 to +17	V
Digital input voltage	V_{I1}	– 0.3 to D_{VDD}+0.3	V
Analog input voltage	V_{I2}	– 0.3 to A_{VDD}+0.3	V
Digital output voltage	V_{O1}	– 0.3 to D_{VDD}+0.3	V
Analog output voltage	V_{O2}	– 0.3 to A_{VDD}+0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +110	°C

Note) The absolute maximum ratings are limiting values under which the device will not be destroyed. Operation is not guaranteed within these ranges.

■ Electrical Characteristics (continued)

2. Operating Conditions at $A_{VSS} = D_{VSS} = 0$ V, $T_a = -20$ °C to +75 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating digital system supply voltage	D_{VDD}	$f_{FY\ max} = 50$ MHz	3.1	—	3.6	V
		$f_{FY\ max} = 40$ MHz	2.7	—	3.6	
Operating analog system supply voltage	A_{VDD}		14.5	—	15.5	V
γ correction voltage input voltage range	V_{REF}0to4		0.2	—	$A_{VDD}/2$	V
	V_{REF}5to9		$A_{VDD}/2$	—	$A_{VDD}-0.2$	
Operating frequency		D_{VDD} = 3.1 V to 3.6 V	—	—	50	MHz
		D_{VDD} = 2.7 V to 3.6 V	—	—	40	
Digital signal input capacitance	C_{IN}	At 1 MHz	—	5	—	pF
γ correction voltage input capacitance	C_{VREF}	At 1 MHz	—	500	—	pF
VOPL input voltage range			$A_{VDD}/4$ – 0.2	—	$A_{VDD}/4$ + 0.2	V
VOPU input voltage range			A_{VDD} × 3/4– 0.2	—	A_{VDD} × 3/4+ 0.2	V
VREF resistance VREF9 to 5, VREF4 to 0	R_{VREF}		—	14	—	kΩ

Note) 1. All the A_{VDD} power supply pins must be connected to each other directly.

2. All the A_{VSS} and D_{VSS} power supply pins must be connected to each other directly.

3. When first applying power, first apply the D_{VDD} voltage, then apply the logic input pin signal levels, and then apply the A_{VDD} voltage. After that apply the VOP and VREF reference voltages. When cutting the power, remove these voltages in the reverse order.

3. DC Characteristics at D_{VDD} = 2.7 V to 3.6 V, A_{VDD} = 14.5 V to 15.5 V, $A_{VSS} = D_{VSS} = 0$ V, $T_a = -20$ °C to +75 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating analog supply current 1 *1,3	I_{SS1}		—	39	45	mA
Operating analog supply current 2	I_{SS2}	A_{VDD} = 15 V *1, 3 With no load	—	11	—	mA
Operating digital supply current *1,2	I_{SS3}		—	2	8	mA
Digital quiescent supply current	I_{SS4}	In the clock stopped state	—	—	100	µA
1) Input pins RL, A, D00 to D07, D10 to D17, D20 to D27, D30 to D37, D40 to D47, D50 to D57, FY, POL, INV1, INV2						
High-level input voltage	V_{IH1}		$0.7 \times D_{VDD}$	—	D_{VDD}	V
Low-level input voltage	V_{IL1}		0	—	$0.3 \times D_{VDD}$	V
Input leakage current	I_{LI1}		−10	—	10	µA
2) I/O pins PRSL, PLSR						
High-level input voltage	V_{IH2}		$0.7 \times D_{VDD}$	—	D_{VDD}	V
Low-level input voltage	V_{IL2}		0	—	$0.3 \times D_{VDD}$	V
High-level output voltage	V_{OH}	D_{VDD} = 3.3 V, IO = −5 mA	$0.7 \times D_{VDD}$	—	—	V
Low-level output voltage	V_{OL}	D_{VDD} = 3.3 V, IO = 2 mA	—	—	$0.3 \times D_{VDD}$	V
Input leakage current	I_{LI2}		−10	—	10	µA

■ Electrical Characteristics (continued)

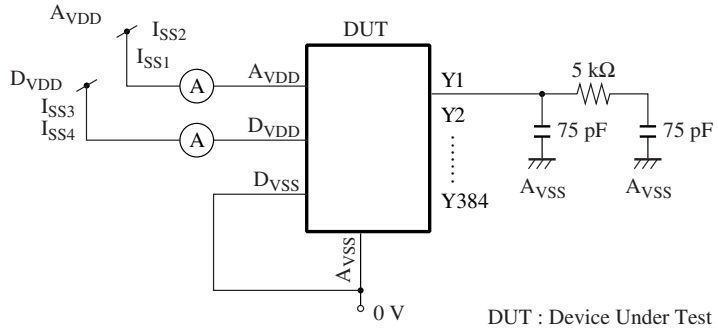
3. DC Characteristics at D_{VDD} = 2.7 V to 3.6 V, A_{VDD} = 14.5 V to 15.5 V, A_{VSS} = D_{VSS} = 0 V, T_a = –20 °C to +75 °C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
3) Pull-down resistor pin TEST						
High-level input voltage	V_{IH3}		0.7 × D_{VDD}	—	D_{VDD}	V
Low-level input voltage	V_{IL3}		0	—	0.3× D_{VDD}	V
Input leakage current	I_{LI3}		–10	—	10	µA
Pull-down resistance	R_{PD}		40	100	350	kΩ
4) Reference voltage input pins VOPU, VOPL						
Input current	I_{VOP}		–100	—	100	µA
5) Analog output pins Y1 to Y384						
Output current *4	I_{VOH}	V_X = 15 V, V_{OUT} = 14 V, A_{VDD} = 15 V, D_{VDD} = 3.3 V	—	– 0.5	– 0.2	mA
	I_{VOL}	V_X = 0.0 V, V_{OUT} = 1.0 V, A_{VDD} = 15 V, D_{VDD} = 3.3 V	0.2	0.5	—	
Output voltage difference *5	ΔV_O	A_{VDD} = 15 V, D_{VDD} = 3.3 V	—	±4	±20	mV
6) Analog output pin (Y1 to Y384) output voltage range						
Operating voltage range *6	V_O		A_{VSS}+0.2	—	A_{VDD}– 0.2	V

Note) 1. *1: The standard conditions are as follows. A clock frequency of 50 MHz, a raster period of 15 µs, the data pattern fixed at FF, the POL level switched between high and low at each raster period, INV1 and INV2 held fixed at the low level, and each of VREF0 to VREF9 held fixed at its respective levels.

*2: The maximum conditions are as follows. A clock frequency of 50 MHz, a raster period of 15 µs, the data pattern switches between FF and 00 on each clock cycle, the POL level switched between high and low at each raster period, INV1 and INV2 held fixed at the low level, and each of VREF0 to VREF9 held fixed at its respective levels.

*3: The loads on the analog output pins (Y1 to Y384) are shown below. The values of the components in the load circuit are subject to change.



DUT : Device Under Test

*4: The VX are the output voltages from the analog output pins Y1 to Y384.
The VOUT are the voltages applied to the analog output pins Y1 to Y384.

*5: The standard conditions apply when the output voltages are at the same voltage as VOPL and VOPU.

*6: Set up VREF0 to VREF9, VOPU, and VOPL so that the output voltages never exceed the output voltage range listed above.

2. The following formula expresses the power dissipation when the loads described in *3 above are attached.
$I_{SS1} \times A_{VDD} + I_{SS3} \times D_{VDD}$
Replace ISS1 in the above formula with the value of ISS2 to calculate the power dissipation when there is no load.

3. The supply current in the no load state is provided for reference purposes and is not guaranteed.

■ Electrical Characteristics (continued)

4. AC Characteristics at D_{VDD} = 2.7 V to 3.6 V, A_{VDD} = 14.5 V to 15.5 V, A_{VSS} = D_{VSS} = 0 V, T_a = –20 °C to +75 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
FY period	t_p	D_{VDD} = 3.1 V to 3.6 V	20	—	—	ns
		D_{VDD} = 2.7 V to 3.6 V	25	—	—	
Clock high-level period	t_{wcH}		4	—	—	ns
Clock low-level period	t_{wcL}		4	—	—	ns
Data and INV setup time	t_{st1}		0	—	—	ns
Data and INV hold time	t_{hd1}		4	—	—	ns
Start pulse setup time	t_{st2}		0	—	—	ns
Start pulse hold time	t_{hd2}		4	—	—	ns
Start pulse low-level period	t_{wsL}		2	—	—	Clock cycles
Start pulse high-level period	t_{wsH}		1	—	—	Clock cycles
Carry signal delay time	t_{d1}	CL = 15 pF, D_{VDD} = 3.1 V to 3.6 V	—	—	13	ns
		CL = 15 pF, D_{VDD} = 2.7 V to 3.6 V	—	—	17	
Carry signal rise time	t_c			64		Clock cycles
A signal low-level period	t_{wA}		2	—	—	µs
A signal start pulse setup time *1	t_{st3}		4	—	—	Clock cycles
Data input invalid time *1	t_{ng1}			1		Clock cycles
Last data timing *1	t_{ng2}		—	—	1	Clock cycles
LCD drive signal delay time *2,3	t_{d2}	A_{VDD} = 15 V	—	—	11	µs

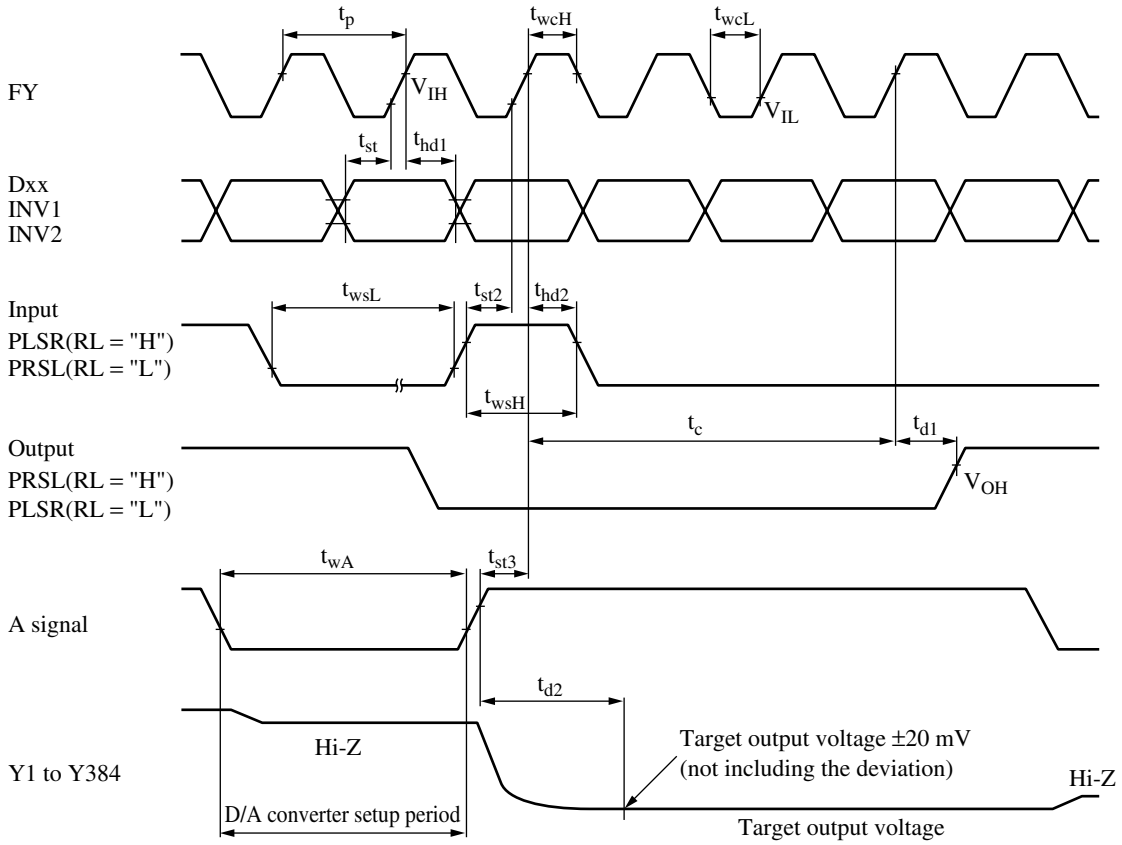
Note) *1: The starting point is at the rise of the first clock cycle after the rise of the PRSL (PLSR) signal.

*2: Stipulated as the value until the drive output voltage reaches the target output voltage ±20 mV (not including the deviation).

*3: See note 1. *3 in section 3. DC Characteristics for the analog output pin load.

■ Electrical Characteristics (continued)

4. AC Characteristics (continued)



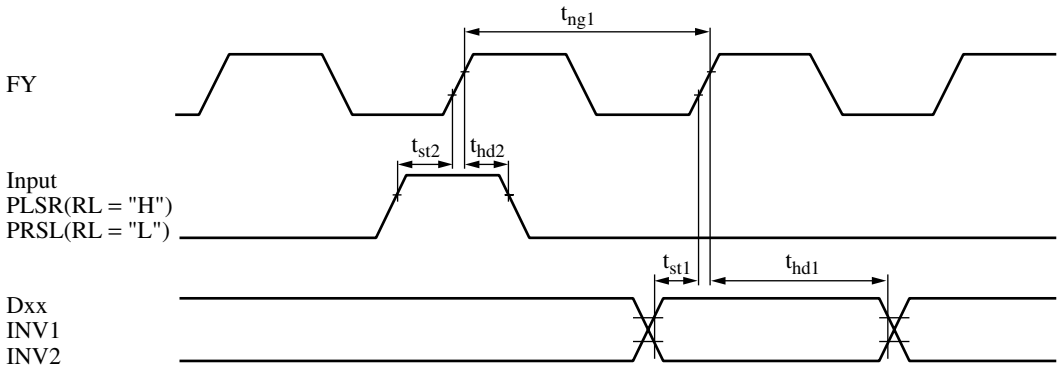
The D/A converter setup period (when the outputs are high impedance) is synchronized with the falling edge of the A signal.

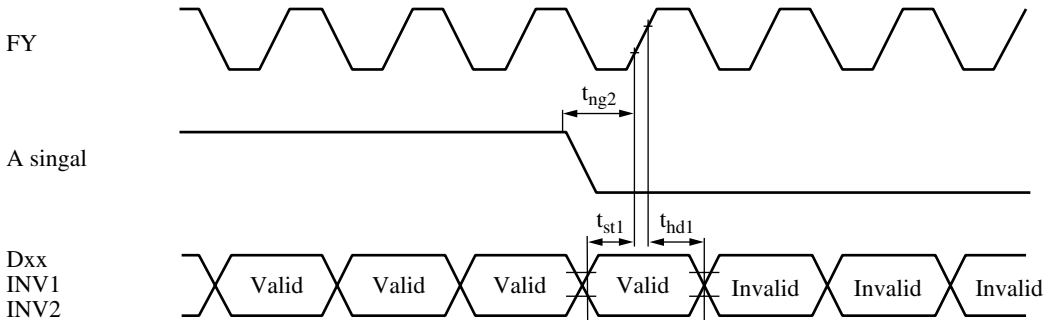
Unless otherwise specified, the digital input and output levels are

$V_{IH} = V_{OH}$ $0.7 \times D_{VDD}$, $V_{IL} = V_{OL} = 0.3 \times D_{VDD}$.

■ Electrical Characteristics (continued)

4. AC Characteristics (continued)





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