National Semiconductor

# MM54C95/MM74C95 4-Bit Right-Shift Left-Shift Register

## General Description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift register.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

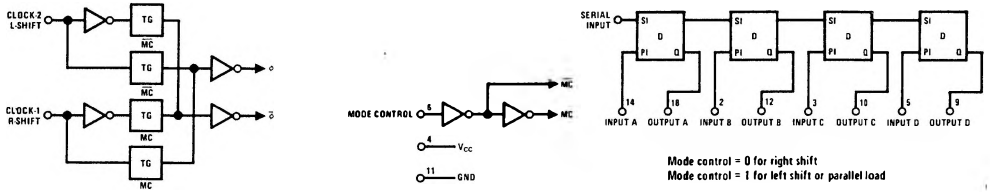
## Features

- Medium speed operation — 10 MHz (typ.) $V_{CC} = 10V$, $C_L = 50pF$
- High noise immunity — 0.45 $V_{CC}$ (typ.)
- Low power — 100 nW/ (typ.)
- Tenth power TTL compatible — Drive 2 LTTL loads
- Wide supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip flop
- Negative edge triggered clocking
- The MM54C95/MM74C95 follows the MM54L95/MM74L95 Pinout.

## Applications

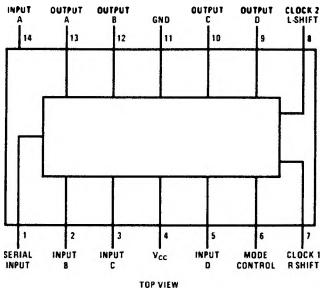
- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

## Block and Connection Diagrams




## Function Table

| INPUTS | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODE CONTROL | CLOCKS 2 (L) | CLOCKS 1 (R) | SERIAL | PARALLEL A | PARALLEL B | PARALLEL C | PARALLEL D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| H | H | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | ↓ | X | X | a | b | c | d | a | b | c | d |
| H | ↓ | X | X | $Q_B$↑ | $Q_C$↑ | $Q_D$↑ | d | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | d |
| L | L | H | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| L | X | ↓ | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| L | X | ↓ | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| ↑ | L | L | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↓ | L | L | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↓ | L | H | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↑ | H | L | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↑ | H | H | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| ↑ | L | H | X | X | X | X | X | Undefined | | | |
| ↓ | H | L | X | X | X | X | X | Operating Conditions | | | |




†Shifting left requires external connection of $Q_B$ to A, $Q_C$ to B, and $Q_D$ to C. Serial data is entered at input D

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↑ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady state input at inputs A, B, C or D, respectively

$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady state input conditions were established.

$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$, $Q_{Dn}$ = the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the most-recent ↓ transition of the clock.

## Absolute Maximum Ratings (Note 1)

| | | | |
|---|---|---|---|
| Voltage at Any Pin | −0.3 V to $V_{CC}$+0.3 V | Maximum $V_{CC}$ Voltage | 18V |
| Operating Temperature | | Package Dissipation | 500 mW |
| MM54C95 | −55°C to +125°C | Operating $V_{CC}$ Range | +3 V to +15 V |
| MM74C95 | −40°C to +85°C | Lead Temperature (Soldering, 10 sec.) | 300°C |
| Storage Temperature | −65°C to +150°C | | |

## DC Electrical Characteristics Max./min. limits apply across temperature range unless otherwise noted.

| | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | **CMOS to CMOS** | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}$ = 5.0 V | 3.5 | | | V |
| | | $V_{CC}$ = 10 V | 8.0 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}$ = 5.0 V | | | 1.5 | V |
| | | $V_{CC}$ = 10 V | | | 2.0 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC}$ = 5.0 V | 4.5 | | | V |
| | | $V_{CC}$ = 10 V | 9 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 5.0 V | | | 0.5 | V |
| | | $V_{CC}$ = 10 V | | | 1 | V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC}$ = 15 V | | | 1 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC}$ = 15 V | −1 | | | μA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 15 V | | 0.050 | 300 | μA |
| | **Low Power TTL/CMOS Interface** | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 54C, $V_{CC}$ = 4.5 V | $V_{CC}$ − 1.5 | | | V |
| | | 74C, $V_{CC}$ = 4.75 V | $V_{CC}$ − 1.5 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 54C, $V_{CC}$ = 4.5 V | | | 0.8 | V |
| | | 74C, $V_{CC}$ = 4.75 V | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C, $V_{CC}$ = 4.5 V, $I_O$ = 360 μA | 2.4 | | | V |
| | | 74C, $V_{CC}$ = 4.75 V, $I_O$ = 360 μA | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C, $V_{CC}$ = 4.5 V, $I_O$ = 360 μA | | | 0.4 | V |
| | | 74C, $V_{CC}$ = 4.75 V, $I_O$ = 360 μA | | | 0.4 | V |
| | **Output Drive (See 54C/74C Family Characteristics Data Sheet)** | | | | | |
| $I_{SOURCE}$ | Output Source Current | $V_{CC}$ = 5.0 V, $V_{IN(0)}$ = 0 V, $T_A$ = 25°C, $V_{OUT}$ = 0 V | −1.75 | | | mA |
| $I_{SOURCE}$ | Output Source Current | $V_{CC}$ = 10 V, $V_{IN(0)}$ = 0 V, $T_A$ = 25°C, $V_{OUT}$ = 0 V | −8.0 | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC}$ = 5.0 V, $V_{IN(1)}$ = 5.0 V, $T_A$ = 25°C, $V_{OUT}$ = $V_{CC}$ | 1.75 | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC}$ = 10 V, $V_{IN(1)}$ = 10 V, $T_A$ = 25°C, $V_{OUT}$ = $V_{CC}$ | 8.0 | | | mA |

## AC Electrical Characteristics $T_A$ = 25°C, $C_L$ = 50 pF, unless otherwise noted.

| | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q | $V_{CC}$ = 5.0 V | | 200 | 400 | ns |
| | | $V_{CC}$ = 10 V | | 80 | 160 | ns |
| $t_{S0}$, $t_{S1}$ | Time Prior to Clock Pulse that Data must be Preset | $V_{CC}$ = 5.0 V | 60 | 30 | | ns |
| | | $V_{CC}$ = 10 V | 25 | 10 | | ns |
| $t_{H0}$, $t_{H1}$ | Time After Clock Pulse that Data must be Held | $V_{CC}$ = 5.0 V | 25 | 10 | | ns |
| | | $V_{CC}$ = 10 V | 10 | 50 | | ns |
| $t_{PW}$ | Minimum Clock Pulse Width ($t_{WL}$ = $t_{WH}$) | $V_{CC}$ = 5.0 V | | 100 | | ns |
| | | $V_{CC}$ = 10 V | | 50 | | ns |
| $t_{SM}$ | Time Prior to Clock Pulse that Mode Control must be Preset | $V_{CC}$ = 5.0 V | 200 | 100 | | ns |
| | | $V_{CC}$ = 10 V | 100 | 50 | | ns |
| $f_{MAX}$ | Maximum Input Clock Frequency | $V_{CC}$ = 5.0 V | 3 | 5 | | MHz |
| | | $V_{CC}$ = 10 V | 6.5 | 10 | | MHz |
| $C_{IN}$ | Input Capacitance | Any Input. (Note 2) | | 5 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance | (Note 3) | | 100 | | pF |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** $C_{PD}$ determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.