MM54C86,MM74C86

MM54C86 MM74C86 Quad 2-Input EXCLUSIVE-OR Gate

TEXAS INSTRUMENTS

National Semiconductor

MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate

General Description

Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range   3.0V to 15V
- Guaranteed noise margin   1.0V
- High noise immunity   0.45 V_{CC} (typ.)
- Low power   Fan out of 2
  TTL compatibility   driving 74L
- Low power consumption   10 nW/package (typ.)
- The MM54C86/MM74C86 follows the MM54LS86/MM74LS86 Pinout

Connection Diagram

Dual-In-Line Package

TL/F/5887–1

Top View
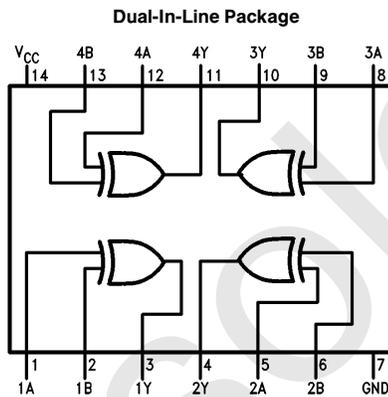
Order Number MM54C86 or MM74C86

Truth Table

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

H = High Level   L = Low Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin (Note 1)	-0.3V to $V_{CC} + 0.3$V
Operating Temperature Range	
MM54C86	$-55°$C to $+125°$C
MM74C86	$-40°$C to $+85°$C
Storage Temperature Range	$-65°$C to $+150°$C

Power Dissipation (P_D)	
Dual-In-Line Package	700 mW
Small Outline	500 mW
Operating Range (V_{CC})	3.0V to 15V
Absolute Maximum (V_{CC})	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0$V	3.5			V
		$V_{CC} = 10$V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0$V			1.5	V
		$V_{CC} = 10$V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0$V, $I_O = -10 \mu$A	4.5			V
		$V_{CC} = 10$V, $I_O = -10 \mu$A	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0$V, $I_O = +10 \mu$A			0.5	V
		$V_{CC} = 10$V, $I_O = +10 \mu$A			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15$V, $V_{IN} = 15$V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15$V, $V_{IN} = 0$V	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15$V		0.01	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5$V	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75$V	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5$V			0.8	V
		74C, $V_{CC} = 4.75$V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5$V, $I_O = -360 \mu$A	2.4			V
		74C, $V_{CC} = 4.75$V, $I_O = -360 \mu$A	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5$V, $I_O = 360 \mu$A			0.4	V
		74C, $V_{CC} = 4.75$V, $I_O = 360 \mu$A			0.4	V
OUTPUT DRIVE (See 54/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0$V, $V_{OUT} = 0$V $T_A = 25°$C	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10$V, $V_{OUT} = 0$V $T_A = 25°$C	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0$V, $V_{OUT} = V_{CC}$ $T_A = 25°$C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10$V, $V_{OUT} = V_{CC}$ $T_A = 25°$C	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* (MM54C86/MM74C86) T_A = 25°C, C_L = 50 pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Time to Logical "1" or "0"	V_{CC} = 5.0V V_{CC} = 10V		110 50	185 90	ns ns
C_{IN}	Input Capacitance	Note 2		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.
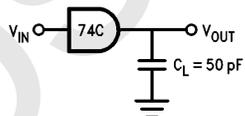
Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance MM54C86/MM74C86
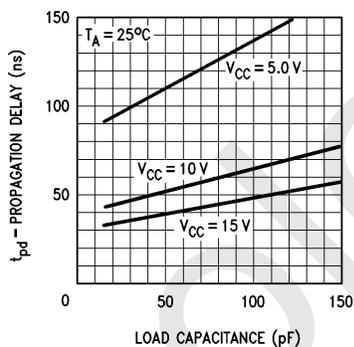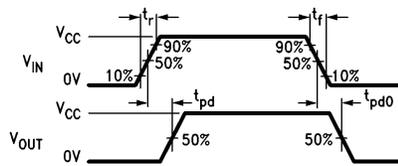

TL/F/5887–2

AC Test Circuit

TL/F/5887–3

Note: Delays Measured with Input t_r, t_f = 20 ns

Switching Time Waveforms

TL/F/5887–4

Physical Dimensions inches (millimeters)

Ceramic Dual-In-Line Package (J)
Order Number MM54C86J or MM74C86J
NS Package Number J14A

Molded Dual-In-Line Package (N)
Order Number MM54C86N or MM74C86N
NS Package Number N14A

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