![National Semiconductor logo]

MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{WE}$, and a $\overline{ME}$ line. The six address lines are internally decoded to select one of 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{ME}$. The TRI-STATE® outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{ME}$, and (t_{HA}) after the positive to negative transition of $\overline{ME}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{WE}$ goes low while $\overline{ME}$ is low. $\overline{WE}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{WE}$ returns high.

Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{WE}$ held high.

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Outputs are in the TRI-STATE® (Hi-Z) condition when the device is writing or disabled.
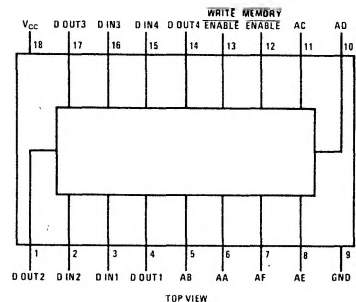
Features

■ Supply voltage range · · · · · · · · · · · 3.0 V to 5.5 V

■ High noise immunity · · · · · · · · · · · 0.45 V_{CC} (typ.)

■ TTL compatible fan out · · · · · · · · · · · 1 TTL load

■ Input address register

■ Low power consumption · · · · · 250 nW/package (typ.) (chip enabled or disabled)

■ Fast access time · · · · · · · · · 250 ns (typ.) at 5.0 V

■ TRI-STATE outputs

■ High voltage inputs

Logic and Connection Diagram

Input Protection
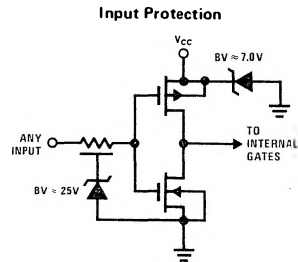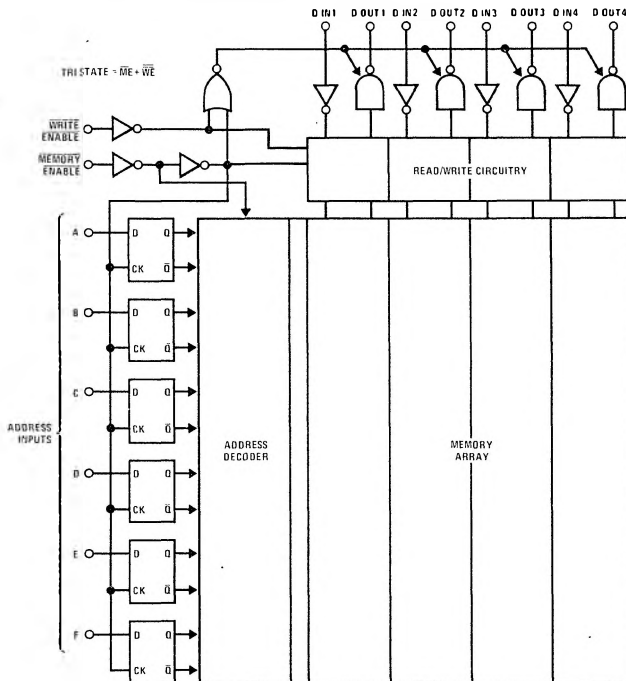
Dual-In-Line Package

TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at any Output Pin	$-0.3\,V$ to $V_{CC} + 0.3\,V$
Voltage at any Input Pin	$-0.3\,V$ to $+15\,V$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 5.5 V
Standby V_{CC} Range	1.5 V to 5.5 V
Absolute Maximum V_{CC}	6.0 V
Lead Temperature (Soldering, 10 seconds(	300°C

Operating Conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

DC Electrical Characteristics
Min./max. limits apply across the temperature and power supply range indicated

	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 15\,V$		0.005	2.0	µA
		$V_{IN} = 5.0\,V$		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0\,V$	−1.0	−0.005		µA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -150\,\mu A$	$V_{CC} - 0.5$			V
		$I_O = -400\,\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6\,mA$			0.4	V
	Output Current in High Impedance State	$V_O = 5.0\,V$		0.005	1.0	µA
		$V_O = 0\,V$	−1.0	−0.005		µA
I_{CC}	Supply Current	$V_{CC} = 5.0\,V$		5.0	300	µA

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0\,V$, $C_L = 50\,pF$

	Parameter		Min.	Typ.	Max.	Units
t_{ACC}	Access Time from Address			250	500	ns
t_{pd}	Propagation Delay from $\overline{ME}$			180	360	ns
t_{SA}	Address Input Set-Up Time		140	70		ns
t_{HA}	Address Input Hold Time		20	10		ns
$t_{\overline{ME}}$	Memory Enable Pulse Width		200	100		ns
$t_{\overline{ME}}$	Memory Enable Pulse Width		400	200		ns
t_{SD}	Data Input Set-Up Time		0			ns
t_{HD}	Data Input Hold Time		30	15		ns
$t_{\overline{WE}}$	Write Enable Pulse Width		140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE® (Note 4)			100	200	ns

	Capacitance					
C_{IN}	Input Capacity Any Input (Note 2)			5.0		pF
C_{OUT}	Output Capacity Any Output (Note 2)			9.0		pF
C_{PD}	Power Dissipation Capacity (Note 3)			350		pF

AC Electrical Characteristics (cont'd) $C_L = 50\,pF$

| Parameter		MM54C910 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5\,V$ to $5.5\,V$		MM74C910 $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.75\,V$ to $5.25\,V$		Units
		Min.	Max.	Min.	Max.	
t_{ACC}	Access Time from Address		860		700	ns
t_{pd1}, t_{pd0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
t_{ME}	Memory Enable Pulse Width	280		260		ns
$t_{\overline{ME}}$	Memory Enable Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	Write Enable Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE® (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

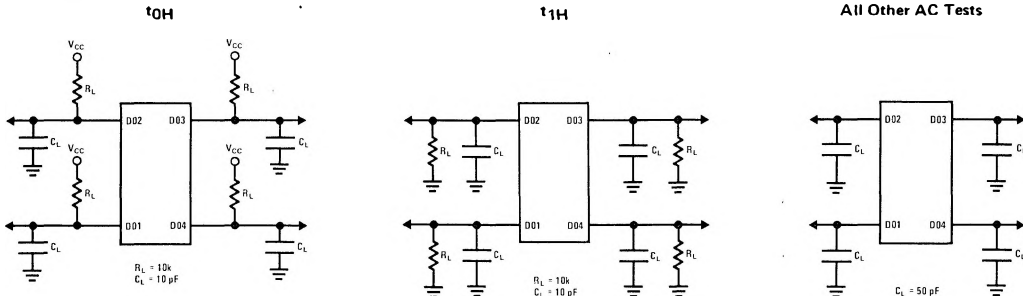**Note 4:** See AC test circuit for t_{1H}, t_{0H}.
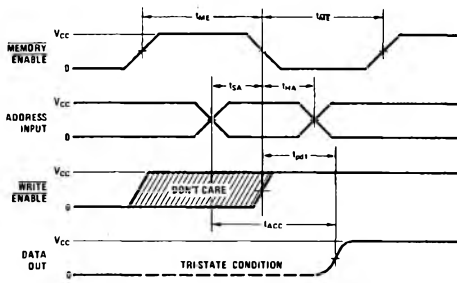
Typical Performance Characteristics

Typical Access Time vs Ambient Temperature
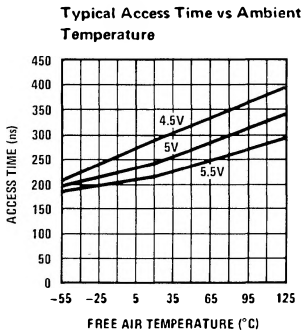
Truth Table

ME	WE	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

AC Test Circuit

Switching Time Waveforms

Read Cycle
(See Note 1)

MEMORY ENABLE

ADDRESS INPUT

WRITE ENABLE

DON'T CARE

DATA OUT

TRI STATE CONDITION

Write Cycle
(See Note 1)

MEMORY ENABLE

ADDRESS INPUT

WRITE ENABLE

DATA INPUT
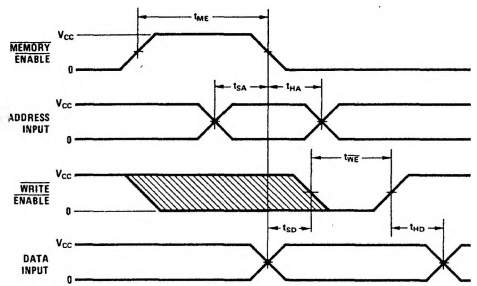
Read Modify Write Cycle
(See Note 1)

MEMORY ENABLE

ADDRESS INPUT

LATCHED ADDRESS

DATA OUT

TRI STATE CONDITION

TRI STATE CONDITION

WRITE ENABLE

DATA IN

t_{0H}

$\overline{ME}$

$0.5 \, V_{CC}$

DATA OUT

TRI-STATE

$0.1 \, V_{CC}$
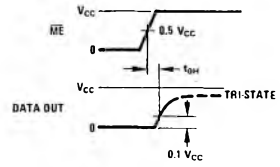
t_{1H}

$\overline{ME}$

$0.5 \, V_{CC}$

DATA OUT

$0.1 \, V_{CC}$

TRI-STATE
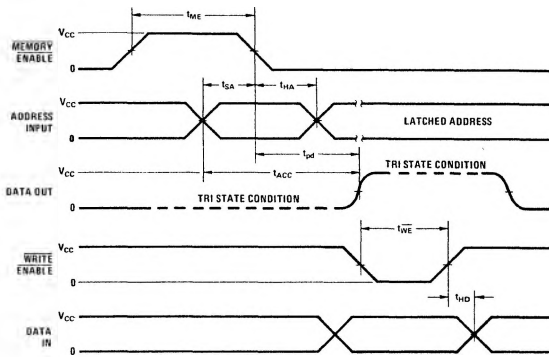
Note 1: MEMORY ENABLE must be brought high for t_{ME} nanoseconds between every address change.
Note 2: $t_r = t_f = 20$ ns for all inputs.