

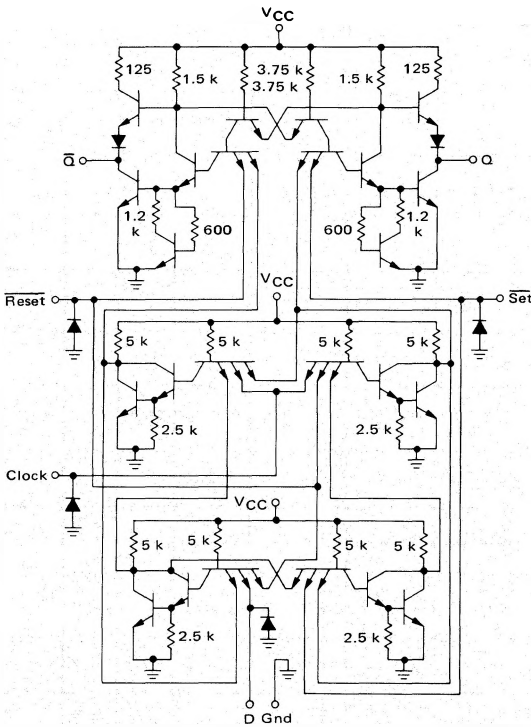
DUAL TYPE D FLIP-FLOP

MC5400/7400 series

MC5479 • MC7479

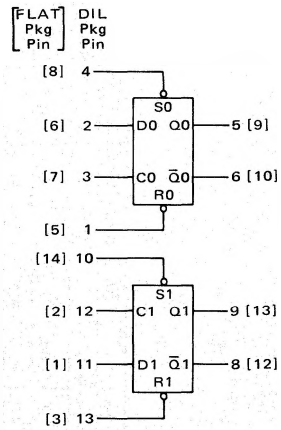
Add Suffix F for TO-86 ceramic package (Case 607).
 Suffix L for TO-116 ceramic package (Case 632).
 Suffix P for TO-116 plastic package (Case 605) MC7479 only.)

CIRCUIT SCHEMATIC
 1/2 OF DEVICE SHOWN



VCC = Pin 14 [4]
 Gnd = Pin 7 [11]

This dual type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.



t_n		t_{n+1}	
D	Q	Q	\bar{Q}
0	0	1	0
1	1	1	0

Input Loading Factor:

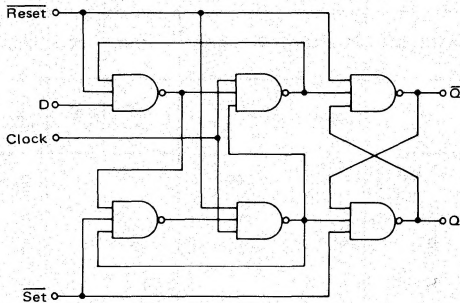
- D = 1
- Set, Clock = 2
- Reset = 3

Output Loading Factor = 10

Total Power Dissipation = 84 mW typ/pkg

Propagation Delay Time = 16 ns typ

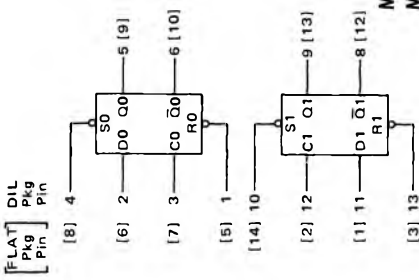
Operating Frequency = 30 MHz typ



LOGIC DIAGRAM
 1/2 OF DEVICE SHOWN

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



$V = V_{CC} = Pin\ 14\ [4]$
 $Gnd = Pin\ 7\ [11]$

Characteristic	Symbol	Pin Under Test	MC5479 Test Limits -55 to +125°C		MC7479 Test Limits 0 to +70°C		TEST CURRENT/VOLTAGE VALUES (All Temperatures)												Pin 7 [11] is grounded for all tests in addition to the pins listed below:		
			Min	Max	Min	Max	Volts														
			mA		mV																
Input Forward Current Set Reset Clock	I _F	D	-1.6	mAdc	-	-1.6	mAdc	I _{OH}	D	V _{IL}	V _{IH}	V _{R1}	V _{HH}	V _{R1}	V _{th1}	V _{th0}	V _{CC}	V _{CCL}	V _{CCH}	C0,C1 C0,C1,D0 C0,C1 C1,D0,S0	
		S	-3.2	mAdc	-	-3.2	mAdc	I _{OL}	S	0.4	2.4	4.5	5.5	4.5	2.0	0.8	5.0	4.50	5.50		
		R	-	mAdc	-	-	mAdc	I _{OL}	R	-	-	-	-	-	-	-	-	-	-	-	
Leakage Current Set Reset Clock	I _{R1}	D	-	40	μAdc	-	40	μAdc	I _{OH}	C	-	-	-	-	-	-	-	-	-	-	C1,R0 C1 C1,D0 C1,D0,R0
		S	-	80	μAdc	-	80	μAdc	I _{OL}	C	-	-	-	-	-	-	-	-	-	-	
		R	-	120	μAdc	-	120	μAdc	I _{OL}	C	-	-	-	-	-	-	-	-	-	-	
Output Output Voltage	V _{OL}	D	-	1.0	mAdc	-	1.0	mAdc	I _{OL}	C	-	-	-	-	-	-	-	-	-	-	C1,R0 C1 C1,D0 C1,D0,R0
		S	-	0.4	Vdc	-	0.4	Vdc	I _{OL}	C	-	-	-	-	-	-	-	-	-	-	
		R	-	0.4	Vdc	-	0.4	Vdc	I _{OL}	C	-	-	-	-	-	-	-	-	-	-	
Short-Circuit Current	I _{SC} †	Q	2.4	-	Vdc	2.4	-	Vdc	I _{OL}	Q	-	-	-	-	-	-	-	-	-	-	C0,C1,D0 C0,C1,D0
		Q	2.4	-	Vdc	2.4	-	Vdc	I _{OL}	Q	-	-	-	-	-	-	-	-	-	-	
Power Requirements (Total Device) Power Supply Drain	I _{pD}	Q	-20	-57	mAdc	-18	-57	mAdc	I _{OL}	Q	-	-	-	-	-	-	-	-	-	-	C0,S0,Q0 C1,R0,Q0
		Q	-20	-57	mAdc	-18	-57	mAdc	I _{OL}	Q	-	-	-	-	-	-	-	-	-	-	

*Momentarily ground pin prior to taking measurement, then set to state indicated.
 † Only one output should be shorted at a time.

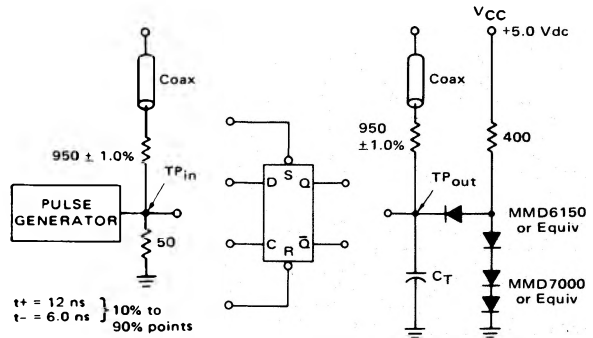
MC5479, MC7479 (continued)

OPERATING CHARACTERISTICS

Data may be applied to the D input any time following 5.0 ns after the leading edge of a clock pulse and 20 ns before the leading edge of the following clock pulse. The state of the D input when the clock changes from the positive logic "0" state to the positive logic "1" state is transferred to the Q output of the flip-flop. The data input cannot be changed between the setup time (20 ns) and the hold time (5.0 ns) without adversely affecting the operation of the flip-flop.

The direct $\overline{\text{Set}}$ and $\overline{\text{Reset}}$ inputs override the clock, and may be applied any time during the operating cycle.

SWITCHING TIME TEST CIRCUIT



PRF = 20 MHz for waveform 1
 = 1.0 MHz for waveforms 2 thru 5

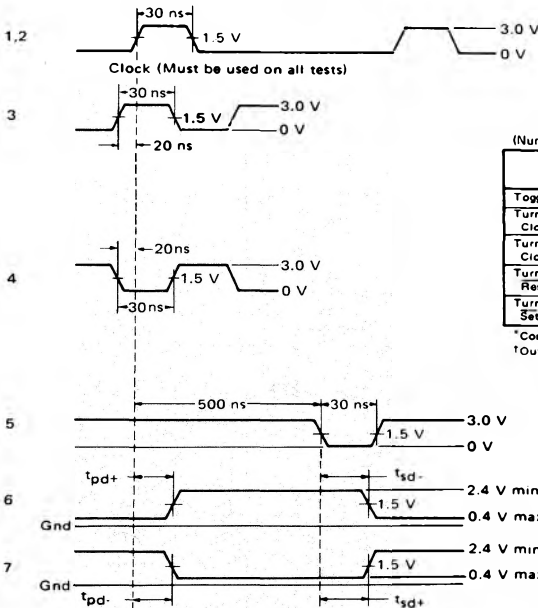
$Z_{out} \approx 50 \Omega$

Two pulse generators are required and must be slaved together to provide the waveforms shown. Only one pulse generator (duty cycle = 50%) is required to test toggle frequency.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 15 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

(Numbers shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	\overline{Q}	LIMITS		
		C	D	\overline{R}	\overline{S}			Min	Max	Unit
Toggle Frequency	t_{Tog}	1*	2.4 V	2.4 V	1	1	20	-		MHz
Turn-On Delay Clock to Q	t_{pd-}	2	4	2.4 V	2.4 V	7	6	-	30	ns
Turn-Off Delay Clock to Q	t_{pd+}	2	3	2.4 V	2.4 V	6	7	-	30	ns
Turn-On Delay Reset to Q	t_{sd-}	2	3	5	2.4 V	7	6	-	25	ns
Turn-Off Delay Set to Q	t_{sd+}	2	4	2.4 V	5	6	7	-	25	ns

*Connect to \overline{Q} .

†Output shall toggle with each input pulse.