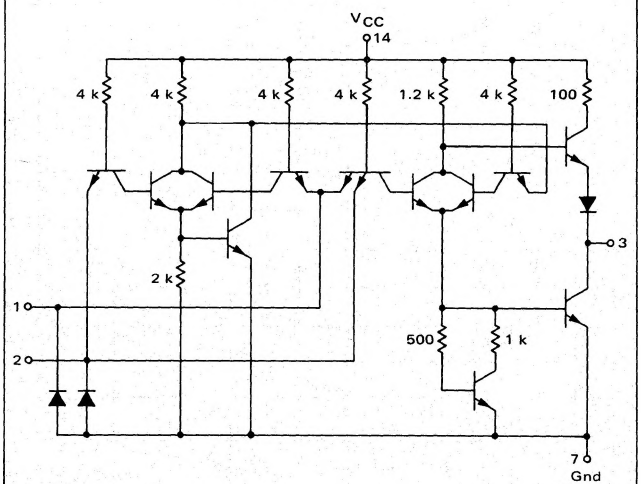
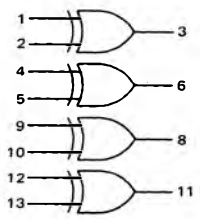
MC3121F • MC3021F
MC3121L • MC3021L,P

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



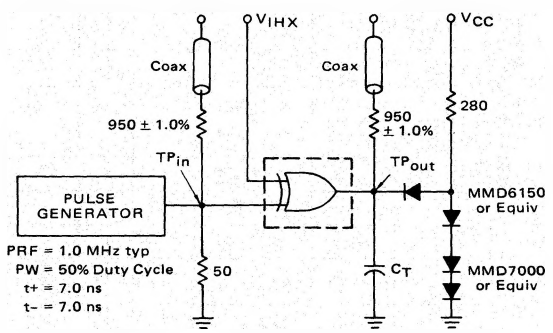
This device consists of four 2-input Exclusive OR gates. They can be used to build parity checking/generating functions. Up/down counters can be built using these gates and J-K flip-flops.

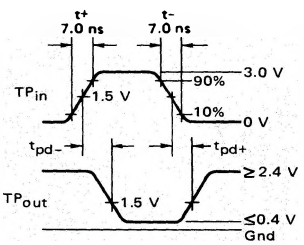


Positive Logic: $3 = 1 \bullet \overline{2} + \overline{1} \bullet 2$

Input Loading Factor = 1.6
Output Loading Factor = 8
Total Power Dissipation = 100 mW typ/pkg
Propagation Delay Time = 14 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





One input to gates not under test must be tied to V_{IHX} the other grounded.

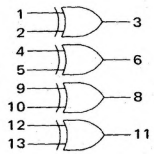
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES														
		mA				Volts										
		I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	V_{max}
MC3121	−55°C	16	-1.6	-	-	1.1	2.0	0.4	2.4	4.0	5.0	4.5	5.5	-	-
	+25°C	16	-1.6	1.0	1.0	1.1	1.8	0.4	2.4	4.0	5.0	4.5	5.5	2.5	7.0
	+125°C	16	-1.6	-	-	0.8	1.8	0.4	2.4	4.0	5.0	4.5	5.5	-	-
MC3021	0°C	16	-1.6	-	-	1.1	2.0	0.4	2.5	4.0	5.0	4.75	5.25	-	-
	+25°C	16	-1.6	1.0	1.0	1.1	1.8	0.4	2.5	4.0	5.0	4.75	5.25	2.5	7.0
	+75°C	16	-1.6	-	-	0.9	1.8	0.4	2.5	4.0	5.0	4.75	5.25	-	-

Characteristic	Symbol	Pin Under Test	MC3121 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC3021 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	V_{max}	Gnd
Input																														
Forward Current	I_F	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	1	-	2,5,10,13	-	-	14	-	-	4,7,9,12
Leakage Current	I_R	1	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	5,10,13	-	-	14	-	-	2,4,7,9,12
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	5.5	-	-	-	Vdc	-	-	1	-	-	-	-	-	5,10,13	-	-	14	-	-	2,4,7,9,12
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-1.5	-	-	Vdc	-	-	-	1	-	-	-	-	5,10,13	-	14	-	-	-	4,7,9,12
Output																														
Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.4	Vdc	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	1,2	-	-	-	5,10,13	-	14	-	-	-	4,7,9,12
		3	-	0.4	-	0.4	-	0.4	Vdc	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1,2	-	-	5,10,13	-	14	-	-	-	4,7,9,12
	V_{OH}	3	2.4	-	2.4	-	2.4	-	Vdc	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	1	2	-	-	5,10,13	-	14	-	-	-	4,7,9,12
		3	2.4	-	2.4	-	2.4	-	Vdc	2.5	-	2.5	-	2.5	-	Vdc	-	3	-	-	2	1	-	-	5,10,13	-	14	-	-	-	4,7,9,12
Short-Circuit Current	I_{SC}	3	-20	-65	-20	-65	-20	-65	mAdc	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	1	-	2,5,10,13	-	-	14	-	-	3,4,7,9,12
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	35	-	-	mAdc	-	-	-	40	-	-	mAdc	-	-	-	-	-	-	1,4,9,12	-	2,5,10,13	-	-	-	-	14	7
Power Supply Drain	I_{PDH}	14	-	28.6	-	28.6	-	28.6	mAdc	-	28.6	-	28.6	-	28.6	mAdc	-	-	-	-	-	-	1,4,9,12	-	2,5,10,13	-	-	14	-	-	7
	I_{PDL}	14	-	42.4	-	42.4	-	42.4	mAdc	-	42.4	-	42.4	-	42.4	mAdc	-	-	-	-	-	-	1,2,4,5	-	-	-	-	14	-	-	7
Switching Parameters																														
Turn-On Delay	t_{pd-}	1,3	-	-	-	25	-	-	ns	-	-	-	25	-	-	ns	1	-	-	-	-	-	-	-	-	14	-	-	2,5,10,13	-	4,7,9,12
Turn-Off Delay	t_{pd+}	1,3	-	-	-	25	-	-	ns	-	-	-	25	-	-	ns	1	-	-	-	-	-	-	-	-	14	-	-	2,5,10,13	-	4,7,9,12

Pins not listed are left open.