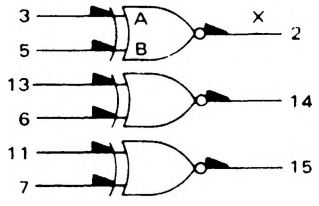

$X = A \bullet B + \bar{A} \bullet B$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, $I_L = -25$ mAdc max

Triple 2-input Exclusive-NOR Gate

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (−30° to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.