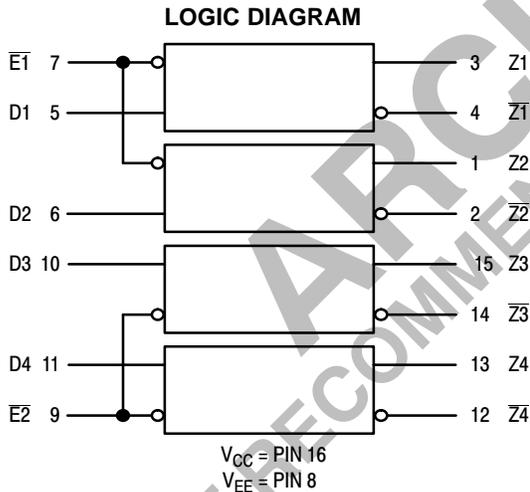


MC10192

Quad Bus Driver

The MC10192 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable (\bar{E}) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of I_R drop and load return voltage V_{LR} does not cause an output collector to go more negative than -2.4 V with respect to V_{CC} . To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC} . When the \bar{E} input is high, both output transistors of a driver are nonconducting. When not used, the \bar{E} inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kW Input Pulldown Resistors on All Inputs (Unused Inputs May Be Left Open)
- Power Dissipation = 575 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ (\bar{E} — Output)
3.0 ns typ (D — Output)



TRUTH TABLE

Inputs		Output	
\bar{E}	D	Z	\bar{Z}
H	X	H	H
L	H	H	L
L	L	L	H

Note: Unused outputs must be terminated to V_{CC} for proper operation.



ON Semiconductor

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MARKING DIAGRAMS



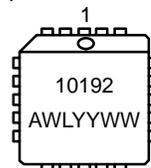
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648

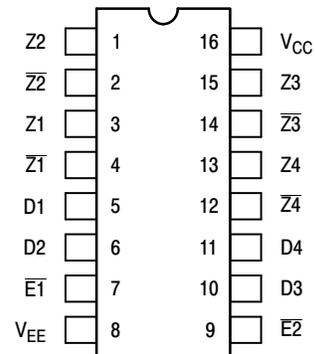


PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

ORDERING INFORMATION

Device	Package	Shipping
MC10192L	CDIP-16	25 Units / Rail
MC10192P	PDIP-16	25 Units / Rail
MC10192FN	PLCC-20	46 Units / Rail

MC10192

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit
			-30°C		+25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	8		154		140		154	mAdc
Input Current	I_{inH}	5		350		220		220	μ Adc
	I_{inL}	5	0.5		0.5		0.3		μ Adc
Output Current High	Logic 1 I_{OH}	2				2.0			mAdc
Output Current Low	Logic 0 I_{OL}	2	13.5	18.0	14.0	18.0	14.0	19.0	mAdc
Threshold Current High	Logic 1 I_{OHC}	2		2.0		2.0		2.0	mAdc
Threshold Current Low	Logic 0 I_{OLC}	2	13.5		14.0		14.0		mAdc
Output Sink Current Low	Logic 0 I_{OS}	2	13.3		13.9		13.3		mAdc
Load Return Voltage Absolute Max Rating (Note 1.)	V_{LR}			5.5		5.5		5.5	V
Output Voltage Low (Note 2.)	V_{OLS}				-2.4				V
Switching Times (50 Ω Load)									ns
Propagation Delay \bar{E} to Output	t_{PHL}				2.0	6.0			
Propagation Delay D to Output	t_{PLH}				1.5	4.5			
Rise/Fall Time (20 to 80%)	t_{TLH} t_{THL}					3.3			

1. The 5.5V value is a maximum rating, do not exceed. A 270 Ω resistor will prevent output transistor breakdown.
2. Limitations of load resistor and load return voltage combinations. Refer to page 1 description.

ELECTRICAL CHARACTERISTICS (continued)

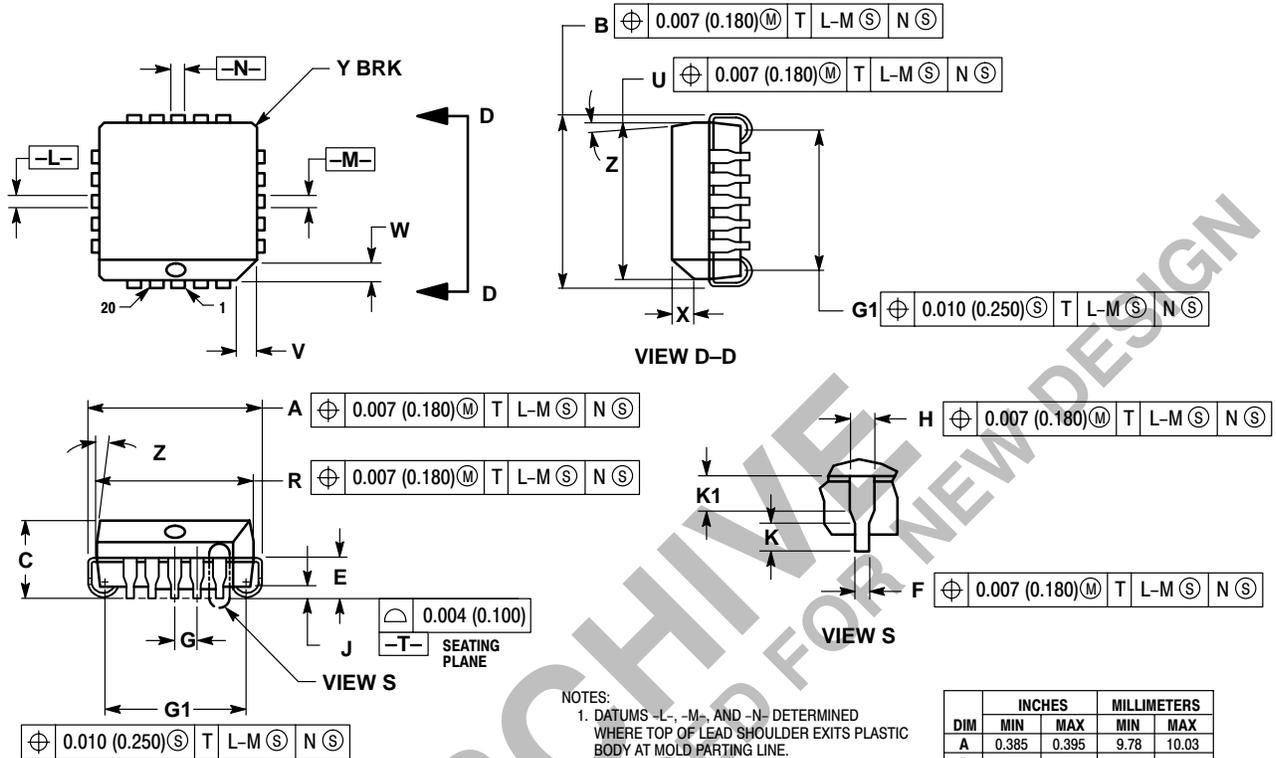
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE VALUES (Volts)					V_{CC} Gnd	
			@ Test Temperature						
			V_{IHmax}	V_{ILmin}	V_{IHamin}	V_{ILAmax}	V_{EE}		
			-30°C	-0.890	-1.890	-1.205	-1.500		-5.2
			+25°C	-0.810	-1.850	-1.105	-1.475		-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2				
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V_{IHmax}	V_{ILmin}	V_{IHamin}	V_{ILAmax}	V_{EE}		
Power Supply Drain Current	I_E	8					8	16	
Input Current	I_{inH}	5	5				8	16	
	I_{inL}	5		5			8	16	
Output Current High	Logic 1 I_{OH}	2		5,6,10,11			8	16	
Output Current Low	Logic 0 I_{OL}	2	5,6,10,11				8	16	
Threshold Current High	Logic 1 I_{OHC}	2		5,7,9,10,11		6	8	16	
Threshold Current Low	Logic 0 I_{OLC}		5,10,11	7,9	6		8	16	
Output Sink Current Low	Logic 0 I_{OS}	2	5,6,10,11				8	16	
Load Return Voltage Absolute Max Rating (Note 1.)	V_{LR}						8	16	
Output Voltage Low (Note 2.)	V_{OLS}						8	16	

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10192

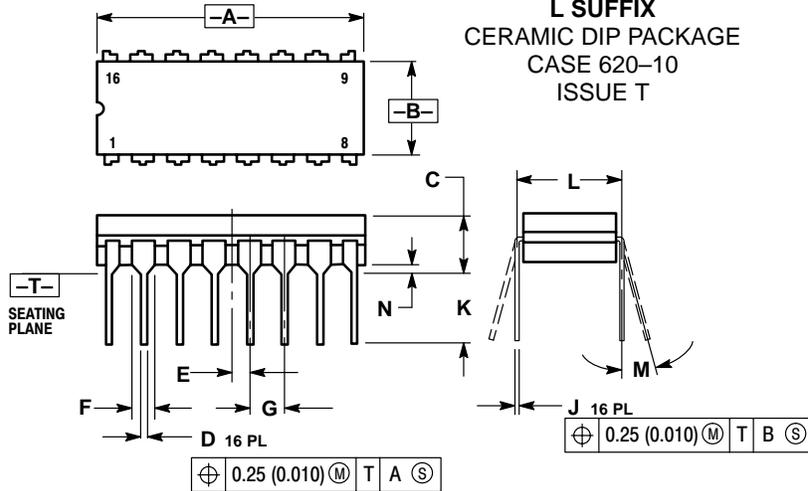
PACKAGE DIMENSIONS

PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



MC10192

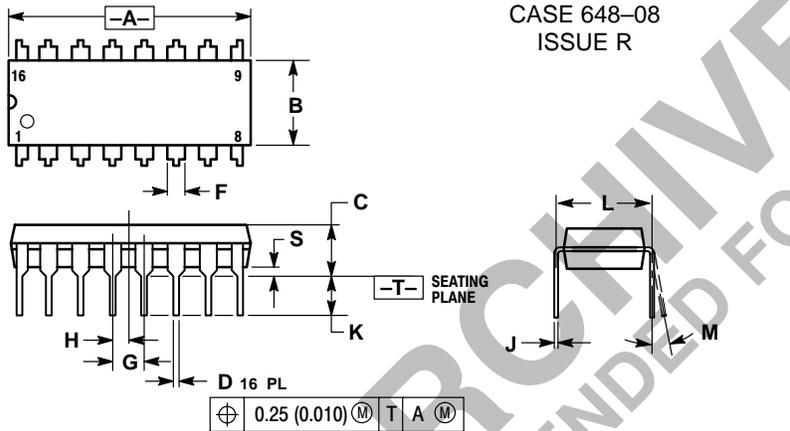
CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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