19-0252; Rev 2; 5/96

MAXIM

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX512/MAX513 contain three 8-bit, voltage-output digital-to-analog converters (DAC A, DAC B, and DAC C). Output buffer amplifiers for DACs A and B provide voltage outputs while reducing external component count. The output buffer for DAC A can source or sink 5mA to within 0.5V of V_{DD} or V_{SS}. The buffer for DAC B can source or sink 0.5mA to within 0.5V of V_{DD} or V_{SS}. DAC C is unbuffered, providing a third voltage output with increased accuracy. The MAX512 operates with a single +5V ±10% supply, and the MAX513 operates with a +2.7V to +3.6V supply. Both devices can also operate with split supplies.

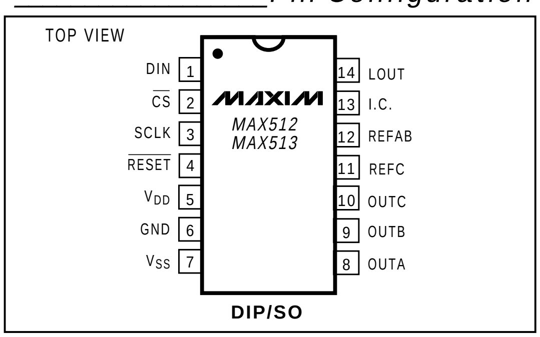
The 3-wire serial interface has a maximum operating frequency of 5MHz and is compatible with SPI™, QSPI™, and Microwire™. The serial input shift register is 16 bits long and consists of 8 bits of DAC input data and 8 bits for DAC selection and shutdown. DAC registers can be loaded independently or in parallel at the positive edge of $\overline{CS}$. A latched logic output is also available for auxiliary control.

Ultra-low power consumption and small packages (14-pin DIP/SO) make the MAX512/MAX513 ideal for portable and battery-powered applications. Supply current is only 1mA, dropping to less than 1µA in shutdown. Any of the three DACs can be independently shut down. In shutdown mode, the DAC's R-2R ladder network is disconnected from the reference input, minimizing system power consumption.

Applications

Digital Gain and Offset Adjustment
Programmable Attenuators
Programmable Current Sources
Programmable Voltage Sources
RF Digitally Adjustable Bias Circuits
VCO Tuning

Pin Configuration



Features

- ♦ **Operate from a Single +5V (MAX512) or +3V (MAX513) Supply, or from Bipolar Supplies**
- ♦ **Low Power Consumption**
  - **1mA Operating Current**
  - **<1µA Shutdown Current**
- ♦ **Unipolar or Bipolar Outputs**
- ♦ **5MHz, 3-Wire Serial Interface**
- ♦ **SPI, QSPI, and Microwire Compatible**
- ♦ **Two Buffered, Bipolar-Output DACs (DACs A/B)**
- ♦ **Independently Programmable Shutdown Mode**
- ♦ **Space-Saving 14-Pin SO/DIP Packages**
- ♦ **Pin and Software Reset**

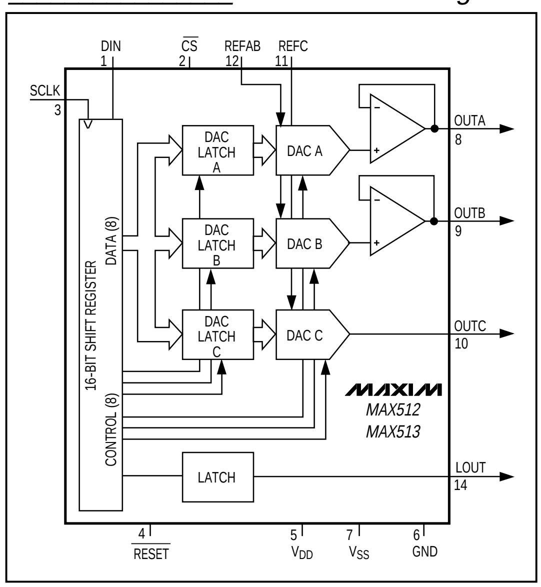
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX512CPD	0°C to +70°C	14 Plastic DIP
MAX512CSD	0°C to +70°C	14 SO
MAX512C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

* *Contact factory for dice specifications.*

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... -0.3V, +6V
V_{SS} to GND.. -6V, +0.3V
V_{DD} to V_{SS} .... -0.3V, +12V
Digital Inputs and Outputs to GND............... -0.3V, (V_{DD} + 0.3V)
REFAB .... (V_{SS} - 0.3V), (V_{DD} + 0.3V)
OUTA, OUTB (Note 1)...V_{SS}, V_{DD}
OUTC..-0.3V, (V_{DD} + 0.3V)
REFC...-0.3V, (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.33mW/°C above +70°C)...........................667mW
CERDIP (derate 9.09mW/°C above +70°C)...................727mW
Operating Temperature Ranges
MAX51_C_ _ ....0°C to +70°C
MAX51_E_ _..-40°C to +85°C
MAX51_MJD ....-55°C to +125°C
Storage Temperature Range.............................-65°C to +165°C
Lead Temperature (soldering, 10sec).............................+300°C

Note 1: The outputs may be shorted to V_{DD}, V_{SS}, or GND if the package power dissipation is not exceeded. Typical short-circuit current to GND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, REFAB = REFC = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Integral Nonlinearity	INL	DAC A/B (Note 2)			±1.5	LSB
		DAC C			±1	
Total Unadjusted Error	TUE	(Note 2)		±1		LSB
Zero-Code Temperature Coefficient		DAC A/B		100		µV/°C
		DAC C		5		
Power-Supply Rejection Ratio	PSRR	MAX512, 4.5V ≤ V_{DD} ≤ 5.5V, REFAB = REFC = 4.096V		0.01		%/%
		MAX513, 2.7V ≤ V_{DD} ≤ 3.6V, REFAB = REFC = 2.4V		0.015		
REFERENCE INPUTS						
Reference Input Voltage Range		REFAB	V_{SS}		V_{DD}	V
		REFC	GND		V_{DD}	
Reference Input Capacitance				25		pF
Reference Input Resistance	R_{REF}	REFAB (Note 3)	8			kΩ
		REFC (Note 3)	12			
Reference Input Resistance (shutdown mode)		REFAB, REFC		2		MΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, REFAB = REFC = V_{DD}, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC OUTPUTS							
Output Voltage Range				0		REF_	V
Capacitive Load		DAC A		0.10			µF
		DAC B		0.01			
		DAC C		0			
Output Resistance		DAC A			0.050		kΩ
		DAC B			0.500		
		DAC C			24		
DIGITAL INPUTS							
Input High Voltage	V_{IH}			(0.7)(V_{DD})			V
Input Low Voltage	V_{IL}					(0.3)(V_{DD})	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			0.1	±10	µA
Input Capacitance	C_{IN}	(Notes 4, 5)				10	pF
DIGITAL OUTPUT							
Output High Voltage	V_{OH}	I_{SOURCE} ≤ 1.6mA		V_{DD} - 0.4			V
Output Low Voltage	V_{OL}	I_{SINK} ≤ 1.6mA				0.4	V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	C_L = 0.1µF (DAC A), C_L = 0.01µF (DAC B)			0.1		V/µs
Voltage-Output Settling Time		To ±½LSB	C_L = 0.1µF (DAC A)		70		µs
			C_L = 0.01µF (DAC B)		70		
			C_L = 0.1nF (DAC C)		35		
Digital Feedthrough and Crosstalk		All 0s to all 1s			10		nV-s
POWER SUPPLIES							
Positive Supply Voltage Range	V_{DD}	MAX512		4.5		5.5	V
		MAX513		2.7		3.6	
Negative Supply Voltage Range (Note 6)	V_{SS}	MAX512		-5.5		-4.5	V
		MAX513		-3.6		-2.7	
Positive Supply Current	I_{DD}	All inputs = 0V	MAX512 (V_{DD} = 5.5V)		1.3	2.8	mA
			MAX513 (V_{DD} = 3.6V)		0.9	2.5	
Negative Supply Current	I_{SS}	All inputs = 0V, V_{SS} = -5.5V			-1.3		mA
Shutdown Supply Current					0.1		µA

Note 2: Digital code from 24 through 232 are due to swing limitations of output amplifiers on DAC A and DAC B. See *Typical Operating Characteristics*.
Note 3: Reference input resistance is code dependent. The lowest input resistance occurs at code 55hex. Refer to the reference input section in the *Detailed Description*.
Note 4: Guaranteed by design. Not production tested.
Note 5: Input capacitance is code dependent. The highest capacitance occurs at code 00hex.
Note 6: For single-supply mode, tie V_{SS} to GND.

TIMING CHARACTERISTICS (Note 4)

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

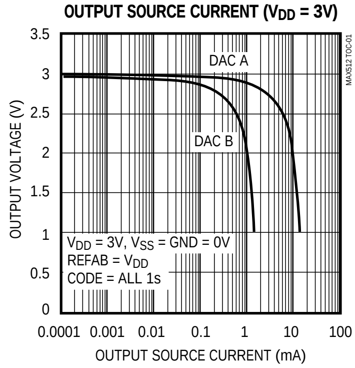
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING						
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		150			ns
SCLK Rise to $\overline{CS}$ Rise Setup Time	t_{CSH}		150			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		50			ns
SCLK Pulse Width High	t_{CH}		100			ns
SCLK Pulse Width Low	t_{CL}		100			ns
Output Delay LOUT	t_{OD}	C_L = 100pF			150	ns
$\overline{CS}$ Pulse Width High	t_{CSPWH}		200			ns

Note 4: Guaranteed by design. Not production tested.

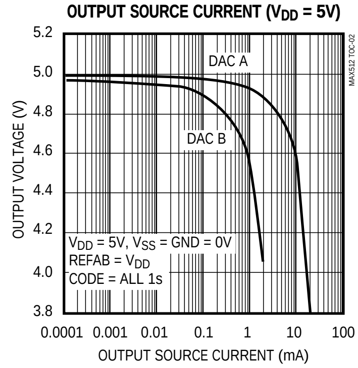
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

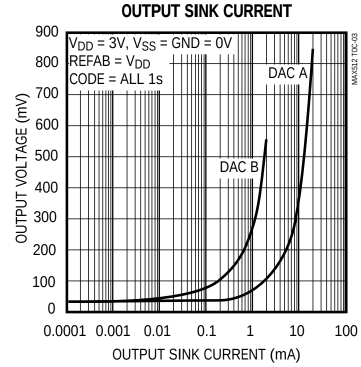
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 3V)



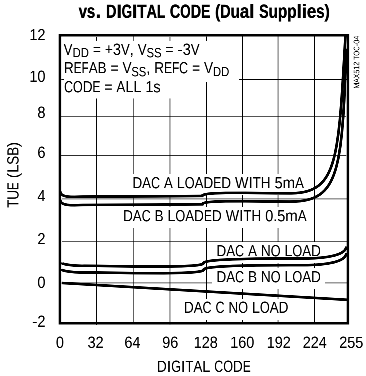
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 5V)



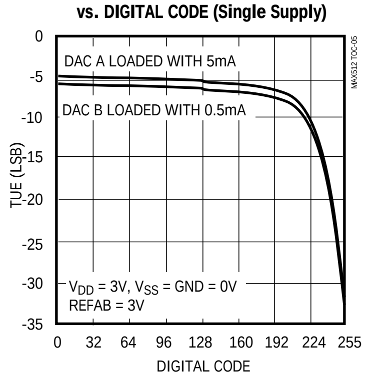
OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



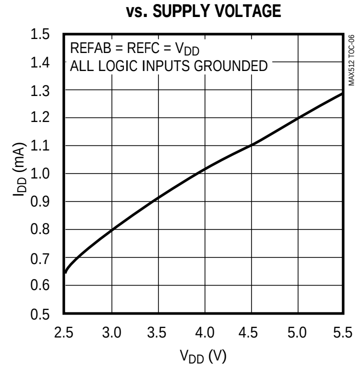
TOTAL UNADJUSTED ERROR vs. DIGITAL CODE (Dual Supplies)



TOTAL UNADJUSTED ERROR vs. DIGITAL CODE (Single Supply)



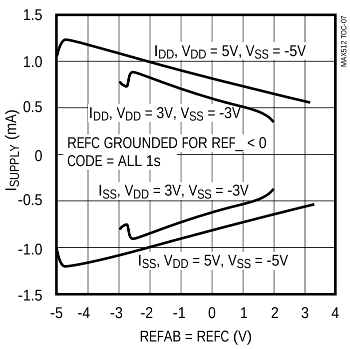
POSITIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



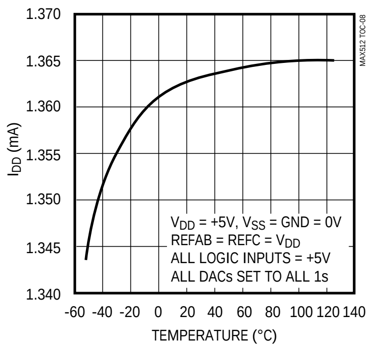
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

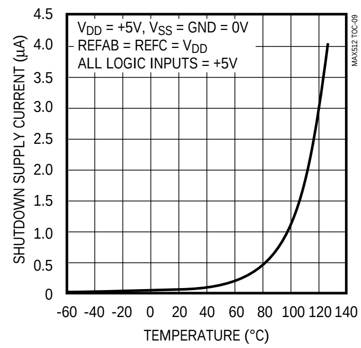
SUPPLY CURRENT vs. REFERENCE VOLTAGE



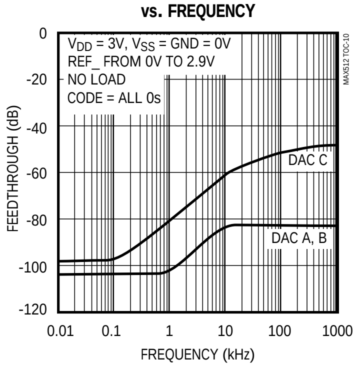
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



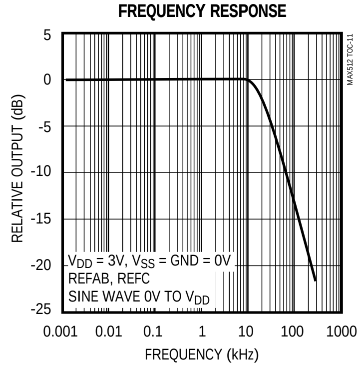
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



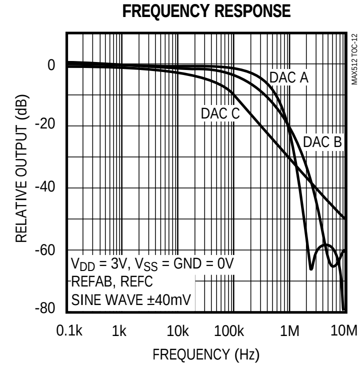
REFERENCE FEEDTHROUGH vs. FREQUENCY



REFERENCE LARGE-SIGNAL FREQUENCY RESPONSE



REFERENCE SMALL-SIGNAL FREQUENCY RESPONSE

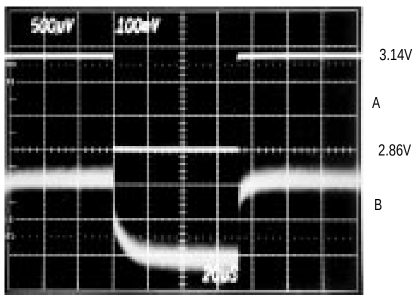


Low-Cost, Triple, 8-Bit Voltage Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

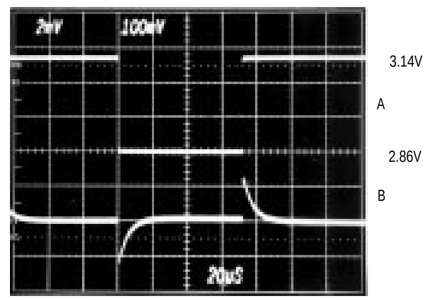
LINE-TRANSIENT RESPONSE (OUTA)



20µs/div

REFAB = 2.56V, NO LOAD, CODE = ALL 1s
A : V_{DD}, 100mV/div
B : OUTA, 500µV/div

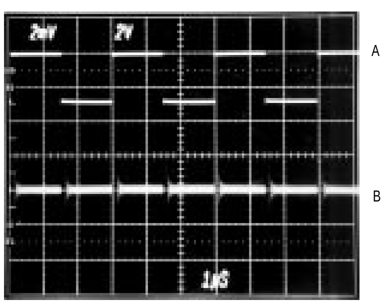
LINE-TRANSIENT RESPONSE (OUTC)



20µs/div

REFC = 2.56V, NO LOAD, CODE = ALL 1s
A : V_{DD}, 100mV/div
B : OUTC, 2mV/div

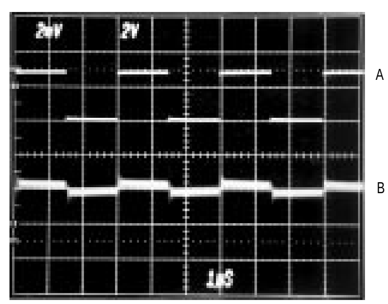
CLOCK FEEDTHROUGH (OUTA)



1µs/div

V_{SS} = 0V, $\overline{CS}$ = HIGH
A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
B: OUTA, 2mV/div

CLOCK FEEDTHROUGH (OUTC)



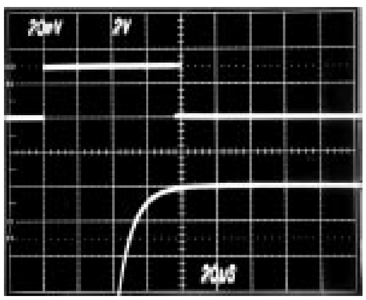
1µs/div

V_{SS} = 0V, $\overline{CS}$ = HIGH
A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
B: OUTC, 2mV/div

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

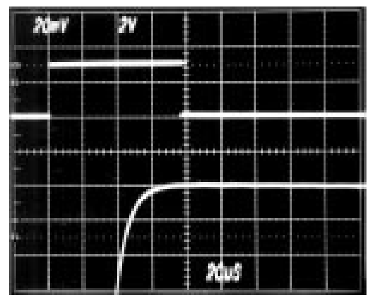
POSITIVE SETTLING TIME (DAC A)



20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 1k Ω, C_L = 0.1µF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 2V/div
B: OUTA, 20mV/div

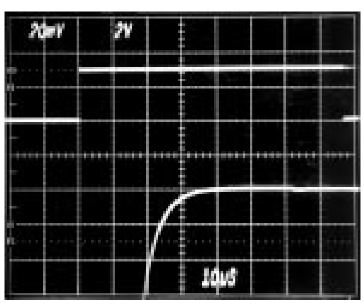
POSITIVE SETTLING TIME (DAC B)



20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 10k Ω, C_L = 0.01µF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 2V/div
B: OUTB, 20mV/div

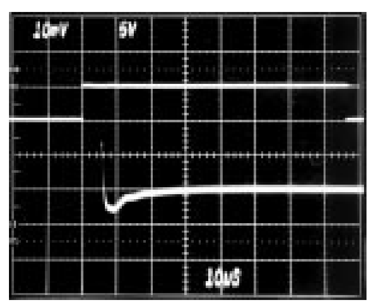
POSITIVE SETTLING TIME (DAC C)



10µs/div

V_{DD} = 3V, V_{SS} = 0V, REFC = V_{DD}, R_L = ∞, C_L = 122pF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 2V/div
B: OUTC, 20mV/div

POSITIVE SETTLING TIME WITH DUAL SUPPLIES



10µs/div

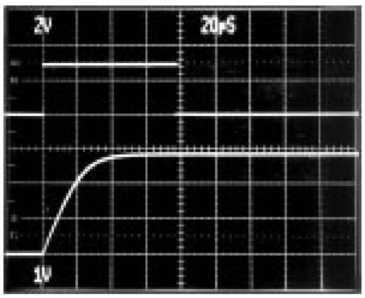
V_{DD} = 5V, V_{SS} = -5V, REFAB = 2.56V, R_L = 1k Ω, C_L = 0.1µF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 5V/div
B: OUTA, 10mV/div

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

TIME EXITING SHUTDOWN MODE



A

B

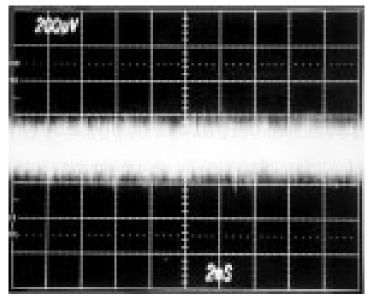
20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 1k Ω, C_L = 0.1µF
DAC LOADED WITH ALL 1s

A: $\overline{CS}$, 2V/div

B: OUTA, 1V/div

OUTPUT VOLTAGE NOISE DC TO 1MHz



OUTA,
200µV/div

2ms/div

DIGITAL CODE = 80, REFAB = V_{DD}, NO LOAD

Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial Data Input of the 16-bit shift register. Data is clocked into the register on the rising edge of SCLK.
2	$\overline{CS}$	Chip Select (active low). Enables data to be shifted into the 16-bit shift register. Programming commands are executed at the rising edge of $\overline{CS}$.
3	SCLK	Serial Clock Input. Data is clocked in on the rising edge of SCLK.
4	$\overline{RESET}$	Asynchronous reset input (active low). Clears all registers to their default state (FFhex for DAC A and DAC B registers); all other registers are reset to 0 (including the input shift register).
5	V_{DD}	Positive Power Supply (2.7V to 5.5V). Bypass with 0.22µF to GND.
6	GND	Ground
7	V_{SS}	Negative Power Supply 0V or (-1.5V to -5.5V). Tie to GND for single supply operation. If a negative supply is applied, bypass with 0.22µF to GND.
8	OUTA	DAC A Output Voltage (Buffered). Resets to full scale. **Connect 0.1µF capacitor or greater to GND.**
9	OUTB	DAC B Output Voltage (Buffered). Resets to full scale. **Connect 0.01µF capacitor or greater to GND.**
10	OUTC	DAC C Output Voltage (Unbuffered). Resets to zero.
11	REFC	DAC C Reference Voltage
12	REFAB	DAC A/B Reference Voltage
13	I.C.	Internally connected. Do not make connections to this pin.
14	LOUT	Logic Output (latched)

Detailed Description

Analog Section

The MAX512/MAX513 contain three 8-bit, voltage-output, digital-to-analog converters (DACs). The DACs are “inverted” R-2R ladder networks using complementary switches that convert 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltages.

The MAX512/MAX513 have two reference inputs: one is shared by DAC A and DAC B and the other is used by DAC C. These inputs allow different full-scale output voltages and different output voltage polarities for the DAC pair A/B and DAC C.

The MAX512/MAX513 include output buffer amplifiers for DACs A and B and input logic for simple microprocessor (µP) and CMOS interfaces.

The MAX512/MAX513 operate in either single-supply or dual-supply mode, as determined by V_{SS}. If V_{SS} is within approximately -0.5V of GND, single-supply mode is assumed. If V_{SS} is below -1.5V, the devices are in dual-supply mode.

Reference Inputs and DAC Output Range

The voltage at REF_ sets the full-scale output of the DACs. The input impedance of the REF_ inputs is code dependent. The lowest value, approximately 12kΩ for REFC (8kΩ for REFAB), occurs when the input code is 01010101 (55hex). The maximum value of infinity occurs when the input code is zero.

In shutdown mode, the selected DAC output is set to zero while the value stored in the DAC register remains unchanged. This removes the load from the reference input to save power. Bringing the MAX512/MAX513 out of shutdown mode restores the DAC output voltage. Because the input resistance at REF_ is code dependent, the DAC’s reference sources should have an output impedance of no more than 5Ω. The input capacitance at the REF_ pins is also code dependent and typically does not exceed 25pF.

The reference voltage on REFAB can range anywhere between the supply rails. In dual-supply mode, a positive reference input voltage on REFAB should be less than (V_{DD} - 1.5V) to avoid saturating the buffer amplifiers. The reference voltage includes the negative supply rail. See the *Output Buffer Amplifier* section for more information. The REFC input accepts positive voltages up to V_{DD} and should not be forced below ground.

The absolute difference between any reference voltage and GND should not exceed 6V.

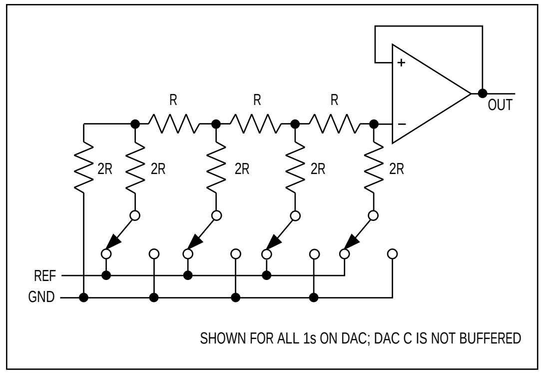


Figure 1. DAC Simplified Circuit Diagram

Output Buffer Amplifiers (DAC A / DAC B)

DAC A and DAC B voltage outputs are internally buffered. The buffer amplifiers have a rail-to-rail (V_{SS} to V_{DD}) output voltage range.

In single-supply mode, the DAC outputs A and B are internally divided by two and the buffer is set to a gain of two, eliminating the need for a buffer input voltage range to the positive supply rail.

In dual-supply mode, the DAC outputs are not attenuated and the buffer is set to unity gain.

Although only necessary for negative output voltages, the dual-supply mode may be used even if the desired DAC output voltage is positive. Possible errors associated with the divide-by-two attenuator and gain-of-two buffers in single-supply mode are eliminated in dual-supply mode. In this case, do not use reference voltages higher than (V_{DD} - 1.5V).

DAC A’s output amplifier can source and sink up to 5mA of current (0.5mA for DAC B buffer). See the Total Unadjusted Error vs. Digital Code graph in the *Typical Operating Characteristics* for dual and single supplies. The amplifier is unity-gain stable with a capacitive load of 0.05µF (0.01µF for DAC B buffer) or greater. The slew rate is limited by the load capacitor and is typically 0.1V/µs with a 0.1µF load (0.01µF for DAC B buffer).

Unbuffered Output (DAC C)

The output of DAC C is unbuffered and has a typical output impedance of 24kΩ. It can be used to drive a high-impedance load, such as an op amp or comparator, and has 35µs typical settling time to 1/2LSB with a single 3V supply. Use DAC C if a quick dynamic response is required.

Shutdown Mode

When programmed to shutdown mode, the outputs of DAC A and B go into a high-impedance state. Virtually no current flows into or out of the buffer amplifiers in that state. The output of DAC C goes to 0V when shut down. In shutdown mode, the REF_ inputs are high impedance (2MΩ typ) to conserve current drain from the system reference; therefore, the system reference does not have to be powered down. The logic output LOUT remains active in shutdown.

Coming out of shutdown, the DAC outputs return to the values kept in the registers. The recovery time is equivalent to the DAC settling time.

Reset

The RESET input is active low. When asserted (RESET = 0), DACs A and B are set to full scale (FFhex) and active, while DAC C is set to zero code (00hex) and active. The 16-bit serial register is cleared to 0000hex. LOUT is reset to zero.

Serial Interface

An active-low chip select (CS) enables the shift register to receive data from the serial data input. Data is clocked into the shift register on every rising edge of the serial clock signal (SCLK). The clock frequency can be as high as 5MHz.

Data is sent MSB first and can be transmitted in one 16-bit word. The write cycle can be interrupted at any time when CS is kept active (low) to allow, for example, two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, the rising edge of CS updates the DAC outputs, the shutdown status, and the status of the logic output. Because of their single buffered structure, DACs cannot be simultaneously updated to different digital values.

Table 1. Input Shift Register

DATA BITS	B0*	DAC Data Bit 0 (LSB)
	B1	DAC Data Bit 1
	B2	DAC Data Bit 2
	B3	DAC Data Bit 3
	B4	DAC Data Bit 4
	B5	DAC Data Bit 5
	B6	DAC Data Bit 6
	B7	DAC Data Bit 7 (MSB)
CONTROL BITS	LA	Load Reg DAC A, Active High
	LB	Load Reg DAC B, Active High
	LC	Load Reg DAC C, Active High
	SA	Shut Down DAC A, Active High
	SB	Shut Down DAC B, Active High
	SC	Shut Down DAC C, Active High
	Q1	Logic Output
	Q2**	Uncommitted Bit

* Clocked in last.
**Clocked in first.

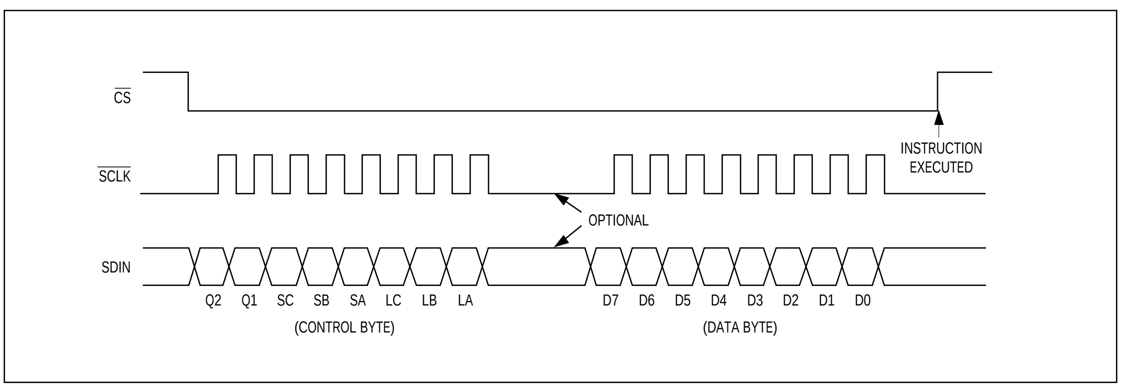


Figure 2. MAX512/MAX513 3-Wire Serial-Interface Timing Diagram

Table 2. Serial-Interface Programming Commands

CONTROL								DATA								FUNCTION
								MSB							LSB	
Q2	Q1	SC	SB	SA	LC	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0	
*	*	*	*	*	0	0	0	X	X	X	X	X	X	X	X	No Operation to DAC Registers
*	*	*	*	*	1	0	0	8-Bit DAC Data								Load Register to DAC C
*	*	*	*	*	0	1	0	8-Bit DAC Data								Load Register to DAC B
*	*	*	*	*	0	0	1	8-Bit DAC Data								Load Register to DAC A
*	*	*	*	*	1	1	1	8-Bit DAC Data								Load All DAC Registers
*	*	0	0	0	*	*	*	X	X	X	X	X	X	X	X	All DACs Active
*	*	1	0	0	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC C
*	*	0	1	0	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC B
*	*	0	0	1	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC A
*	*	1	1	1	*	*	*	X	X	X	X	X	X	X	X	Shut Down All DACs
X	0	*	*	*	*	*	*	X	X	X	X	X	X	X	X	Reset LOUT
X	1	*	*	*	*	*	*	X	X	X	X	X	X	X	X	Set LOUT

X *Don't care.*

* *Not shown for clarity. The functions of loading and shutting down the DACs and programming the logic can be combined in a single command.*

Serial-Input Data Format and Control Codes

Table 2 lists the serial-input data format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally. Every control bit performs one function. Data is clocked in starting with Q2 (uncommitted bit), followed by the remaining control bits and the data byte. The LSB of the data byte (B0) is the last bit clocked into the shift register (Figure 2).

Example of a 16-bit input word:

Loaded in First															Loaded in Last
Q2	Q1	SC	SB	SA	LC	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0
X	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0

The example above performs the following functions:

- 80hex (128 decimal) loaded into DAC registers A and B.
- Content of the DAC C register remains unchanged.
- DAC A and DAC B are active.
- DAC C is shut down.
- LOUT is reset to 0.

Digital Inputs

The digital inputs are compatible with CMOS logic. Supply current increases slightly when toggling the logic inputs through the transition zone between $(0.3)(V_{DD})$ and $(0.7)(V_{DD})$.

Digital Output

The latched digital output (LOUT) has a 1.6mA source capability while maintaining a $(V_{DD}$ - 0.4V) output level. With a 1.6mA sink current, the output voltage is guaranteed to be no more than 0.4V. The output can be used for digital auxiliary control. Please note that the digital output remains fully active during shutdown mode.

Microprocessor Interfacing

The MAX512/MAX513 serial interface is compatible with Microwire, SPI, and QSPI. For SPI and QSPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the inactive state of clock to zero and CPHA = 0 changes data at the falling edge of SCLK. This setting allows both SPI and QSPI to run at full clock speeds (0.5MHz and 4MHz, respectively). If a serial port is not available on your µP, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the voltage outputs by operating the serial clock only when necessary.

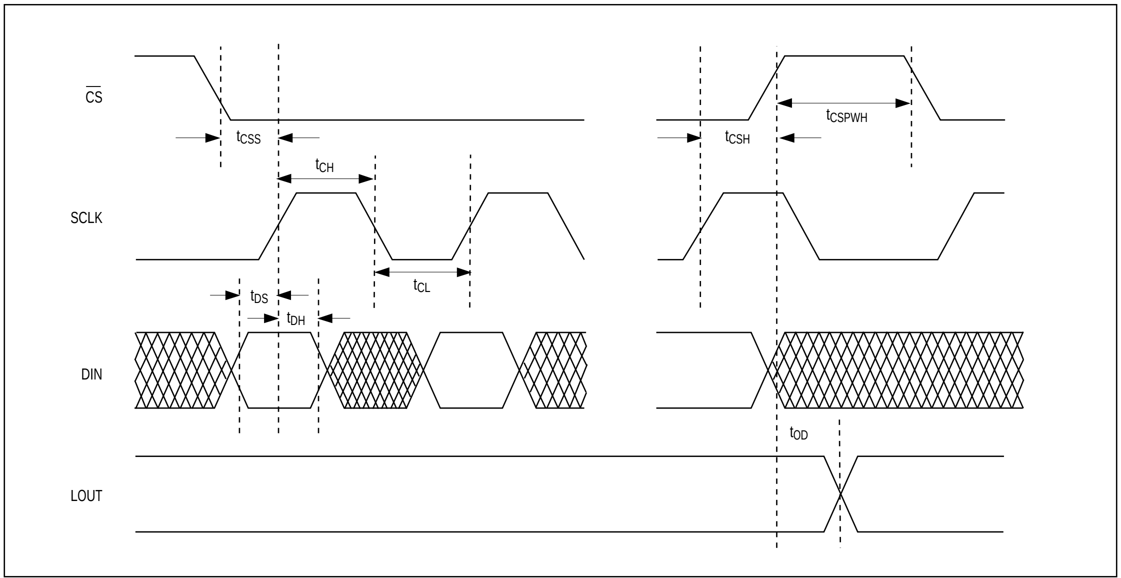


Figure 3. MAX512/MAX513 Detailed Serial-Interface Timing Diagram

Applications Information

Power-Supply and Reference Operating Ranges

The MAX512 is fully specified to operate with V_{DD} = 5V ±10% and V_{SS} = GND = 0V. The MAX513 is specified for single-supply operation with V_{DD} ranging from 2.7V to 3.6V, covering all commonly used supply voltages in 3V systems. The MAX512/MAX513 can also be used with a negative supply ranging from -1.5V to -5.5V. Using a negative supply typically improves zero-code error and settling time (as shown in the *Typical Operating Characteristics* graphs).

The two separate reference inputs for the DAC pair A/B and the unbuffered output C allow different full-scale output voltages and, if a negative supply is used, also allow different polarity. In dual-supply mode, REFAB can vary from V_{SS} to (V_{DD} - 1.5V). In single-supply mode, the specified range for REFAB is 0V to V_{DD}. REFC can range from GND to V_{DD}. Do not force REFC below ground.

Power-supply sequencing is not critical. If a negative supply is used, make sure V_{SS} is never more than 0.3V above ground. Do not apply signals to the digital inputs until the device is powered-up. If this is not possible, add current-limiting resistors to the digital inputs.

Power-Supply Bypassing and Ground Management

In single-supply operation (V_{SS} = GND), GND and V_{SS} should be connected to the highest quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. For dual-supply operation, bypass V_{SS} with a 0.1µF to 0.22µF capacitor to GND. Reference inputs can be used without bypassing. For optimum line/load-transient response and noise performance, bypass the reference inputs with 0.1µF to 4.7µF to GND. Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Separate analog lines with ground traces between them. Make sure that high-frequency digital lines are not routed in parallel to analog lines.

Unipolar Output

With unipolar output, the output voltage and the reference voltage are the same polarity. The MAX512/MAX513 can be used with a single supply if the reference voltages are positive. With a negative supply, the REFAB voltage can vary from V_{SS} to approximately (V_{DD} - 1.5V), allowing two-quadrant multiplication.

Table 3. Unipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+REF\_ \times \left(\frac{128}{256}\right) = +\frac{REF\_}{2}$
0	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

Note :

$$1LSB = REF\_ \times 2^{-8} = REF\_ \times \left(\frac{1}{256}\right)$$

$$ANALOG\ OUTPUT = REF\_ \times \left(\frac{D}{256}\right)$$

Table 4. Bipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-REF\_ \times \left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-REF\_ \times \left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-REF\_ \times \left(\frac{128}{128}\right) = -REF\_$

Note :

$$1LSB = REF\_ \times 2^{-(8-1)} = REF\_ \times \left(\frac{1}{128}\right)$$

$$ANALOG\ OUTPUT = REF\_ \times \left(\frac{D}{128} - 1\right)$$

Bipolar Output

Using Figure 4's circuit, the MAX512/MAX13 can be configured for bipolar outputs. Table 4 lists the bipolar codes and corresponding output voltages. There are two ways to achieve rail-to-rail outputs: 1) Operate the MAX512/MAX513 with a single supply and positive reference voltages or 2) Use dual supplies with a positive or negative voltage at REFAB and a positive voltage at REFC. In either case, the op amps need dual supplies. When using the dual-supply mode, possible errors associated with the divide-by-two attenuator and gain-of-two buffer are eliminated (see the *Output Buffer Amplifier* section). For maximum output swing of all outputs in dual-supply mode, connect REFAB to V_{SS} and REFC to V_{DD}. In single-supply mode, connect REFAB, REFC, and V_{DD} together.

With dual supplies, DACs A and B can perform four-quadrant multiplication. Please note that in dual-supply mode, the REFAB input ranges from V_{SS} to (V_{DD} - 1.5V). Because REFC accepts only positive inputs, DAC C performs two-quadrant multiplication.

Figure 4 shows Maxim's ICL7612A with rail-to-rail input common-mode range and rail-to-rail output voltage swing—ideal for a high output voltage swing from low supply voltages.

RF Applications

Both the MAX512 and MAX513 can bias GaAs FETs, where the gate of the FETs must be negatively biased to ensure that there is no drain current. In a typical application, power to the RF amplifiers should not be turned on until the bias voltages provided by DAC A and DAC B are fully established; likewise, the supply should be turned off before the bias voltage is switched off. Figure 5 shows how DAC B supplies the negative bias V_{GG1} for the driver stage and DAC A provides the negative bias V_{GG2} for the output stage [1].

The DAC A and DAC B outputs are also ideal for controlling VCOs in mobile radios or cellular phones. Other applications include varactor and PIN diode circuits.

The unbuffered DAC C provides a span within GND and V_{DD} and is individually set at REF C. DAC C typically adjusts offset and gain in the system.

1 [John Wachsmann. "A High-Efficiency GaAs MMIC Power Amplifier for 1.9GHz PCS Applications," Proceedings of the First Annual Wireless Symposium, pp. 375, Penton Publishing, Jan. 1993.]

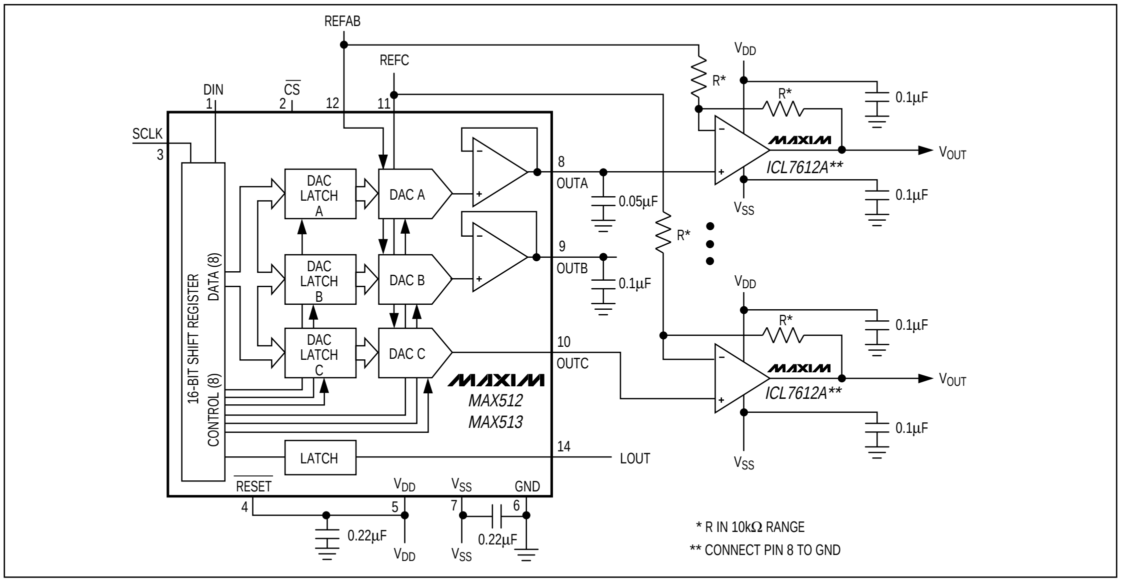


Figure 4. Bipolar Output Circuit

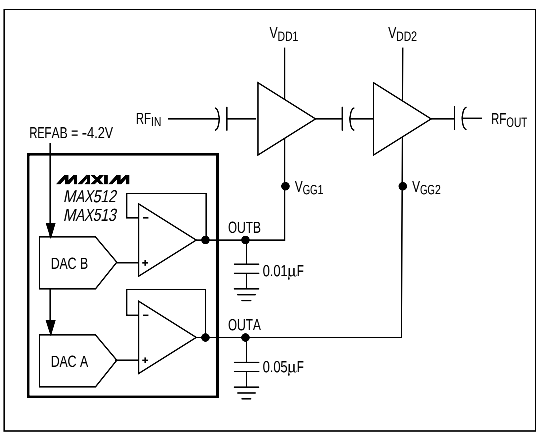


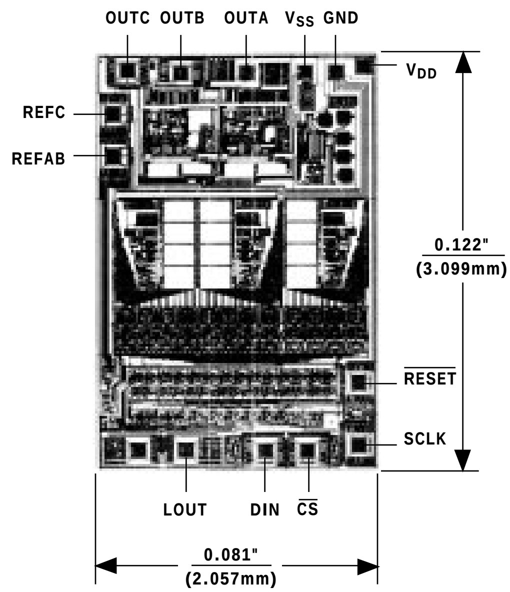
Figure 5. RF Bias Circuit

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX512EPD	-40°C to +85°C	14 Plastic DIP
MAX512ESD	-40°C to +85°C	14 SO
MAX512MJD	-55°C to +125°C	14 CERDIP
MAX513CPD	0°C to +70°C	14 Plastic DIP
MAX513CSD	0°C to +70°C	14 SO
MAX513C/D	0°C to +70°C	Dice*
MAX513EPD	-40°C to +85°C	14 Plastic DIP
MAX513ESD	-40°C to +85°C	14 SO
MAX513MJD	-55°C to +125°C	14 CERDIP

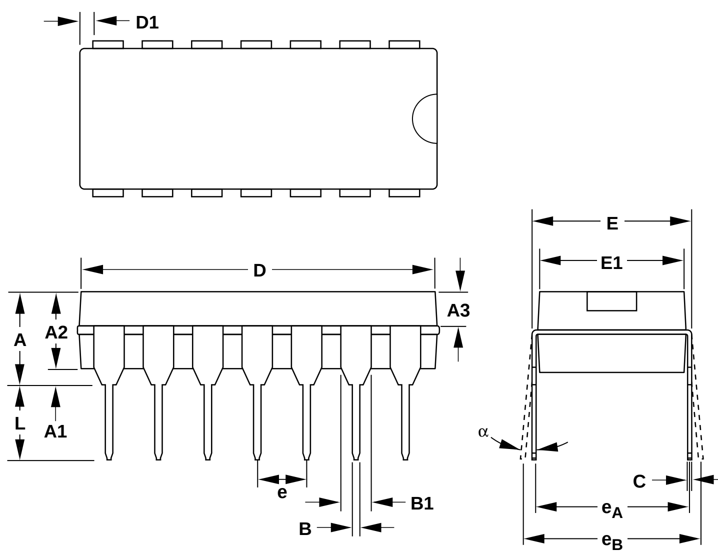
** Contact factory for dice specifications.*

Chip Topography



TRANSISTOR COUNT: 1910
SUBSTRATE CONNECTED TO V_{DD}

Package Information



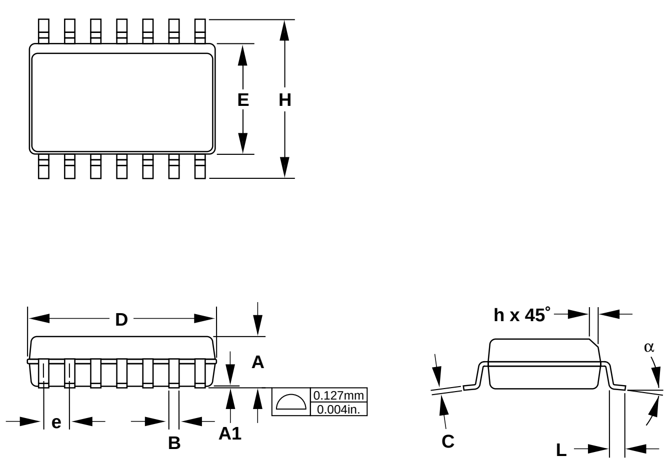
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.735	0.765	18.67	19.43
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-330A

14-PIN PLASTIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-331A



14-PIN PLASTIC SMALL-OUTLINE PACKAGE

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19-0172; Rev 6; 2/97

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

General Description

The MAX531/MAX538/MAX539 are low-power, voltage-output, 12-bit digital-to-analog converters (DACs) specified for single +5V power-supply operation. The MAX531 can also be operated with ±5V supplies. The MAX538/MAX539 draw only 140µA, and the MAX531 (with internal reference) draws only 260µA. The MAX538/MAX539 come in 8-pin DIP and SO packages, while the MAX531 comes in 14-pin DIP and SO packages. All parts have been trimmed for offset voltage, gain, and linearity, so no further adjustment is necessary.

The MAX538's buffer is fixed at a gain of +1 and the MAX539's buffer at a gain of +2. The MAX531's internal op amp may be configured for a gain of +1 or +2, as well as for unipolar or bipolar output voltages. The MAX531 can also be used as a four-quadrant multiplier without external resistors or op amps.

For parallel data inputs, see the MAX530 data sheet.

Applications

Battery-Powered Test Instruments

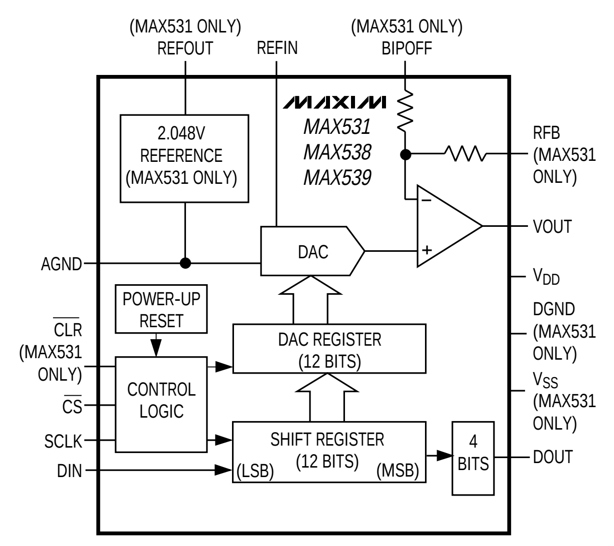
Digital Offset and Gain Adjustment

Battery-Operated/Remote Industrial Controls

Machine and Motion Control Devices

Cellular Telephones

Functional Diagram



Features

- ♦ **Operate from Single +5V Supply**
- ♦ **Buffered Voltage Output**
- ♦ **Internal 2.048V Reference (MAX531)**
- ♦ **140µA Supply Current (MAX538/MAX539)**
- ♦ **INL = ±1/2LSB (max)**
- ♦ **Guaranteed Monotonic over Temperature**
- ♦ **Flexible Output Ranges:**
  - **0V to V_{DD} (MAX531/MAX539)**
  - **V_{SS} to V_{DD} (MAX531)**
  - **0V to 2.6V (MAX531/MAX538)**
- ♦ **8-Pin SO/DIP (MAX538/MAX539)**
- ♦ **Power-On Reset**
- ♦ **Serial Data Output for Daisy-Chaining**

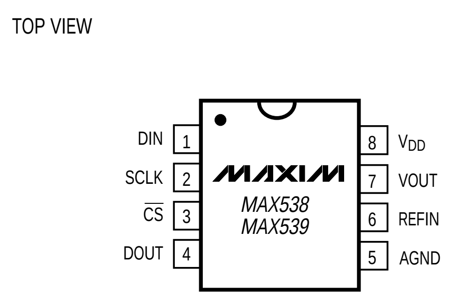
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX531ACPD	0°C to +70°C	14 Plastic DIP	±1/2
MAX531BCPD	0°C to +70°C	14 Plastic DIP	±1
MAX531ACSD	0°C to +70°C	14 SO	±1/2
MAX531BCSD	0°C to +70°C	14 SO	±1
MAX531BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C only.*

Pin Configurations



DIP/SO

Pin Configurations continued at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

+5V, Low-Power, Voltage-Output Serial 12-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND and V_{DD} to AGND ....-0.3V, +6V
V_{SS} to DGND and V_{SS} to AGND ....-6V, +0.3V
V_{DD} to V_{SS} ....-0.3V, +12V
AGND to DGND..-0.3V, +0.3V
Digital Input Voltage to DGND ....-0.3V, (V_{DD} + 0.3V)
REFIN ....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
REFOUT to AGND ....-0.3V, (V_{DD} + 0.3V)
RFB ....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
BIPOFF...(V_{SS} - 0.3V), (V_{DD} + 0.3V)
V_{OUT} (Note 1) ....V_{SS}, V_{DD}
Continuous Current, Any Pin...............................-20mA, +20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)....727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)...800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Ranges
MAX53_ _C_ _ ....0°C to +70°C
MAX53_ _E_ _ ....-40°C to +85°C
Storage Temperature Range ....-65°C to +165°C
Lead Temperature (soldering, 10sec) ....+300°C

Note 1: The output may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation limit is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = +5V ±10%, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT (MAX531), C_{REFOUT} = 33µF (MAX531), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Relative Accuracy (Note 2)	INL	MAX53_AC/E			±0.5	LSB
		MAX53_BC/E			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Offset Error	V_{OS}	MAX53_ _C/E	0		8	LSB
Unipolar Offset Tempco	TCV_{OS}			3		ppm/°C
Gain Error (Note 2)	GE	MAX53_ _C/E			±1	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio (Note 3)	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		0.4	1	LSB/V
VOLTAGE OUTPUT (VOUT)						
Output Voltage Range		MAX531 (G = +1), MAX538	0		V_{DD} - 2	V
		MAX531 (G = +2), MAX539	0		V_{DD} - 0.4	
Output Load Regulation		VOUT = 2V, R_L = 2kΩ			1	LSB
Short-Circuit Current	I_{SC}			12		mA
REFERENCE INPUT (REFIN)						
Voltage Range			0		V_{DD} - 2	V
Input Resistance		Code dependent, minimum at code 555 hex	40			kΩ
Input Capacitance		Code dependent (Note 4)	10		50	pF
AC Feedthrough		REFIN = 1kHz, 2Vp-p		-80		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V_{DD} = +5V ±10%, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT (MAX531), C_{REFOUT} = 33µF (MAX531), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT—MAX531 only)							
Reference Output Voltage		V_{DD} = 5.0V	T_A = +25°C	2.024	2.048	2.072	V
			MAX531BC	2.017		2.079	
			MAX531BE	2.013		2.083	
Temperature Coefficient	TC_{REFOUT}	MAX531AC/AE/AM/BM			30	50	ppm/°C
		MAX531BC/BE			30		
Resistance	R_{REFOUT}	(Note 5)			0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V				300	µV/V
Noise Voltage	e_n	0.1Hz to 10kHz			400		µVp-p
Minimum Required External Capacitor	C_{MIN}			3.3			µF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{CLR}$)							
Input High	V_{IH}			2.4			V
Input Low	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance	C_{IN}				8		pF
DIGITAL OUTPUT (DOUT)							
Output High	V_{OH}	I_{SOURCE} = 2mA		V_{DD} - 1			V
Output Low	V_{OL}	I_{SINK} = 2mA				0.4	V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	T_A = +25°C		0.15	0.25		V/µs
Voltage-Output Settling Time		To ±1/2LSB, VOUT = 2V			25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz			5		nV-s
Signal-to-Noise plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p (G = +1 or +2), code = FFF hex			68		dB
POWER SUPPLY							
Positive Supply Voltage	V_{DD}			4.5		5.5	V
Power-Supply Current	I_{DD}	All inputs = 0V or V_{DD}, output = no load	MAX531		260	400	µA
			MAX538, MAX539		140	300	
SWITCHING CHARACTERISTICS							
$\overline{CS}$ Setup Time	t_{CSS}			20			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}			15			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}			0			ns
SCLK High Width	t_{CH}			35			ns
SCLK Low Width	t_{CL}			35			ns
DIN Setup Time	t_{DS}			45			ns
DIN Hold Time	t_{DH}			0			ns
DOUT Valid Propagation Delay	t_{DO}	C_L = 50pF				80	ns
$\overline{CS}$ High Pulse Width	t_{CSW}			20			ns
$\overline{CLR}$ Pulse Width	t_{CLR}			25			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CS1}			50			ns

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only)

(V_{DD} = +5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution	N			12			Bits
Relative Accuracy	INL	Tested at V_{DD} = 5V, V_{SS} = -5V	MAX531AC/E			±0.5	LSB
			MAX531BC/E			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Bipolar Offset Error	V_{OS}	BIPOFF = REFIN, MAX531_C/E				±8	LSB
Bipolar Offset Tempco	TCV_{OS}	BIPOFF = REFIN			3		ppm/°C
Gain Error (Unipolar or Bipolar)	GEU	MAX531_C/E				±1	LSB
Gain-Error Tempco					1		ppm/°C
Power-Supply Rejection Ratio (Note 3)	PSRR	4.5V ≤ V_{DD} ≤ 5.5V, -5.5V ≤ V_{SS} ≤ -4.5V			0.4	1	LSB/V
REFERENCE INPUT (REFIN)							
Voltage Range				V_{SS} + 2		V_{DD} - 2	V
Input Resistance		Code dependent, minimum at code 555 hex		40			kΩ
Input Capacitance		Code dependent (Note 4)		10		50	pF
AC Feedthrough		REFIN = 1kHz, 2.0Vp-p			-80		dB
REFERENCE OUTPUT (REFOUT—MAX531 only)							
Reference Output Voltage		V_{DD} = 5.0V	T_A = +25°C	2.024	2.048	2.072	V
			MAX531BC	2.017		2.079	
			MAX531BE	2.013		2.083	
Temperature Coefficient	TC_{REFOUT}	MAX531AC/AE/AM/BM			30	50	ppm/°C
		MAX531BC/BE			30		
Resistance	R_{REFOUT}	(Note 5)			0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V				300	µV/V
Noise Voltage	e_n	0.1Hz to 10kHz			400		µVp-p
Minimum Required External Capacitor	C_{MIN}			3.3			µF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)							
Input High	V_{IH}			2.4			V
Input Low	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance	C_{IN}				8		pF
DIGITAL OUTPUT (DOUT)							
Output High	V_{OH}	I_{SOURCE} = 2mA		V_{DD} - 1			V
Output Low	V_{OL}	I_{SINK} = 2mA				0.4	V

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only) (continued)

(V_{DD} = +5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE OUTPUT (VOUT)						
Output Voltage Range		MAX531 (G = +1)	V_{SS} + 2		V_{DD} - 2	V
		MAX531 (G = +2)	V_{SS} + 0.4		V_{DD} - 0.4	
Output Load Regulation		VOUT = 2V, R_L = 2kΩ			1	LSB
Short-Circuit Current	I_{SC}			12		mA
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR		0.15	0.25		V/µs
Voltage-Output Settling Time		To ±1/2LSB, VOUT = 2V		25		µs
Digital Feedthrough		Step 000 hex to FFF hex		5		nV-s
Signal-to-Noise plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p, (G = +1)		68		dB
		REFIN = 1kHz, 2Vp-p, (G = +2)		68		
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Negative Supply Voltage	V_{SS}		-5.5		0	V
Positive Supply Current	I_{DD}	All inputs = 0V or V_{DD}, no load		260	400	µA
Negative Supply Current	I_{SS}	All inputs = 0V or V_{DD}, no load		-120	-200	µA
SWITCHING CHARACTERISTICS						
$\overline{CS}$ Setup Time	t_{CSS}		20			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		15			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
SCLK High Width	t_{CH}		35			ns
SCLK Low Width	t_{CL}		35			ns
DIN Setup Time	t_{DS}		45			ns
DIN Hold Time	t_{DH}		0			ns
DOUT Valid Propagation Delay	t_{DO}	C_L = 50pF			80	ns
$\overline{CS}$ High Pulse Width	t_{CSW}		20			ns
$\overline{CLR}$ Pulse Width	t_{CLR}		25			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CS1}		50			ns

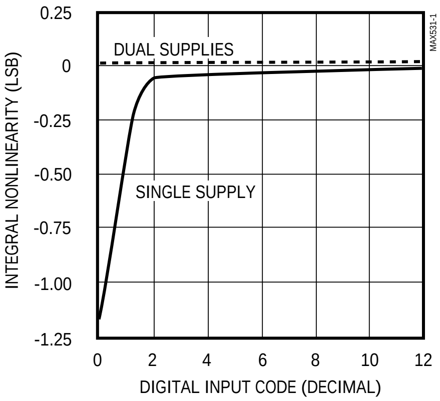
Note 2: In single-supply operation, INL and GE calculated from code 11 to code 4095. Tested at V_{DD} = +5V.
Note 3: This specification applies to both gain-error power-supply rejection ratio and offset-error power-supply rejection ratio.
Note 4: Guaranteed by design.
Note 5: Tested at I_{OUT} = 100µA. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

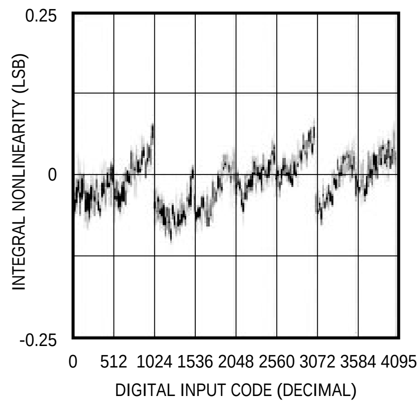
Typical Operating Characteristics

(V_{DD} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted.)

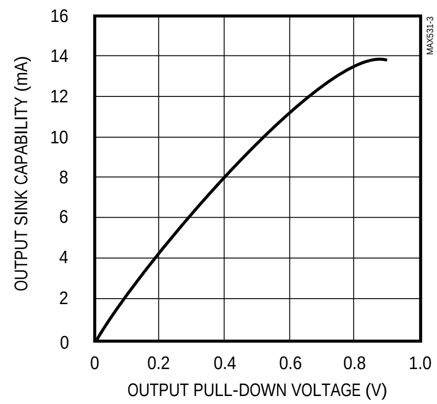
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (FIRST 12 CODES)



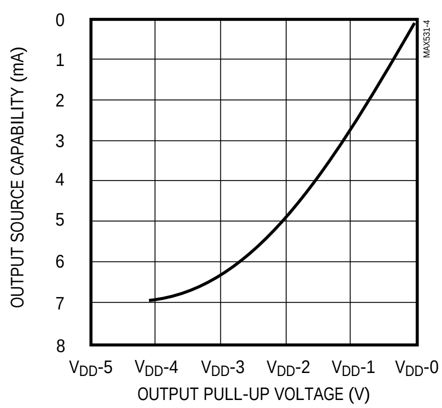
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (ALL CODES)



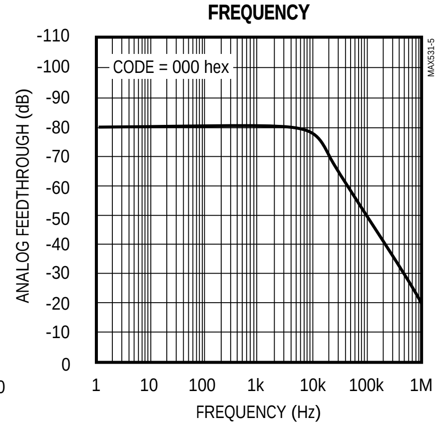
OUTPUT SINK CAPABILITY vs. OUTPUT PULL-DOWN VOLTAGE



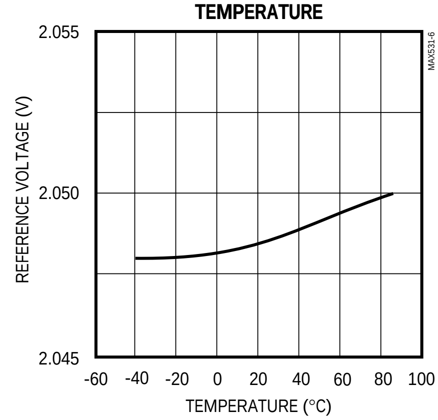
OUTPUT SOURCE CAPABILITY vs. OUTPUT PULL-UP VOLTAGE



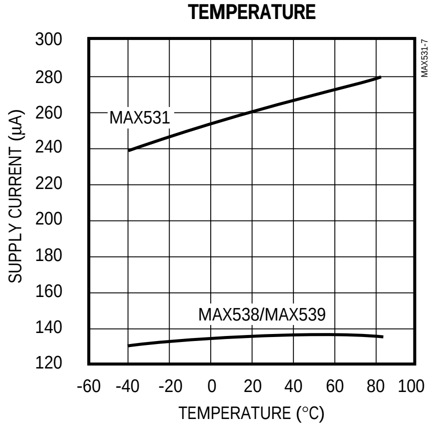
ANALOG FEEDTHROUGH vs. FREQUENCY



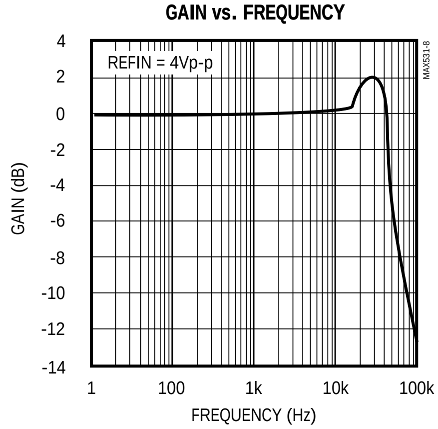
MAX531 REFERENCE VOLTAGE vs. TEMPERATURE



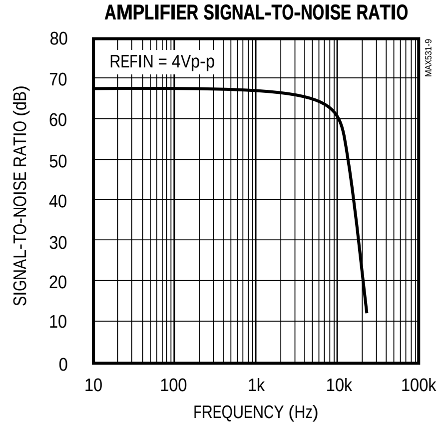
SUPPLY CURRENT vs. TEMPERATURE



MAX531 GAIN vs. FREQUENCY



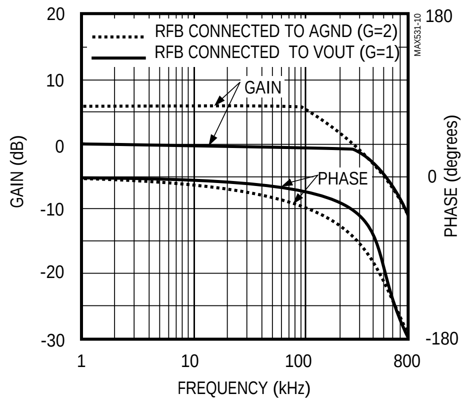
MAX531 AMPLIFIER SIGNAL-TO-NOISE RATIO



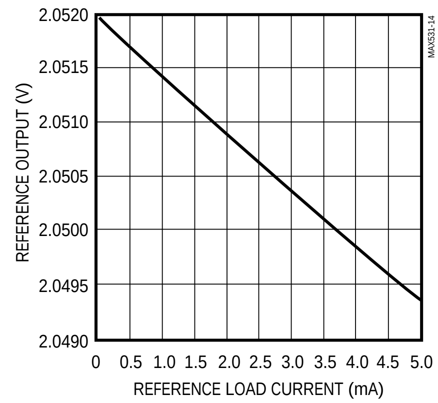
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted.)

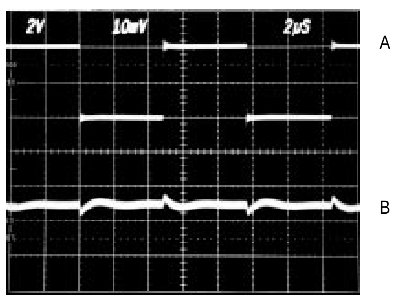
MAX531
GAIN AND PHASE vs. FREQUENCY



MAX531 REFERENCE OUTPUT VOLTAGE
vs. REFERENCE LOAD CURRENT

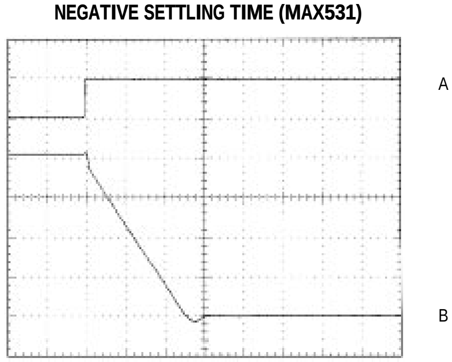


DIGITAL FEEDTHROUGH



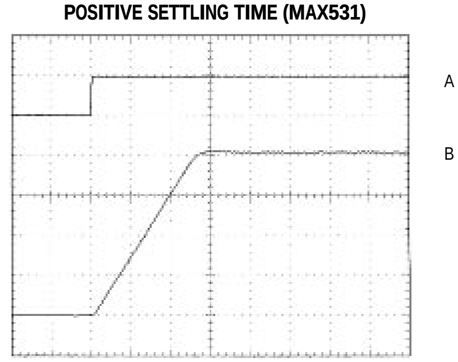
2µs/div
$\overline{CS}$ = HIGH
A: DIN = 4Vp-p, 100kHz
B: VOUT, 10mV/div

NEGATIVE SETTLING TIME (MAX531)



5µs/div
V_{DD} = ±5V, V_{REFIN} = 2V, BIPOLAR CONFIGURATION
A: $\overline{CS}$ RISING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div

POSITIVE SETTLING TIME (MAX531)



5µs/div
V_{DD} = ±5V, V_{REFIN} = 2V, BIPOLAR CONFIGURATION
A: $\overline{CS}$ RISING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div

Pin Description

PIN		NAME	FUNCTION
MAX531	MAX538 MAX539		
1	—	BIPOFF	Bipolar Offset/Gain Resistor
2	1	DIN	Serial Data Input
3	—	$\overline{CLR}$	Clear. Asynchronously sets DAC register to 000 hex.
4	2	SCLK	Serial Clock Input
5	3	$\overline{CS}$	Chip Select, active low
6	4	DOUT	Serial Data Output for daisy-chaining
7	—	DGND	Digital Ground
8	5	AGND	Analog Ground
9	6	REFIN	Reference Input
10	—	REFOUT	Reference Output, 2.048V
11	—	V_{SS}	Negative Power Supply
12	7	VOUT	DAC Output
13	8	V_{DD}	Positive Power Supply
14	—	RFB	Feedback Resistor

Detailed Description

General DAC Discussion

The MAX531/MAX538/MAX539 use an "inverted" R-2R ladder network with a single-supply CMOS op amp to convert 12-bit digital data to analog voltage levels (see *Functional Diagram*). The term "inverted" describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX531/MAX538/MAX539's topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to 000 hex on power-up. Additionally, a clear $\overline{CLR}$ pin, when held low, sets the DAC register to 000 hex. $\overline{CLR}$ operates asynchronously and independently from the chip-select ($\overline{CS}$) pin.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output, BiCMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 12-bit performance. Settling time is 25µs to 0.01% of final value. The settling time is considerably longer when the DAC code is initially set to 000 hex, because at this code the op amp is completely debiased. Start from code 001 hex if necessary. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF load capacitance.

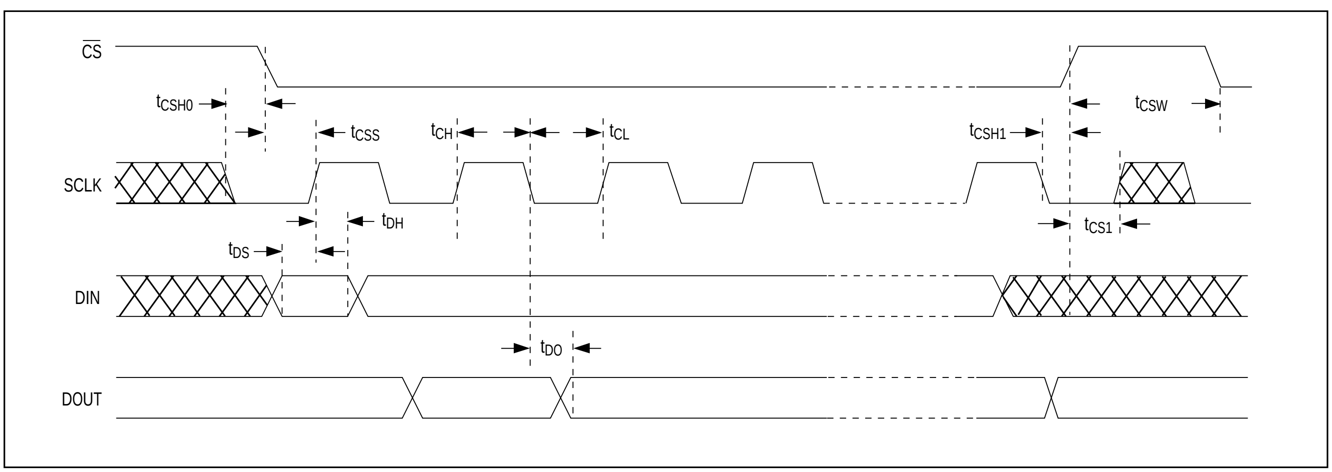


Figure 1. Timing Diagram

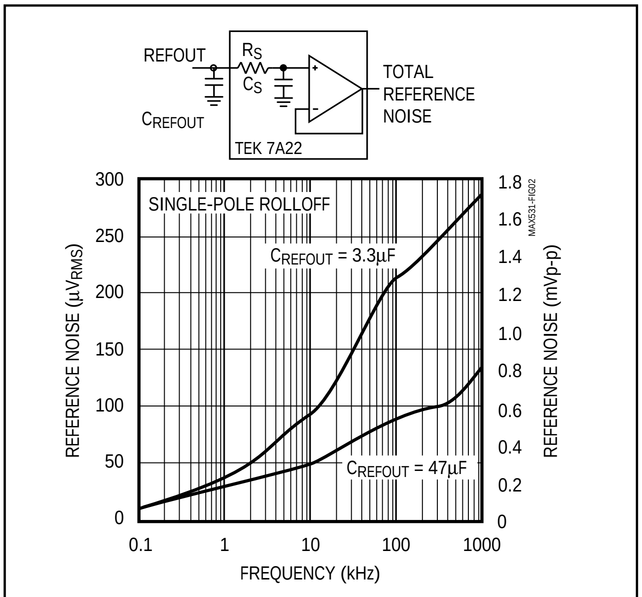


Figure 2. Reference Noise vs. Frequency

Internal Reference (MAX531 only)

The on-chip reference is lesser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current, so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typically, source current is 5mA and sink current is 100µA.

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50µA maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100µA to avoid gain errors.

For applications requiring very low-noise performance, connect a 33µF capacitor from REFOUT to AGND. If noise is not a concern, a lower value capacitor (3.3µF min) may be used. To reduce noise further, insert a buffered RC filter between REFOUT and REFIN (Figure 2). The reference bypass capacitor, C_{REFOUT}, is still required for reference stability. In applications not requiring the reference, connect REFOUT to V_{DD} or use the MAX538 or MAX539 (no internal reference).

External Reference

An external reference in the range (V_{SS} + 2V) to (V_{DD} - 2V) may be used with the MAX531 in dual-supply operation. With the MAX538/MAX539 or the MAX531 in single-supply use, the reference must be positive and may not exceed V_{DD} - 2V. The reference voltage determines the DAC's full-scale output. The DAC input resistance is code dependent and is minimum (40kΩ) at code 555 hex and virtually infinite at code 000 hex. REFIN's input capacitance is also code dependent and has a 50pF maximum value at several codes. Because of the code-dependent nature of reference input impedances, a high-quality, low-output-impedance amplifier (such as the MAX480 low-power, precision op amp) should be used.

If an upgrade to the internal reference is required, the 2.5V MAX873A is suitable: ±15mV initial accuracy, TCV_{OUT} = 7ppm/°C (max).

Logic Interface

The MAX531/MAX538/MAX539 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

Figure 1 shows the MAX531/MAX538/MAX539 timing. The maximum serial clock rate is given by 1 / (t_{CH} + t_{CL}), approximately 14MHz. The digital update rate is limited by the chip-select period, which is 16 x (t_{CH} + t_{CL}) + t_{CSW}. This equals a 1.14µs, or 877kHz, update rate. However, the DAC settling time to 12 bits is 25µs, which may limit the update rate to 40kHz for full-scale step transitions.

Applications Information

Refer to Figures 3a and 3b for typical operating connections.

Serial Interface

The MAX531/MAX538/MAX539 use a three-wire serial interface that is compatible with SPI™, QSPI™ (CPOL = CPHA = 0), and Microwire™ standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the *Functional Diagram*). Sixteen bits of serial data are clocked into the DAC MSB first with the MSB preceded by four fill (dummy) bits. The four dummy bits are not normally needed. They are required **only** when DACs are daisy-chained. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. The serial input data is held in a 16-bit serial shift register. On $\overline{CS}$'s rising edge, the 12 least significant bits are transferred to the DAC register and update the DAC. With $\overline{CS}$ high, data cannot be clocked into the MAX531/MAX538/MAX539.

The MAX531/MAX538/MAX539 input data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The QSPI interface allows variable data input from eight to 16 bits, and can be loaded into the DAC in one write cycle.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

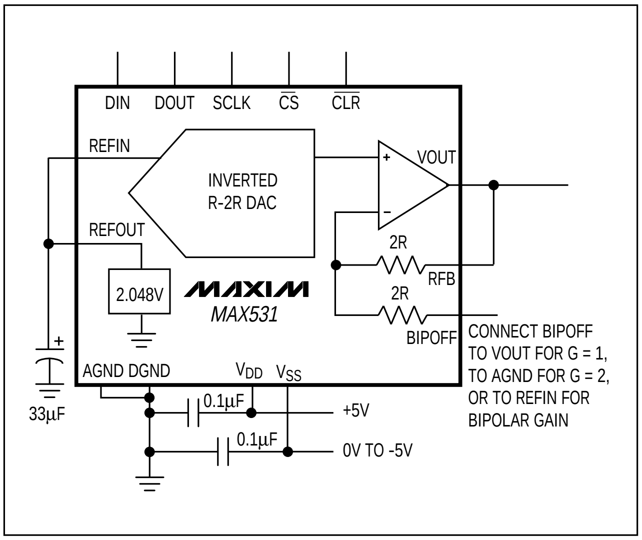


Figure 3a. MAX531 Typical Operating Circuit

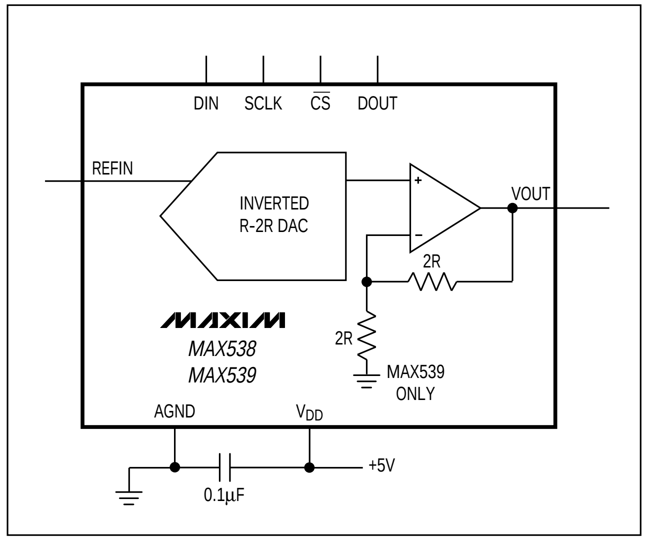


Figure 3b. MAX538/MAX539 Typical Operating Circuit

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. DOUT does **not** go into a high-impedance state when $\overline{CS}$ is high. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

Any number of MAX531/MAX538/MAX539 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that t_{CL} ($\overline{CS}$ low to SCLK high) is greater than t_{DO} + t_{DS}.

Unipolar Configuration

The MAX531 is configured for a gain of +1 (0V to V_{REFIN} unipolar output) by connecting BIPOFF and RFB to VOUT (Figure 6). The converter operates from either single or dual supplies in this configuration. See Table 1 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, 1LSB = V_{REFIN} (2^{-12}). The MAX538 is internally configured for unipolar gain = +1 operation.

A gain of +2 (0V to $2V_{REFIN}$ unipolar output) is set up by connecting BIPOFF to AGND and RFB to VOUT (Figure 7). Table 2 shows the DAC-latch contents vs. VOUT. The MAX531 operates from either single or dual supplies in this mode. In this range, 1LSB = (2)(V_{REFIN}) (2^{-12}) = (V_{REFIN})(2^{-11}). The MAX539 is internally configured for unipolar gain = +2 operation.

Bipolar Configuration

A bipolar range is set up by connecting BIPOFF to REFIN and RFB to VOUT, and operating from dual (±5V) supplies (Figure 8). Table 3 shows the DAC-latch contents (input) vs. VOUT (output). In this range, 1LSB = V_{REFIN} (2^{-11}).

Four-Quadrant Multiplication

The MAX531 can be used as a four-quadrant multiplier by connecting BIPOFF to REFIN and RFB to VOUT, using (1) an offset binary digital code, (2) bipolar power supplies, using dual power supplies, and (3) a bipolar analog input at REFIN within the range V_{SS} + 2V to V_{DD} - 2V, as shown in Figure 9.

In general, a 12-bit DAC's output is (D) (V_{REFIN}) (G), where "G" is the gain (+1 or +2) and "D" is the binary representation of the digital input divided by 2^{12} or 4096. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost, as there are the same number of steps. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V (G = +2) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. Negative full scale is $-V_{REFIN}$, while positive full scale is $+V_{REFIN}$ - 1LSB.

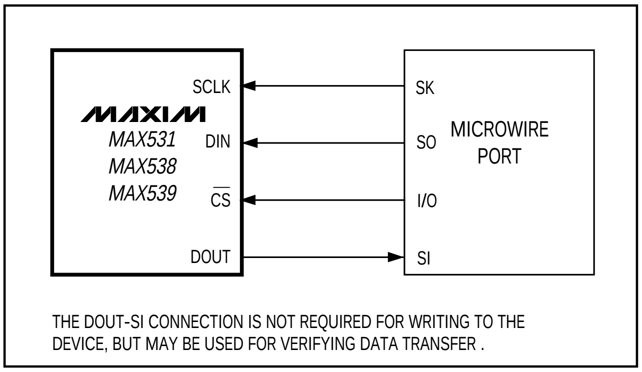


Figure 4. Microwire Connection

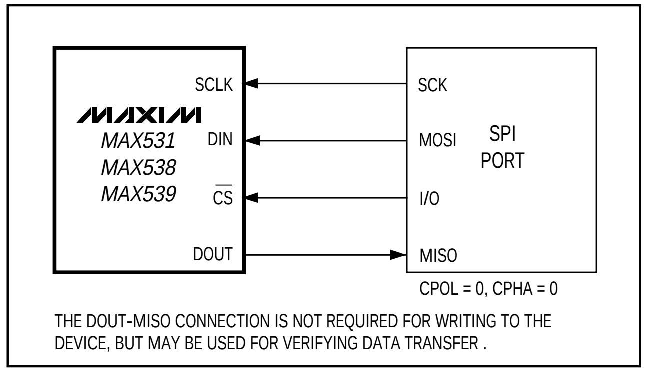


Figure 5. SPI/QSPI Connection

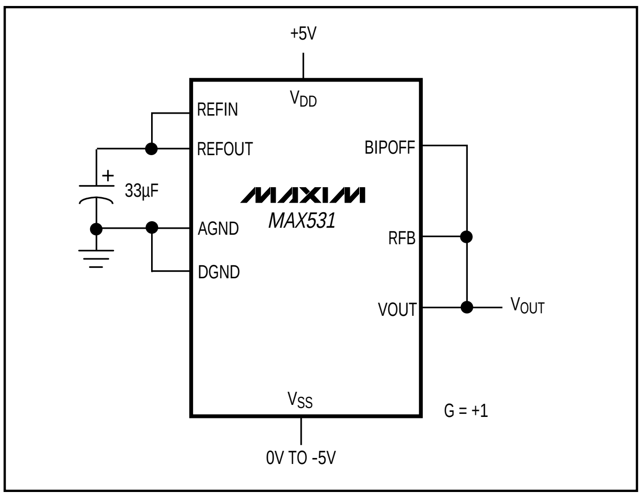


Figure 6. Unipolar Configuration (0V to +2.048V Output)

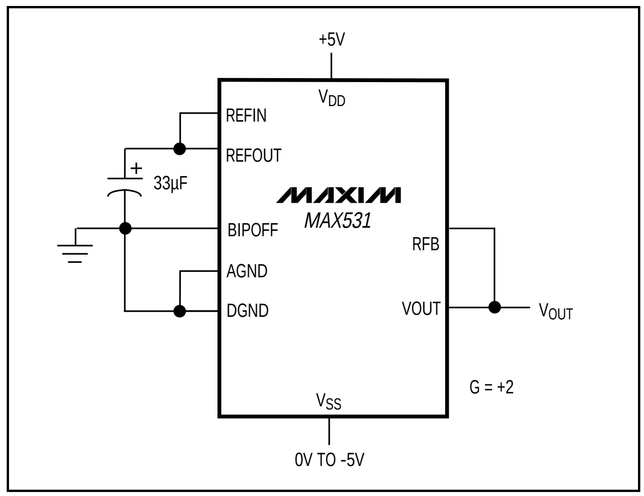


Figure 7. Unipolar Configuration (0V to +4.096V Output)

Table 1. Unipolar Binary Code Table (0V to V_{REFIN} Output), Gain = +1

INPUT	OUTPUT
1111 1111 1111	$(V_{REFIN}) \frac{4095}{4096}$
1000 0000 0001	$(V_{REFIN}) \frac{2049}{4096}$
1000 0000 0000	$(V_{REFIN}) \frac{2048}{4096} = +V_{REFIN} / 2$
0111 1111 1111	$(V_{REFIN}) \frac{2047}{4096}$
0000 0000 0001	$(V_{REFIN}) \frac{1}{4096}$
0000 0000 0000	0V

Table 2. Unipolar Binary Code Table (0V to $2V_{REFIN}$ Output), Gain = +2

INPUT	OUTPUT
1111 1111 1111	$+2 (V_{REFIN}) \frac{4095}{4096}$
1000 0000 0001	$+2 (V_{REFIN}) \frac{2049}{4096}$
1000 0000 0000	$+2 (V_{REFIN}) \frac{2048}{4096} = +V_{REFIN}$
0111 1111 1111	$+2 (V_{REFIN}) \frac{2047}{4096}$
0000 0000 0001	$+2 (V_{REFIN}) \frac{1}{4096}$
0000 0000 0000	0V

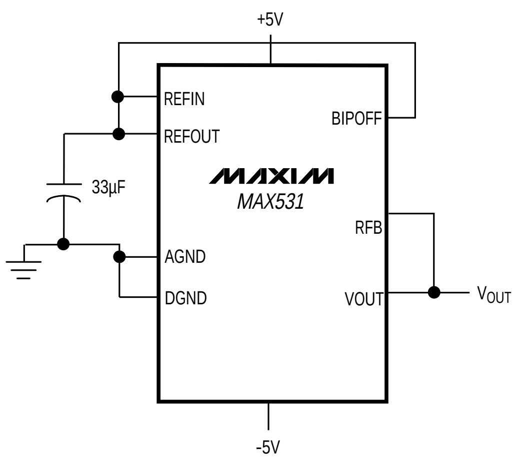


Figure 8. Bipolar Configuration (-2.048V to +2.048V Output)

Table 3. Bipolar (Offset Binary) Code Table ($-V_{REFIN}$ to $+V_{REFIN}$ Output)

INPUT	OUTPUT
1111 1111 1111	$(+V_{REFIN}) \frac{2047}{2048}$
1000 0000 0001	$(+V_{REFIN}) \frac{1}{2048}$
1000 0000 0000	0V
0111 1111 1111	$(-V_{REFIN}) \frac{1}{2048}$
0000 0000 0001	$(-V_{REFIN}) \frac{2047}{2048}$
0000 0000 0000	$(-V_{REFIN}) \frac{2048}{2048} = -V_{REFIN}$

Single-Supply Linearity

As with any amplifier, the MAX531/MAX538/MAX539's output buffer can be positive or negative. When the offset is positive, it is easily accounted for (Figure 10). However, when the offset is negative, the buffer output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive.

Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinearity near-zero output when operating with a single supply. To account for this nonlinearity in the MAX531/MAX538/MAX539, linearity and gain error are measured from code 11 to code 4095. The output buffer's offset and nonlinear behavior do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 4095.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

DGND and AGND should be connected together at the chip. For the MAX531 in single-supply applications, connect V_{SS} to AGND at the chip. The best ground connection may be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass V_{DD} (and V_{SS} in dual-supply mode) with a 0.1µF ceramic capacitor, connected between V_{DD} and AGND (and between V_{SS} and AGND). Mount with short leads close to the device. Ferrite beads may also be used to further isolate the analog and digital power supplies.

Figures 11a and 11b illustrate the grounding and bypassing scheme described.

Saving Power

When the DAC is not being used by the system, minimize power consumption by setting the appropriate code to minimize load current. For example, in bipolar mode, with a resistive load to ground, set the DAC code to mid-scale (Table 3). If there is no output load, minimize internal loading on the reference by setting the DAC to all 0s (on the MAX531, use $\overline{CLR}$). Under this condition, REFIN is high impedance and the op amp operates at its minimum quiescent current. Due to these low current levels, the output settling time for an input code close to 0 typically increases to 60µs (no more than 100µs).

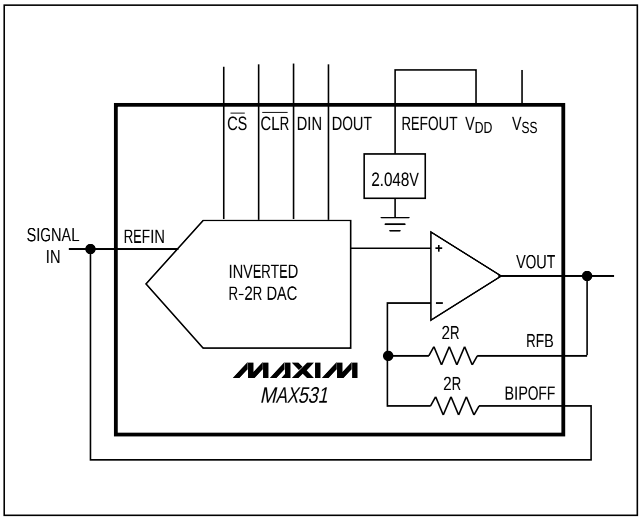


Figure 9. MAX531 Connected as Four-Quadrant Multiplier. The unused REFOUT is connected to V_{DD}.

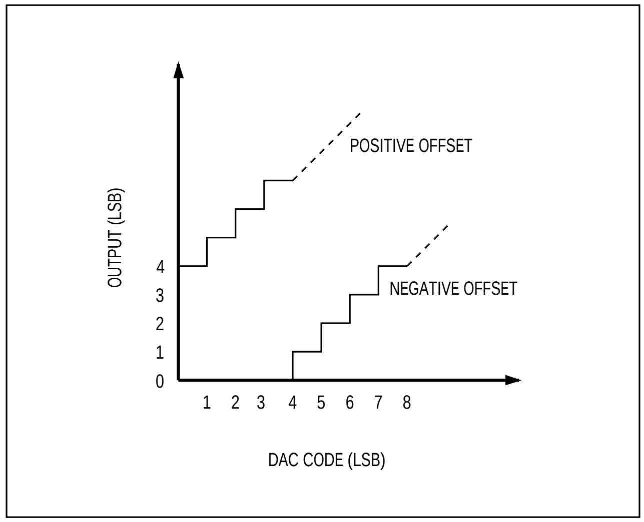


Figure 10. Single-Supply Offset

AC Considerations

Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package and cause internal stray capacitance to appear at the DAC output as noise, even though $\overline{CS}$ is held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding $\overline{CS}$ high, transmitting 555 hex from DIN to DOUT.

Analog Feedthrough

Because of internal stray capacitance, higher frequency analog input signals may couple to the output as shown in the Analog Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. It is tested by holding $\overline{CS}$ high, setting the DAC code to all 0s, and sweeping REFIN.

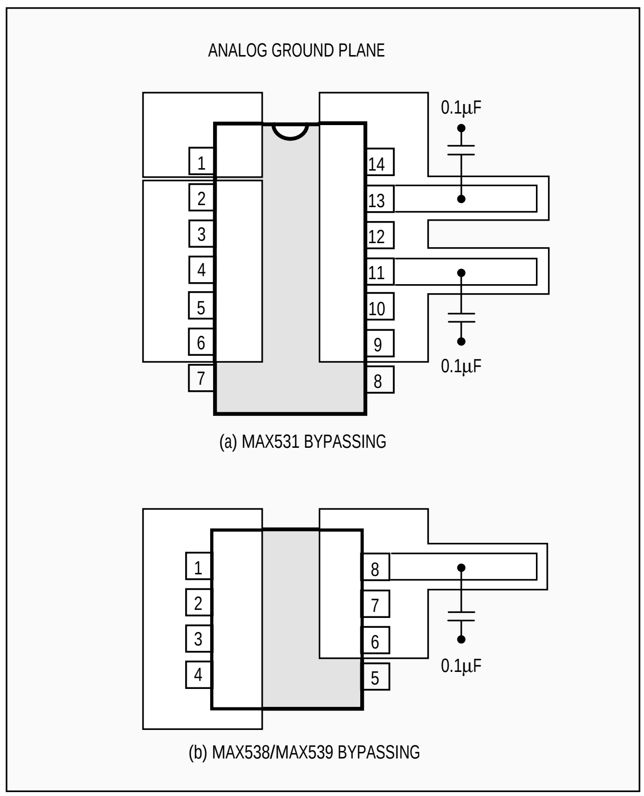


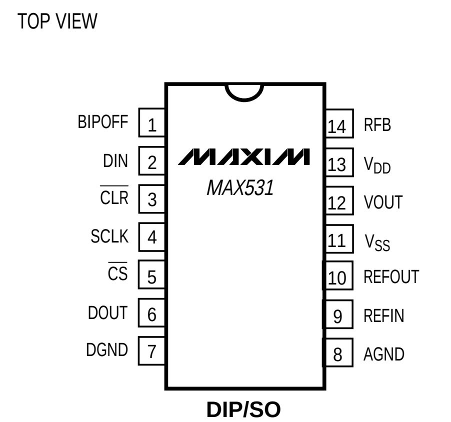
Figure 11. Power-Supply Bypassing

Ordering Information (continued)

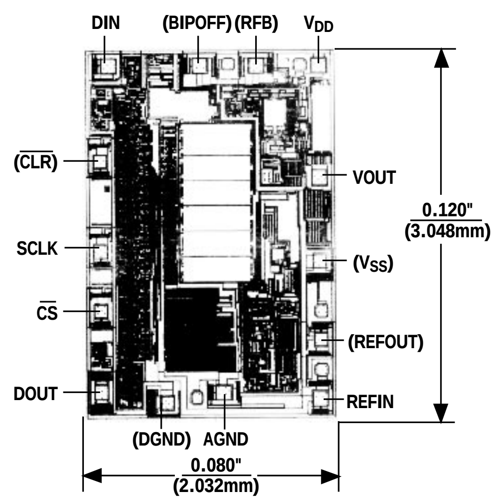
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX531AEPD	-40°C to +85°C	14 Plastic DIP	±1/2
MAX531BEPD	-40°C to +85°C	14 Plastic DIP	±1
MAX531AESD	-40°C to +85°C	14 SO	±1/2
MAX531BESD	-40°C to +85°C	14 SO	±1
MAX538ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX538BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX538ACSA	0°C to +70°C	8 SO	±1/2
MAX538BCSA	0°C to +70°C	8 SO	±1
MAX538BC/D	0°C to +70°C	Dice*	±1
MAX538AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX538BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX538AESA	-40°C to +85°C	8 SO	±1/2
MAX538BESA	-40°C to +85°C	8 SO	±1
MAX539ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX539BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX539ACSA	0°C to +70°C	8 SO	±1/2
MAX539BCSA	0°C to +70°C	8 SO	±1
MAX539BC/D	0°C to +70°C	Dice*	±1
MAX539AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX539BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX539AESA	-40°C to +85°C	8 SO	±1/2
MAX539BESA	-40°C to +85°C	8 SO	±1

Dice are specified at T_A = +25°C only.

Pin Configurations (continued)



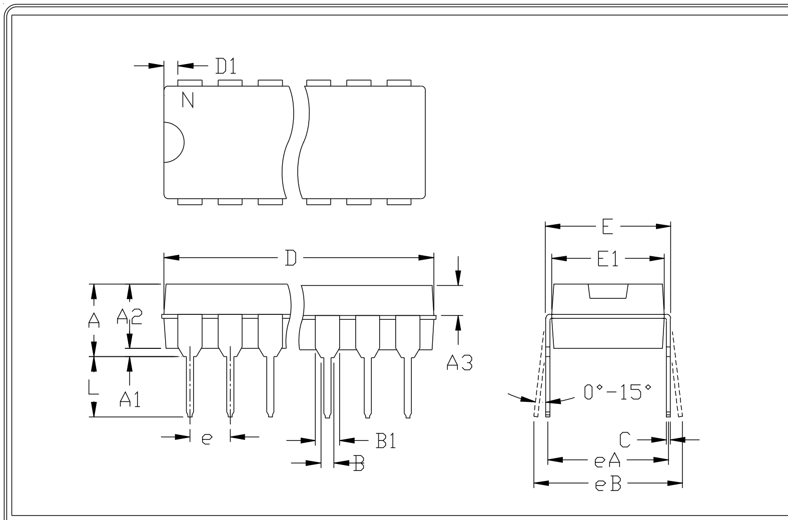
Chip Topography



( ) ARE FOR MAX531 ONLY.

TRANSISTOR COUNT: 922
SUBSTRATE CONNECTED TO V_{DD}

Package Information



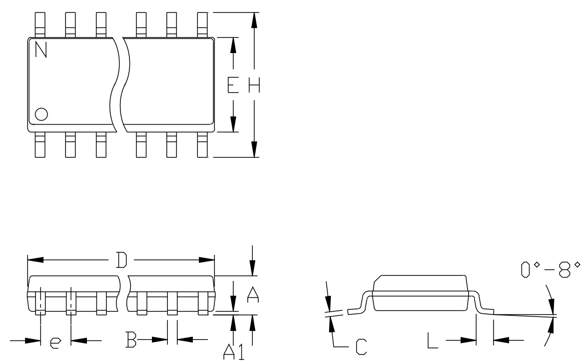
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0043 | REV: A

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: SOIC .150"

1/1

DOCUMENT CONTROL NUMBER: 21-0041 REV: A

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19-1972; Rev 1; 10/92

MAXIM

CMOS, 12-Bit, Serial-Input Multiplying DAC

MAX543

General Description

The MAX543 is a 12-bit, current-output, multiplying digital-to-analog converter (DAC) that comes in space-saving 8-pin DIP and 8- or 16-pin surface-mount SO packages. Its 3-wire serial interface saves additional board space and also results in low power dissipation. When used with microprocessors (µPs) with a serial port, the MAX543 minimizes the digital noise feedthrough from its input pins to its output. The serial port can be used as a dedicated analog bus and kept inactive while the MAX543 is in use. Serial interfacing also reduces the complexity of opto- or transformer-isolated applications.

The MAX543 contains a 12-bit R-2R type DAC, a serial-in parallel-out shift register, a DAC register and control logic. On the rising edge of the clock (CLK) pulse, the serial input (SRI) data is shifted into the MAX543. When all the data is clocked in, it is transferred into the DAC register by taking the $\overline{LOAD}$ input low.

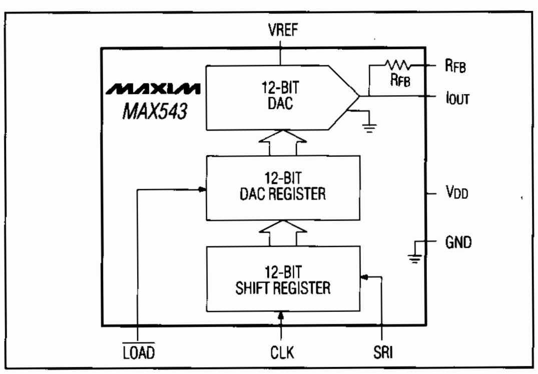
The MAX543 is specified with a single power supply of either +5V or +15V. With a +5V supply, the digital inputs are TTL and +5V CMOS compatible. High-voltage CMOS compatibility is maintained with a +15V supply.

Maxim's MAX543 uses low-tempco thin-film resistors laser trimmed to ±1/4LSB linearity and better than ±1LSB gain accuracy. The digital inputs are protected against electrostatic discharge (ESD) damage and can typically withstand over 5,000V of ESD voltages.

Applications

- Automatic Calibration
- Motion-Control Systems
- µP-Controlled Systems
- Programmable Amplifiers/Attenuators
- Digitally Controlled Filters

Functional Diagram



Features

- ♦ **12-Bit Accuracy in 8-Pin MiniDIP or SO**
- ♦ **Fast 3-Wire Serial Interface**
- ♦ **Low INL and DNL (±1/2LSB Max)**
- ♦ **Gain Accuracy to ±1LSB Max**
- ♦ **Low Gain Tempco (5ppm/°C Max)**
- ♦ **Operates with +5V or +15V Supplies**
- ♦ **TTL/CMOS Compatible**
- ♦ **ESD Protected**

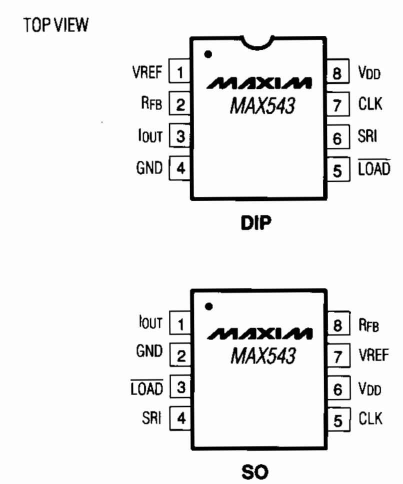
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSBs)
MAX543ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX543BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX543ACSA	0°C to +70°C	8 SO	±1/2
MAX543BCSA	0°C to +70°C	8 SO	±1
MAX543ACWE	0°C to +70°C	16 Wide SO	±1/2
MAX543BCWE	0°C to +70°C	16 Wide SO	±1
MAX543BC/D	0°C to +70°C	Dice*	±1
MAX543AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX543BEPA	-40°C to +85°C	8 Plastic DIP	±1

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Pin Configurations



Note: 8-DIP and 8-SOIC Pinouts differ.
Wide SO on last page.

Call toll free 1-800-998-8800 for free samples or literature.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V
VREF to GND . . . . . ±25V
VRFB to GND . . . . . ±25V
Digital Input Voltage to GND . . . . . -0.3V, V_{DD} + 0.3V
V_{IOUT} to GND . . . . . -0.3V, V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) . . 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) . . 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX543AC/BC_ _ . . . . . 0°C to +70°C
MAX543AE/BE_ _ . . . . . -40°C to +85°C
MAX543AM/BMJA . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, +12V or +15V; VREF = +10V; V_{IOUT} = GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Integral Nonlinearity	INL			MAX543A			±1/2	LSB
				MAX543B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits over temperature		MAX543A			±1/2	LSB
				MAX543B			±1	
Gain Error	FSE	Using internal R_{FB}	T_A = +25°C	MAX543A			±1	LSB
				MAX543B			±2	
			T_A = T_{MIN} to T_{MAX}	All grades			±2	
Gain Tempco ΔGain/ΔTemp (Note 2)	TCFS	Using internal R_{FB}				±1	±5	ppm/°C
DC Supply Rejection	PSR	ΔV_{DD} = ±5%					±0.001	%/%
DYNAMIC PERFORMANCE (Note 2)								
Current Settling Time	t_S	T_A = +25°C, to 1/2LSB, I_{OUT} load is 100Ω‖13pF, DAC register alternately loaded with all 1s and all 0s				0.25	1	µs
Digital-to-Analog Glitch	Q	VREF = 0V, I_{OUT} load is 100Ω‖13pF, DAC register alternately loaded with all 1s and all 0s				2	20	nV-s
AC Feedthrough at I_{OUT}	FTE	VREF = ±10V_{p-p} at 10kHz, DAC register loaded with all 0s				0.4	1	mV_{p-p}
Total Harmonic Distortion	THD	VREF = 6V_{rms} at 1kHz, DAC register loaded with all 1s				-85		dB
Output Noise-Voltage Density	e_n	10Hz to 100kHz, measured between R_{FB} and I_{OUT}				13	15	nV/√Hz
REFERENCE INPUT								
Input Resistance	RREF				7	11	15	kΩ
Input Resistance Tempco	TCR					-200		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, +12V or +15V; VREF = +10V; V_{IOUT} = GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

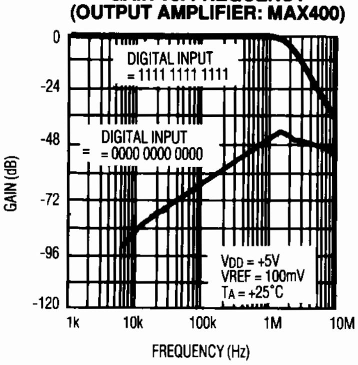
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG OUTPUT								
I_{OUT} Leakage Current	I_{LKG}	DAC register loaded with all 0s	T_A = +25°C	All grades		±0.5	±5	nA
			T_A = T_{MIN} to T_{MAX}	MAX543AC/BC/AE/BE			±25	
				MAX543AM/BM			±100	
I_{OUT} Capacitance (Note 2)	C_{OUT}	DAC register loaded with all 0s				55	80	pF
		DAC register loaded with all 1s				85	110	
DIGITAL INPUTS								
Input High Voltage	V_{IH}	V_{DD} = 5V			2.4			V
		V_{DD} = 15V			13.5			
Input Low Voltage	V_{IL}	V_{DD} = 5V					0.8	V
		V_{DD} = 15V					1.5	
Input Leakage Current	I_{IN}	Digital inputs at 0V or V_{DD}					±1	µA
Input Capacitance (Note 2)	C_{IN}	Digital inputs at 0V or V_{DD}					8	pF
SWITCHING CHARACTERISTICS (Note 3)								
CLK Pulse Width High	t_{CH}				90			ns
CLK Pulse Width Low	t_{CL}				120			ns
SRI Data to CLK Setup	t_{DS}				40			ns
SRI Data to CLK Hold	t_{DH}				80			ns
$\overline{LOAD}$ Pulse Width	t_{LD}				120			ns
LSB CLK to $\overline{LOAD}$	t_{SL}				0			ns
$\overline{LOAD}$ High to CLK	t_{LC}				0			ns
POWER SUPPLY								
V_{DD} Range	V_{DD}	V_{DD} = 12V or 15V			+11.40		+15.75	V
		V_{DD} = 5V			+4.75		+5.25	
I_{DD} Range	I_{DD}	All digital inputs at V_{IL} or V_{IH}					500	µA
		All digital inputs at 0V or V_{DD}				5	100	

Note 1: Tests are performed at V_{DD} = +5V and V_{DD} = +15V. Operation at +12V is guaranteed by power-supply rejection (PSR) tests.
Note 2: Guaranteed by design, not subject to test.
Note 3: Sample tested to 0.1% AQL.

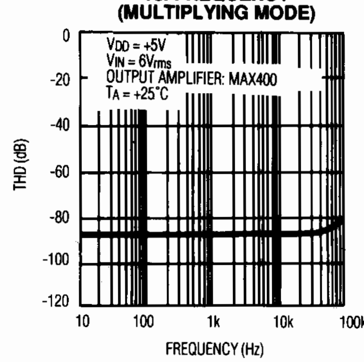
CMOS, 12-Bit, Serial-Input Multiplying DAC

Typical Operating Characteristics

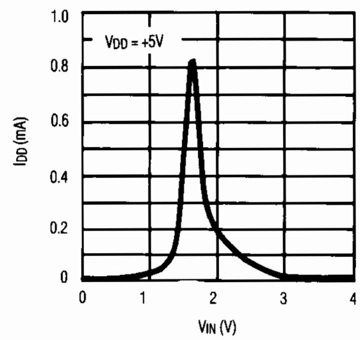
GAIN vs. FREQUENCY (OUTPUT AMPLIFIER: MAX400)



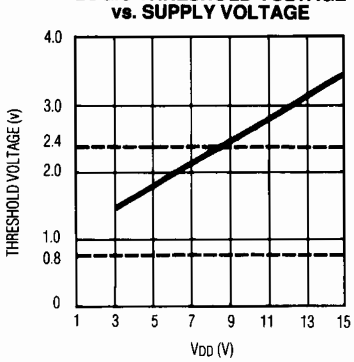
TOTAL HARMONIC DISTORTION vs. FREQUENCY (MULTIPLYING MODE)



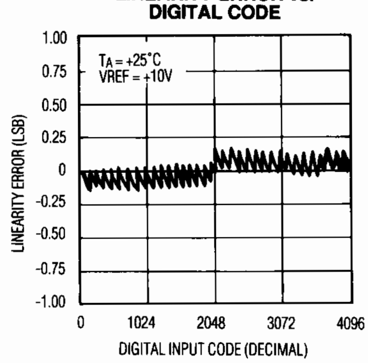
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



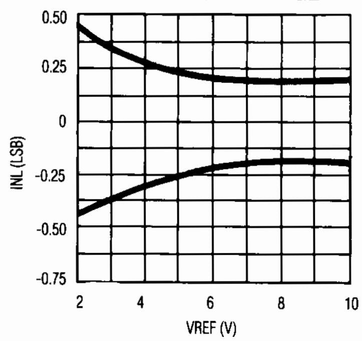
LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



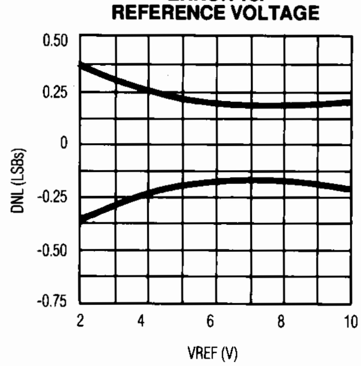
LINEARITY ERROR vs. DIGITAL CODE



INTEGRAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



DIFFERENTIAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



Detailed Description

D/A Converter

The MAX543 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches, as shown in Figure 1. Binary weighted currents are switched to either I_{OUT} or GND depending on the status of each input data bit. Although the current at I_{OUT} and GND depends on the digital input code, the sum of the two output currents is always equal to the input current at VREF.

The current output (I_{OUT}) can be converted into a voltage by adding an external output amplifier (Figure 3). The VREF input accepts a wide range of signals, including fixed and time-varying voltage or current inputs. If a current source is used for the reference input, then a low-tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor (R_{FB}) is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain-temperature coefficient.

The I_{OUT} pin output capacitance (C_{OUT}) is code dependent and is typically 55pF with all switches to GND and 85pF with all switches to I_{OUT}.

Digital Circuit

Figure 2 shows the MAX543 timing diagram. The most significant bit (MSB) is always loaded first on the rising edge of the clock. When all data is shifted into the MAX543, the DAC register is loaded by taking the $\overline{LOAD}$ signal low. The DAC register is transparent when $\overline{LOAD}$ is low and latched when $\overline{LOAD}$ is high. If the $\overline{LOAD}$ signal is taken low before the LSB bit is fully shifted into the shift register, the DAC output can produce a "glitch." If this is undesirable, the $\overline{LOAD}$ signal can be delayed 30ns after the rising edge of the LSB clock edge to avoid this condition.

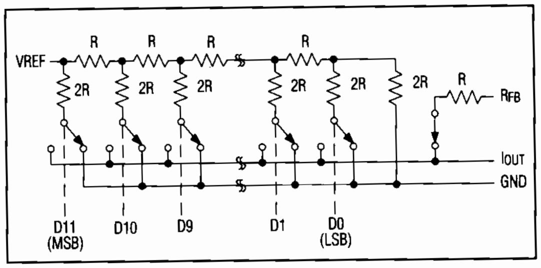


Figure 1. MAX543 Simplified Circuit

The MAX543's input buffer inverters act as level shifters, converting TTL levels into CMOS logic levels. These input buffers are TTL and 5V-CMOS compatible (0.8V and 2.4V) at V_{DD} = 5V. For V_{DD} = 15V the input buffers are CMOS compatible (1.5V and 13.5V). At this supply voltage, the input buffers are in their linear region when the input voltages are between 1V and 6V. Therefore, to minimize high supply currents, the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and GND) as possible.

Circuit Configurations

Unipolar Operation

Figure 3 shows the MAX543's basic application. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, VREF.

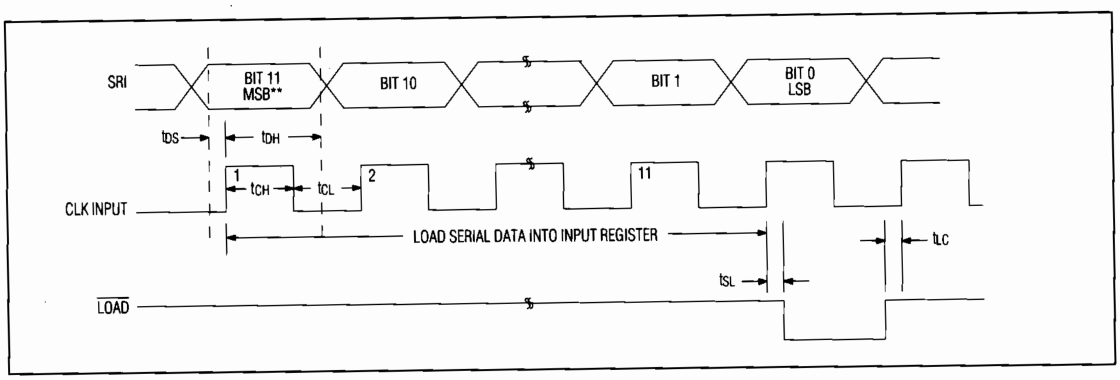


Figure 2. Write-Cycle Timing Diagram

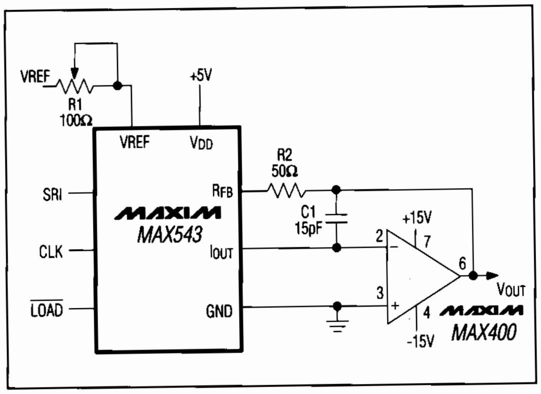


Figure 3. Unipolar Operation

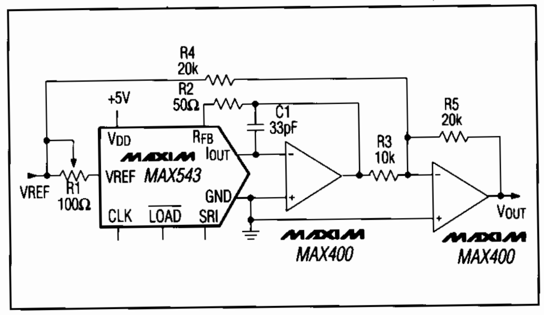


Figure 4. Bipolar Operation

Table 1. Unipolar Binary-Code Table for Circuit of Figure 3

DIGITAL INPUT MSB … LSB	ANALOG OUTPUT
1111 1111 1111	$-VREF\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-VREF\left(\frac{2048}{4096}\right) = -\frac{VREF}{2}$
0000 0000 0001	$-VREF\left(\frac{1}{4096}\right)$
0000 0000 0000	0

Table 2. Offset Binary-Code Table for Circuit of Figure 4

DIGITAL INPUT MSB … LSB	ANALOG OUTPUT
1111 1111 1111	$+VREF\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+VREF\left(\frac{1}{2048}\right)$
1000 0000 0000	0
0111 1111 1111	$-VREF\left(\frac{1}{2048}\right)$
0000 0000 0000	$-VREF\left(\frac{2048}{2048}\right)$

In many applications, gain adjustment will not be necessary since the part's gain accuracy is sufficient, or is trimmed at the reference source. In these cases, resistors R1 and R2 in Figure 3 can be omitted. If the gain is trimmed and the DAC is operated over a wide temperature range, use low-tempco (<300ppm/°C) resistors for R1 and R2.

Capacitor C1 provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the output of the DAC.

Bipolar Operation

Figure 4 shows the MAX543 operating in bipolar (or 4-quadrant multiplying) mode. A second amplifier and three matched resistors (R3 , R4 and R5) are required. These resistors must be of the same material (preferably

Table 3. Twos-Complement Code Table

DIGITAL INPUT MSB … LSB	ANALOG OUTPUT
0111 1111 1111	$+VREF\left(\frac{2047}{2048}\right)$
0000 0000 0001	$+VREF\left(\frac{1}{2048}\right)$
0000 0000 0000	0
1111 1111 1111	$-VREF\left(\frac{1}{2048}\right)$
1000 0000 0000	$-VREF\left(\frac{2048}{2048}\right)$

metal film or wire-wound) for good temperature tracking characteristics (<15ppm/°C), and should match to 0.01% for 12-bit performance. The output code is offset binary and is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control the amplitude. The MSB can be inverted in software using an exclusive-OR instruction to make the MAX543 work with twos-complement coding. Table 3 shows the code relationships to output voltage for twos-complement operation.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is needed to adjust the ratio of R3 and R4 for 0V out. Trim full scale by loading the DAC with all 0s or all 1s, and adjusting VREF's amplitude or varying R5 until the desired positive or negative output is obtained. In many applications, the gain adjustment will not be necessary, especially when using parts with a guaranteed maximum ±1LSB gain error. In these cases the gain can be trimmed at the reference source and resistors R1 and R2 in Figure 4 omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low-tempco (<300ppm/°C) resistors should be used for R1 and R2.

Single-Supply Operation (Voltage Mode)

The MAX543 can be conveniently used in single-supply (voltage mode) operation with I_{OUT} biased at any voltage between GND and V_{DD}. I_{OUT} must not be allowed to go 0.3V lower than the GND or 0.3V higher than V_{DD}. Otherwise, internal diodes would turn on, causing a high current flow from the supply that could damage the device.

Figure 5 shows the MAX543 connected as a voltage-output DAC. I_{OUT} is connected to the reference-voltage

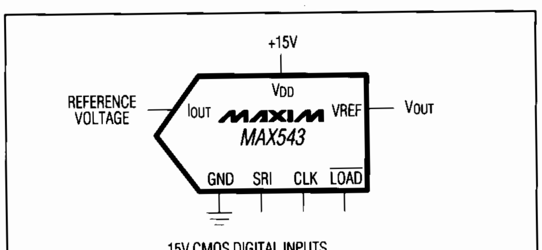


Figure 5. Single-Supply Operation Using Voltage-Switching Mode

source and GND is grounded. The DAC output now appears at the VREF pin, which has a constant impedance equal to the reference input resistance (typically 11kΩ). This output should be buffered with an op amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

The input impedance of the reference input (I_{OUT}) for this mode is code dependent, and the circuit's response time depends on the reference source's behavior with changing load conditions.

Two advantages of voltage-mode operation are single-supply operation and that a negative reference is not required for a positive output. Note that the reference input (I_{OUT}) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral (INL) and differential nonlinearity (DNL).

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage-output mode.

MAX543 Opto-Isolated Application

Figure 6a shows the MAX543 interface to optocouplers for isolated barrier applications. Three optocouplers (OC1, OC2 and OC3) carry the serial data and clocking signals across the isolation barrier. Isolated power sources, V+ and V-, supply the MAX543, the output amplifier and optocouplers. If data word updates are infrequent and large analog output transitions can be tolerated while serial data is being clocked in, then parts count can be reduced by eliminating optocoupler OC3 and tying $\overline{LOAD}$ (pin 5) of the MAX543 low.

When using type 6N136 optocouplers, this circuit accepts serial data at a maximum clock rate of 100kHz, or 130µs per data word. The SERIAL DATA and $\overline{LOAD}$ signals should change coincident with the falling edge of CLOCK, as shown in the timing diagram (Figure 6b). A positive CLOCK cycle is masked during the time $\overline{LOAD}$ is low.

The MAX543 will also work with 5V isolated supplies using the optocoupler circuit of Figure 6a. Change the values of R1 through R3 to 3kΩ to maintain switching speed with the lower value of V+.

Current drawn from V- for the MAX543 and optocoupler is 3.5mA at a 100kHz clock rate when all data bits are set to 0. V+ current drops to 0 (excluding reference and op-amp current) when no new data is being loaded and CLOCK, SERIAL DATA, and $\overline{LOAD}$ are static high.

CMOS, 12-Bit, Serial-Input Multiplying DAC

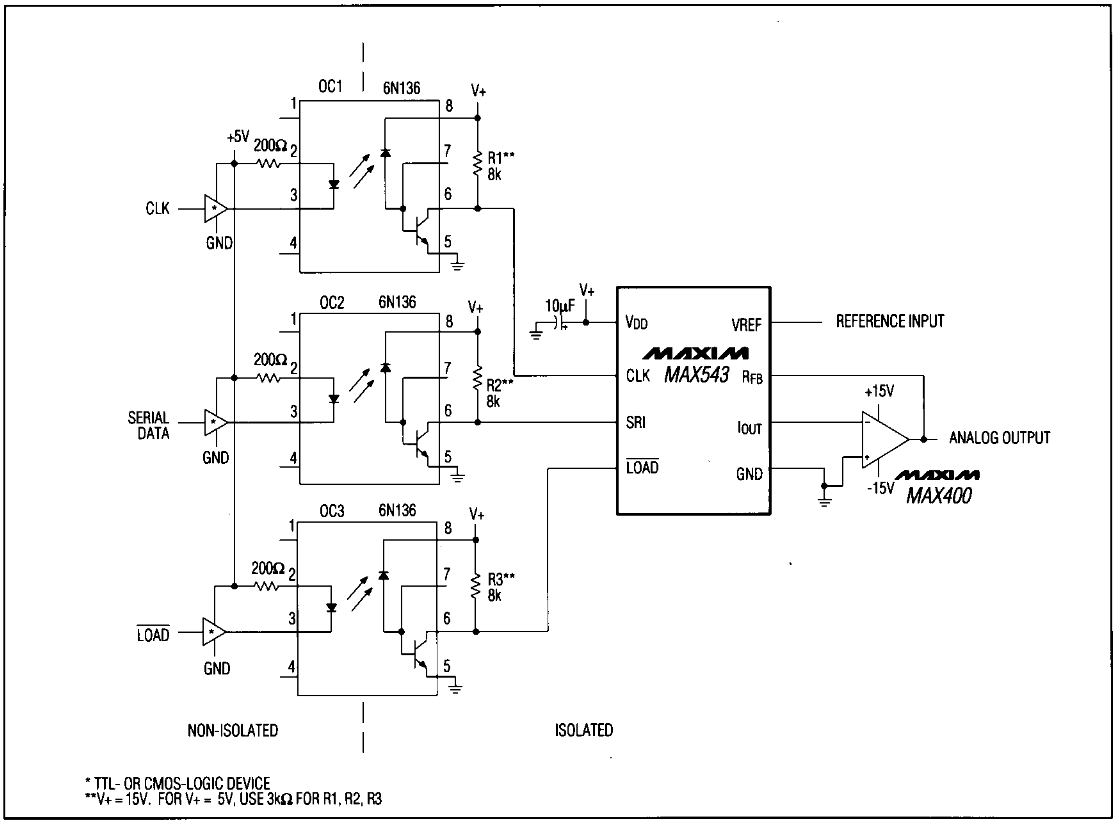


Figure 6a. MAX543 Opto-Coupled Application

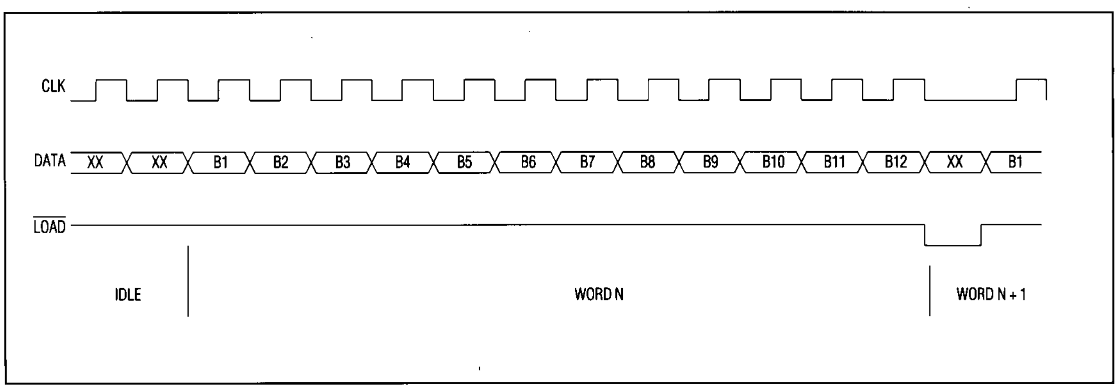


Figure 6b. MAX543 Opto-Isolated Timing

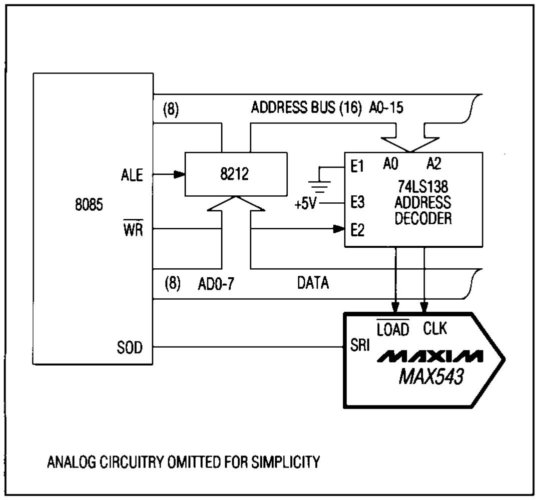


Figure 7. MAX543 8085 Interface

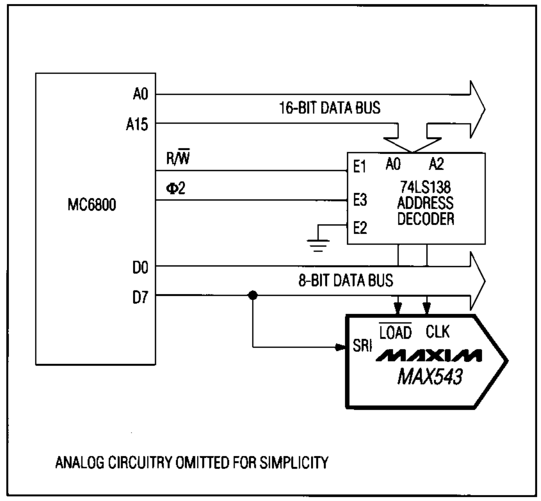


Figure 8. MAX543 MC6800 Interface

Microprocessor Interfacing

Interfacing to the 8085

Figure 7 shows the MAX543 interfacing to the 8085 µP. The SOD line from the 8085 sends serial data to the DAC. This data is clocked into the MAX543 by executing memory-write instructions. Generate the CLK input for the DAC by decoding address 8000 and WR signal. The data is transferred into the DAC register with a memeory-write instruction to address A000, which brings LOAD low. The data for the MAX543 is stored in right-justified format in registers H and L of the 8085.

Interfacing to the MC6800

Figure 8 shows the MAX543 interfacing to the MC6800 µP. Transfer the data into the MAX543 by executing successive memory-write instructions while changing the data between writes to construct the serial data to the DAC.

The D7 data line is used for the SRI signal. The lower half of the memory location 0000 holds the four MSB data bits, and the 0001 location holds the eight LSB data bits. The memory address 2000, R/W, and 02 are decoded to genenrate the CLK signal for the DAC with each memory write. Similarly, a memory write to address 4000 transfers data into the DAC register by bringing the MAX543's LOAD input low.

Applications Information

Output Amplifier Offset

For best linearity, terminate I_{OUT} and GND at exactly 0V. In most applications, I_{OUT} is connected to the summing junction of an inverting op amp. The amplifiers's input offset voltage can degrade the DAC's linearity by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\,(1 + R_{FB}/R_O)$$

where V_{OS} is the op amp's offset and R_O is the DAC's output resistance. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$ – a change of $2/3V_{OS}$. Therefore, an amplifier with 3mV of offset will degrade the linearity by 2mV – almost a full LSB with a 10V reference voltage. For best linearity, use a low-offset amplifier such as the MAX400, otherwise the amplifier offset must be trimmed to zero. A good guide rule is that V_{OS} should be no more than 1/10LSB.

The output-amplifer input bias current (I_B) can also limit performance since I_B X R_{FB} generates an offset error. Therefore, I_B should be much less than the DAC output current for 1LSB, typically 250nA with VREF = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output-amplifier noninverting input is grounded through a "bias-current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the output amplifier's AC characteristics are not critical. In higher-speed applications where either the reference input is an AC signal or the DAC output must quickly settle to a new programmmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic coupling of the signal from the VREF pin to I_{OUT}. This is normally a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on ciruit-board layout and on-chip capacitive coupling. Layout-induced feedthrough can be minimized with guard traces beween digital inputs, VREF, and I_{OUT} pins.

The DAC output follows the digital inputs when the $\overline{LOAD}$ pin is low. In this mode, invalid outputs and voltage glitches can appear at the DAC output. Keeping the $\overline{LOAD}$ input high until all the data is shifted into the MAX543 eliminates this problem.

Compensation

A compenation capacitor, C1, may be required when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used, but typically ranges from 10pF to 33pF. Too small a value causes output ringing, while excess capacitance overdamps the output. The size of C1 can be minimized and the output-voltage settling time improved by keeping the cirucit-boad trace and stray capacitance at I_{OUT} as low as possible.

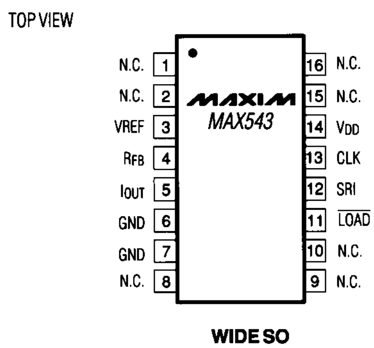
Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low-resistance (less than 0.2Ω) connection. The current at I_{OUT} and GND varies with input code, creating a code-dependent error if these terminals are connected to ground (or a "virtural ground") through a resistive path.

Connect a 1µF bypass capacitor in parallel with a 0.01µF ceramic capacitor across V_{DD} and GND, and as close to the pins as possible.

The MAX543 has high-impedance digital inputs. To minimize noise pick-up, tie them to either V_{DD} or GND when not in use. It is good practice to connect active inputs to V_{DD} or GND through high-value resistors (1MΩ) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

Pin Configurations (continued)

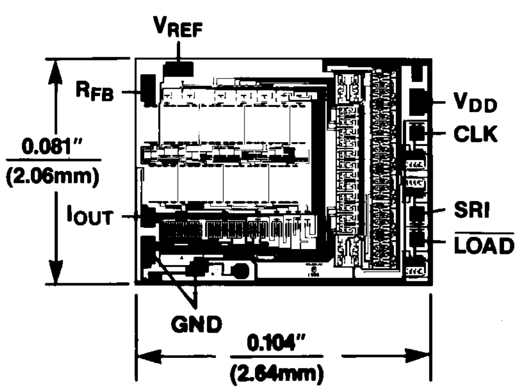


* PINS 6 AND 7 MUST BE CONNECTED TOGETHER AS CLOSE TO THE PACKAGE AS POSSIBLE

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSBs)
MAX543AESA	-40°C to +85°C	8 SO	±1/2
MAX543BESA	-40°C to +85°C	8 SO	±1
MAX543AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX543BEWE	-40°C to +85°C	16 Wide SO	±1
MAX543AEJA	-40°C to +85°C	8 CERDIP	±1/2
MAX543BEJA	-40°C to +85°C	8 CERDIP	±1
MAX543AMJA	-55°C to +125°C	8 CERDIP	±1/2
MAX543BMJA	-55°C to +125°C	8 CERDIP	±1

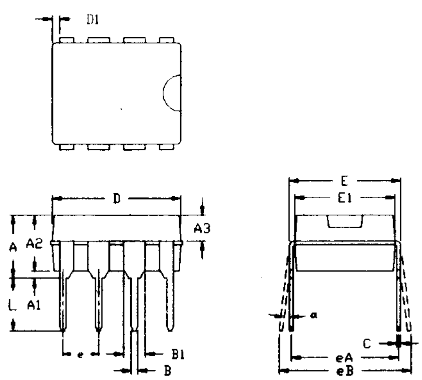
Chip Topography



CMOS, 12-Bit, Serial-Input Multiplying DAC

Package Information

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.348	0.390	8.84	9.91
D1	0.005	0.035	0.13	0.89
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. MEETS JEDEC MS-001 AB

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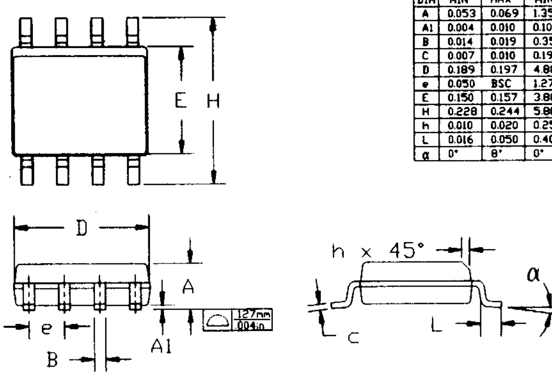
21-324 A

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AA

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