19-4011; Rev 1; 12/96

MAXIM

# Voltage-Output, 12-Bit Multiplying DACs



## General Description

The MAX501/MAX502 are 12-bit, 4-quadrant, voltage-output, multiplying digital-to-analog converters (DACs) with an output amplifier. Thin-film resistors, laser trimmed at the wafer level, maintain accuracy over the full operating temperature range.

The MAX501/MAX502 have buffered latches that are easily interfaced with microprocessors. Data is transferred into the input register in either a right-justified 8+4-bit format (MAX501) or with a 12-bit-wide data path (MAX502). In the MAX501, an $\overline{LDAC}$ signal transfers data from the input register to the DAC register. In the MAX502, the input registers are controlled by standard $\overline{CHIP\ SELECT}$ ($\overline{CS}$) and $\overline{WRITE}$ ($\overline{WR}$) signals. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs are grounded, making all latches transparent. All logic inputs are level triggered and compatible with TTL and +5V CMOS logic levels.

The internally compensated, low-input offset-voltage output amplifier provides an output voltage from +10V to -10V while sourcing and sinking up to 5mA.

## Applications

Digital Attenuators
Programmable-Gain Amplifiers
Servo Controls
Digital to 4mA-to-20mA Converters
Automatic Test Equipment
Programmable Power Supplies

## Features

- **12-Bit Voltage Output DAC**
- **±10V and 5mA Output Drive**
- **Monotonic Over Temperature**
- **Four Range-Scaling Resistors**
- **8+4 (MAX501) and 12-Bit (MAX502) Interface**
- **24-Pin DIP and Wide SO Packages**

## Ordering Information

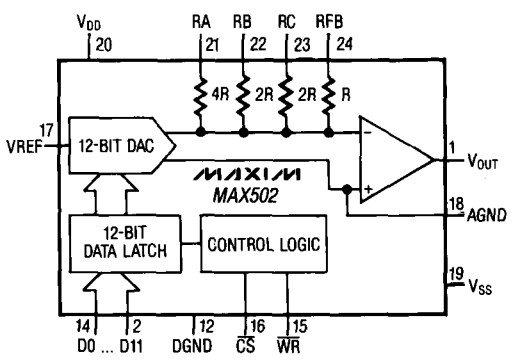
| PART | TEMP. RANGE | PIN-PACKAGE | ERROR (LSBs) |
|---|---|---|---|
| MAX501ACNG | 0°C to +70°C | 24 Narrow Plastic DIP | ±1/2 |
| MAX501BCNG | 0°C to +70°C | 24 Narrow Plastic DIP | ±3/4 |
| MAX501ACWG | 0°C to +70°C | 24 Wide SO | ±1/2 |
| MAX501BCWG | 0°C to +70°C | 24 Wide SO | ±3/4 |
| MAX501BC/D | 0°C to +70°C | Dice* | ±3/4 |
| MAX501AENG | -40°C to +85°C | 24 Narrow Plastic DIP | ±1/2 |
| MAX501BENG | -40°C to +85°C | 24 Narrow Plastic DIP | ±3/4 |
| MAX501AEWG | -40°C to +85°C | 24 Wide SO | ±1/2 |
| MAX501BEWG | -40°C to +85°C | 24 Wide SO | ±3/4 |
| MAX501AMRG | -55°C to +125°C | 24 Narrow CERDIP** | ±1/2 |
| MAX501BMRG | -55°C to +125°C | 24 Narrow CERDIP** | ±3/4 |

**Ordering information continued on last page.**

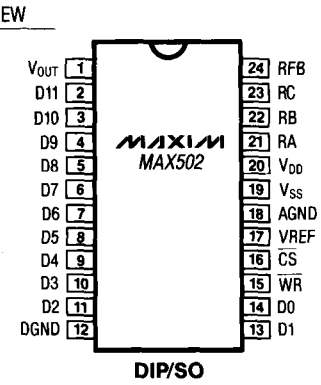
* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

## Functional Diagram




## Pin Configurations




**DIP/SO**

MAX501 on last page

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to DGND ..... -0.3V, +17V
$V_{SS}$ to DGND ..... +0.3V, -17V
VREF to AGND ..... ±25V
RFB to AGND ..... ±25V
RA to AGND ..... ±25V
RB to AGND ..... ±25V
RC to AGND ..... ±25V
$V_{OUT}$ to AGND (Note 1) ..... $V_{DD}$ +0.3V, $V_{SS}$ -0.3V
$V_{DD}$ to AGND ..... -0.3V, +17V
AGND to DGND ..... -0.3V, $V_{DD}$

Digital Input Voltage to DGND ..... -0.3V, $V_{DD}$
Continuous Power Dissipation (any package)
to +75°C ..... 650mW
derate above +75°C ..... 10mW/°C
Operating Temperature Ranges:
MAX501_C_, MAX502_C_ ..... 0°C to +70°C
MAX501_E_, MAX502_E_ ..... -40°C to +85°C
MAX501_M_, MAX502_M_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

**Note 1:** $V_{OUT}$ may be shorted to AGND, $V_{DD}$, or $V_{SS}$ if the power dissipation of the package is not exceeded.

*Stresses beyond those under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

Dual Supply ($V_{DD}$ = +11.4V to +15.75V, $V_{SS}$ = -11.4V to -15.75V, VREF = +10V, AGND = DGND = 0V, $R_L$ = 2kΩ, $C_L$ = 100pF, all grades, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | | |
| Resolution | N | | | 12 | | | Bits |
| Relative Accuracy | INL | $T_A$ = +25°C | MAX501/502A | | | ±1/2 | LSB |
| | | | MAX501/502B | | | ±3/4 | |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | MAX501/502A | | | ±3/4 | |
| | | | MAX501/502B | | | ±1 | |
| Differential Nonlinearity | DNL | | | | | ±1 | LSB |
| Zero-Code Offset Error | | $T_A$ = +25°C | | | | ±1 | mV |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | MAX501/502_C/E | | | ±2 | |
| | | | MAX501/502_M | | | ±3 | |
| Offset Temperature Coefficient | $\Delta V_{OS}/\Delta Temp$ | | | | ±5 | | µV/°C |
| Gain Error | | RFB, $V_{OUT}$ connected | | | | ±3 | LSB |
| | | RC or RB connected to $V_{OUT}$, VREF = 5V | | | | ±4½ | |
| | | RA, $V_{OUT}$ connected, VREF = 2.5V | | | | ±6 | |
| Gain Temperature Coefficient | $\Delta Gain/\Delta Temp$ | | | | ±1 | | ppm/°C |
| Reference Input Resistance | | RFB | | 8 | 12 | 16 | kΩ |
| Application Resistor Ratio Matching | | RA to RB to RC match | | | | 0.5 | % |

## ELECTRICAL CHARACTERISTICS (continued)

Dual Supply ($V_{DD}$ = +11.4V to +15.75V, $V_{SS}$ = -11.4V to -15.75V, VREF = +10V, AGND = DGND = 0V, $R_L$ = 2kΩ, $C_L$ = 100pF, all grades, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | | |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0V and $V_{DD}$ | $T_A$ = +25°C | | | ±1 | µA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±10 | |
| Input Low Voltage | $V_{IL}$ | | | | | 0.8 | V |
| Input High Voltage | $V_{IH}$ | | | 2.4 | | | V |
| Input Capacitance | $C_{IN}$ | | | | 7 | | pF |
| **POWER SUPPLIES** | | | | | | | |
| Supply Voltage | $V_{DD}$ | | | 11.40 | | 15.75 | V |
| | $V_{SS}$ | | | -11.40 | | -15.75 | |
| Supply Current | $I_{DD}$ | $V_{OUT}$ unloaded | | | | 10 | mA |
| | $I_{SS}$ | $V_{OUT}$ unloaded | | | | 4 | |
| Power-Supply Rejection | PSR | ΔGain/Δ$V_{DD}$ | VREF = -10V<br>$V_{DD}$ = 15V ± 5% | | | ±0.02 | %/% |
| | | | VREF = -8.9V<br>$V_{DD}$ = 12V ± 5% | | | | |
| | | ΔGain/Δ$V_{SS}$ | VREF = 10V<br>$V_{SS}$ = -15V ± 5% | | | ±0.02 | |
| | | | VREF = 8.9V<br>$V_{SS}$ = -12V ± 5% | | | | |
| **DYNAMIC PERFORMANCE (Note 3)** | | | | | | | |
| Output-Voltage Settling Time | $t_S$ | To ±0.01% of full scale | | | | 5 | µs |
| Slew Rate | SR | | | | 5 | | V/µs |
| DAC Glitch Impulse | | Major carry transition | | | 450 | | nV-s |
| Multiplying Feedthrough Error | | VREF = ±10V at 10kHz, DAC = all 0s | | | 5 | | $mV_{P-P}$ |
| Unity-Gain Small-Signal Bandwidth | | | | | 3 | | MHz |
| Full-Power Bandwidth | | | | | 250 | | kHz |
| Total Harmonic Distortion | THD | VREF = $6V_{RMS}$ at 1kHz | | | -90 | | dB |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Open-Loop Gain | $A_{VO}$ | RFB not connected, $V_{OUT}$ = ±10V, $R_L$ = 2kΩ | | 90 | | | dB |
| Output Resistance | $R_O$ | | | | 0.2 | | Ω |
| Short-Circuit Current | | $T_A$ = +25°C | | | 20 | | mA |
| Output Noise Voltage | | 0.1Hz to 10Hz, $T_A$ = +25°C | | | 2 | | $\mu V_{RMS}$ |
| | | f = 1kHz, $T_A$ = +25°C | | | 25 | | $nV/\sqrt{Hz}$ |

## TIMING CHARACTERISTICS (See Figures 1a, 1b)

Dual Supply ($V_{DD}$ = +11.4V to +15.75V, $V_{SS}$ = -11.4V to -15.75V, VREF = +10V, AGND = DGND = 0V, $R_L$ = 2kΩ, $C_L$ = 100pF, all grades, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Note 2)

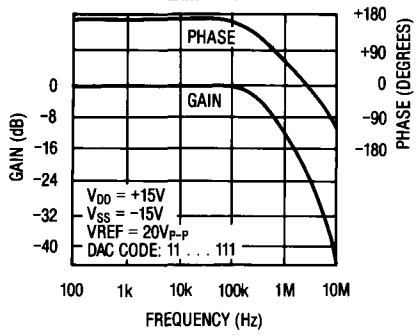
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **MAX501** | | | | | | | |
| Chip Select to Write-Setup Time | $t_{CS}$ | | | 0 | | | ns |
| Write Pulse Width | $t_{WR}$ | $T_A$ = +25°C | | 55 | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 70 | | | |
| Data-Setup Time | $t_{DS}$ | MAX501_C/E | | 50 | | | ns |
| | | MAX501_M | | 60 | | | |
| Data-Hold Time | $t_{DH}$ | | | 10 | 0 | | ns |
| $\overline{LDAC}$ Pulse Width | $t_{LDAC}$ | | | 70 | | | ns |
| $\overline{CLR}$ Pulse Width | $t_{CLR}$ | | | 70 | | | ns |
| $\overline{SET}$ Pulse Width | $t_{SET}$ | | | 200 | | | ns |
| **MAX502** | | | | | | | |
| Chip Select to Write-Setup Time | $t_{CS}$ | | | 0 | | | ns |
| Write Pulse Width | $t_{WR}$ | $T_A$ = +25°C | | 40 | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | MAX502_C/E | 50 | | | |
| | | | MAX502_M | 60 | | | |
| Data-Setup Time | $t_{DS}$ | MAX502_C/E | | 50 | | | ns |
| | | MAX502_M | | 60 | | | |
| Data-Hold Time | $t_{DH}$ | | | 10 | 0 | | ns |

**Note 2:** $V_{OUT}$ must be less than $V_{DD}$ - 2.5V and greater than $V_{SS}$ + 2.5V to ensure correct operation. Performance at supplies other than $V_{DD}$ = +15V and $V_{SS}$ = -15V is guaranteed by PSRR tests. Leave unused feedback resistors floating.

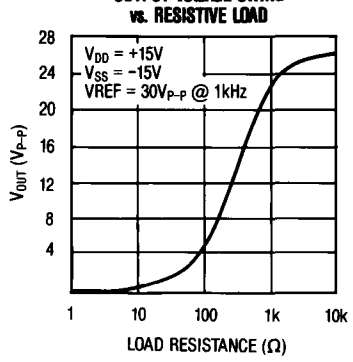
**Note 3:** Dynamic Performance and Output Characteristics are included for design guidance and are not subject to test.

## Typical Operating Characteristics

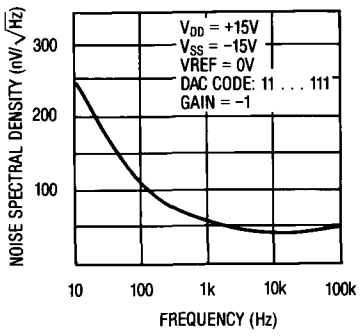
FREQUENCY RESPONSE, GAIN = -1



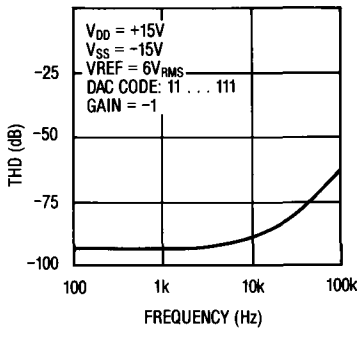

OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



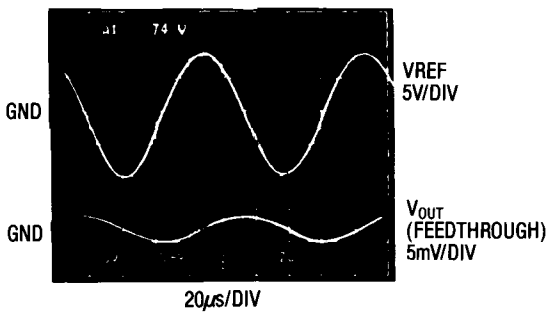

NOISE SPECTRAL DENSITY



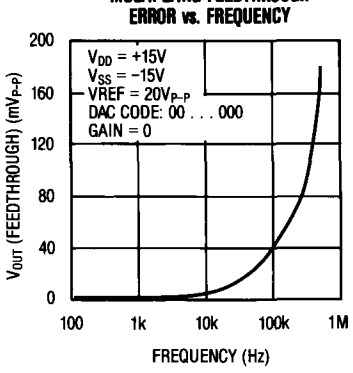

THD vs. FREQUENCY




MULTIPLYING FEEDTHROUGH ERROR




MULTIPLYING FEEDTHROUGH ERROR vs. FREQUENCY



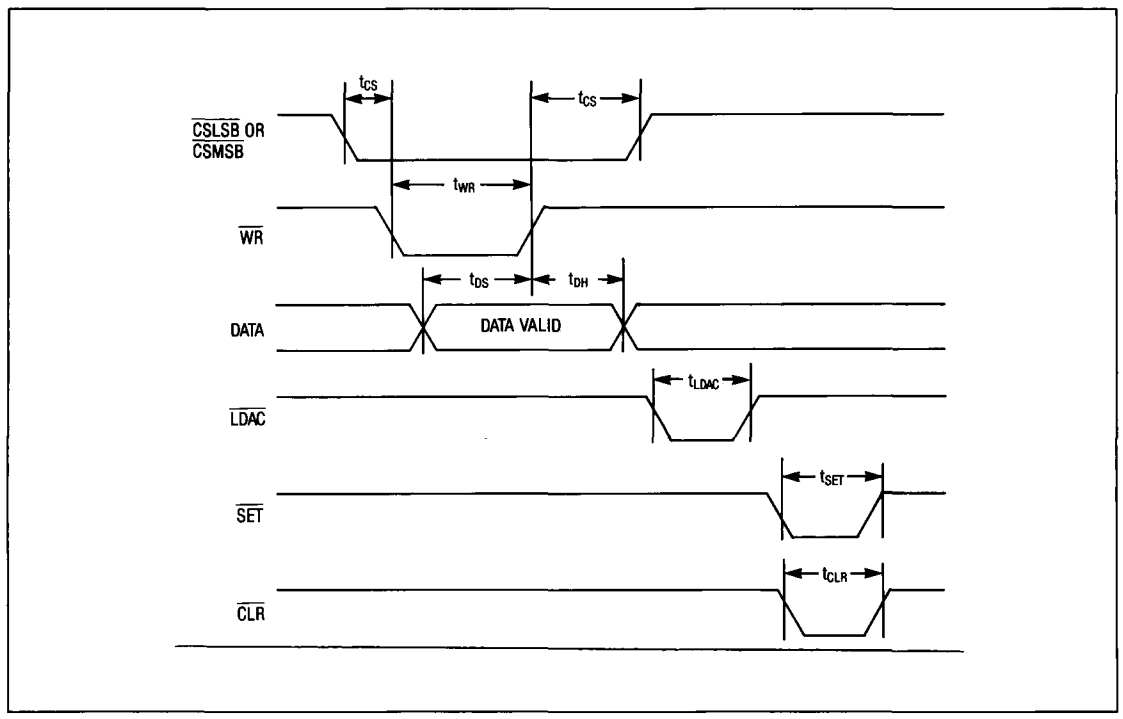



*Figure 1a. MAX501 Timing Diagram*

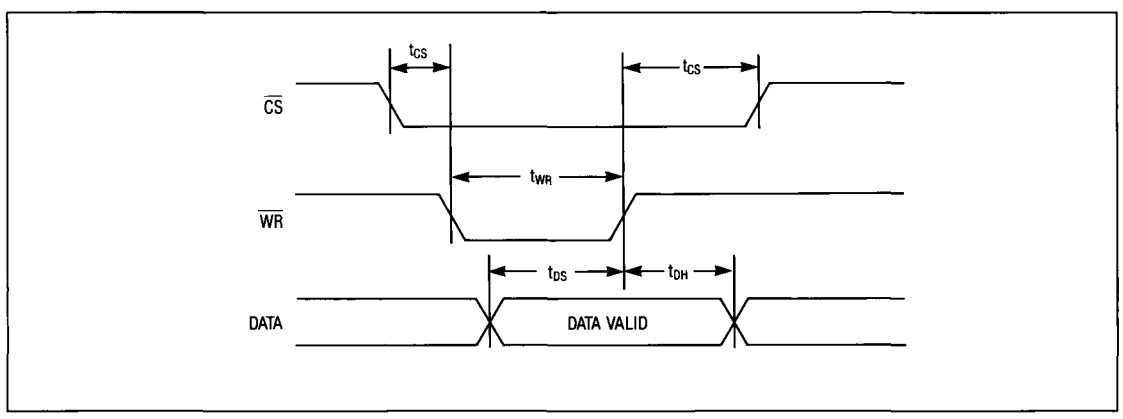



*Figure 1b. MAX502 Timing Diagram*

**NOTES:**
1. All input signal rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 20ns$.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

## Pin Descriptions

**MAX501**

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{OUT}$ | Voltage Output |
| 2 | $\overline{LDAC}$ | Asynchronous Load DAC Input is active low |
| 3 | $\overline{SET}$ | Sets DAC register to all 1s |
| 4 | $\overline{CLR}$ | Sets DAC register to all 0s |
| 5-8 | D7-D4 | Data Bits 7 to 4 |
| 9 | D3/D11 | Data Bit 3 or 11 |
| 10 | D2/D10 | Data Bit 2 or 10 |
| 11 | D1/D9 | Data Bit 1 or 9 |
| 12 | DGND | Digital Ground |
| 13 | D0/D8 | Data Bit 0 or 8 (LSB) |
| 14 | $\overline{CSLSB}$ | LSB Chip-Select Input is active low |
| 15 | $\overline{WR}$ | Write Input is active low |
| 16 | $\overline{CSMSB}$ | MSB Chip-Select Input is active low |
| 17 | VREF | Reference Input to DAC |
| 18 | AGND | Analog Ground |
| 19 | $V_{SS}$ | -12V to -15V Supply Voltage Input |
| 20 | $V_{DD}$ | +12V to +15V Supply Voltage Input |
| 21 | RA | Scaling Resistor: RA = 4RFB |
| 22 | RB | Scaling Resistor: RB = 2RFB |
| 23 | RC | Scaling Resistor: RC = 2RFB |
| 24 | RFB | Feedback Resistor |

**MAX502**

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{OUT}$ | Voltage Output |
| 2-11 | D11-D2 | Data Bits 2 to 11 (MSB) |
| 12 | DGND | Digital Ground |
| 13,14 | D1, D0 | Data Bits 0 to 1 (LSB) |
| 15 | $\overline{WR}$ | Write Input is active low |
| 16 | $\overline{CS}$ | Chip-Select Input is active low |
| 17 | VREF | Reference Input to DAC |
| 18 | AGND | Analog Ground |
| 19 | $V_{SS}$ | -12V to -15V Supply Voltage Input |
| 20 | $V_{DD}$ | +12V to +15V Supply Voltage Input |
| 21 | RA | Scaling Resistor: RA = 4RFB |
| 22 | RB | Scaling Resistor: RB = 2RFB |
| 23 | RC | Scaling Resistor: RC = 2RFB |
| 24 | RFB | Feedback Resistor |

## Detailed Description

### Digital Circuit

Figures 2a and 2b are simplified circuit diagrams of the MAX501 and MAX502 input control logic. For the MAX501, a low on $\overline{CSLSB}$ and $\overline{WR}$ with $\overline{CSMSB}$ high loads the least significant bit (LSB) byte into the input register. The LSB byte is then latched into the input register on the rising edge of either a $\overline{WR}$ or a $\overline{CSLSB}$. Similarly, a low on $\overline{CSMSB}$ and $\overline{WR}$ with $\overline{CSLSB}$ high loads the most significant bit (MSB) nibble into the input register. The MSB nibble is then latched into the input register on the rising edge of either a $\overline{WR}$ or a $\overline{CSMSB}$ pulse. With all 12 bits loaded, a low on $\overline{LDAC}$ transfers the data to the DAC register. For the MAX502, a low on $\overline{CS}$ and $\overline{WR}$ transfers the data on the input registers to the DAC latch. Both parts' digital inputs are TTL and CMOS compatible, providing easy microprocessor ($\mu$P) interfacing. Tables 1 and 2 are MAX501 and MAX502 truth tables.

**Table 1. MAX501 Truth Table**

| $\overline{WR}$ | $\overline{CSMSB}$ | $\overline{CSLSB}$ | $\overline{LDAC}$ | $\overline{CLR}$ | $\overline{SET}$ | OPERATION |
|---|---|---|---|---|---|---|
| X | X | X | X | X | 0 | DAC Register overridden by 1's<br>Input Register unaffected |
| X | X | X | X | 0 | 1 | DAC Register overridden by 0's<br>Input Register unaffected |
| 0 | 0 | 1 | 1 | 1 | 1 | Load MSB nibble into Input Register |
| 0 | 1 | 0 | 1 | 1 | 1 | Load LSB byte into Input Register |
| X | X | X | 0 | 1 | 1 | Transfer Input Register to DAC Register |
| 1 | X | X | 1 | 1 | 1 | No Operation |
| 0 | 1 | 1 | 1 | 1 | 1 | No Operation |
| 0 | R | 1 | 1 | 1 | 1 | Latching MSB nibble into Input Register |
| R | 0 | 1 | 1 | 1 | 1 | Latching MSB nibble into Input Register |
| 0 | 1 | R | 1 | 1 | 1 | Latching LSB byte into Input Register |
| R | 1 | 0 | 1 | 1 | 1 | Latching LSB byte into Input Register |

H = High State, L = Low State, R = Rising Edge, X = Don't Care

**Table 2. MAX502 Truth Table**

| $\overline{WR}$ | $\overline{CS}$ | OPERATION |
|---|---|---|
| H | X | No Operation |
| X | H | No Operation |
| L | L | Input Register is Transparent |
| L | R | Input Register is Latched |
| R | L | Input Register is Latched |

H = High State, L = Low State, R = Rising Edge, X = Don't Care

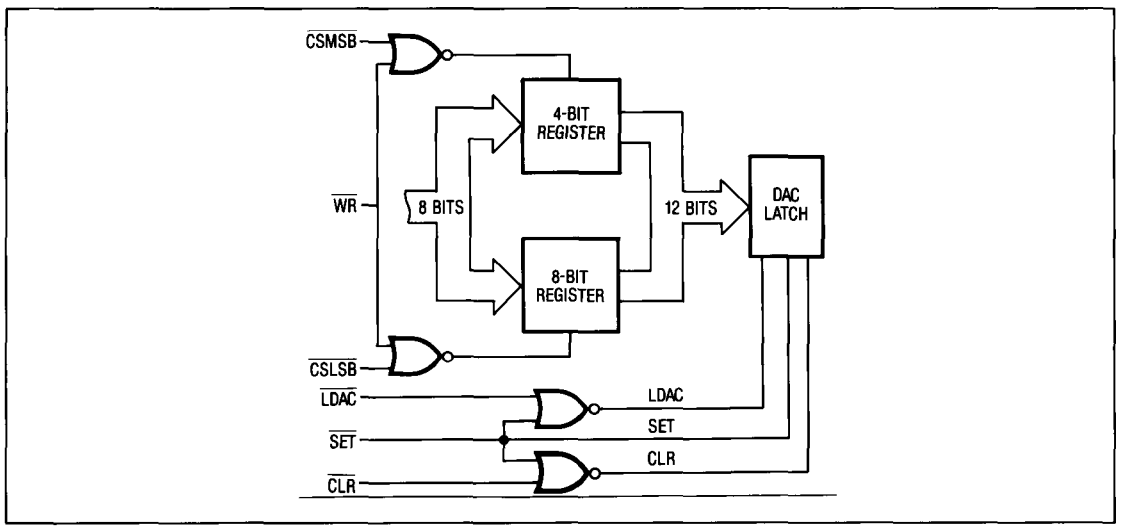



*Figure 2a. MAX501 Input Control Logic*

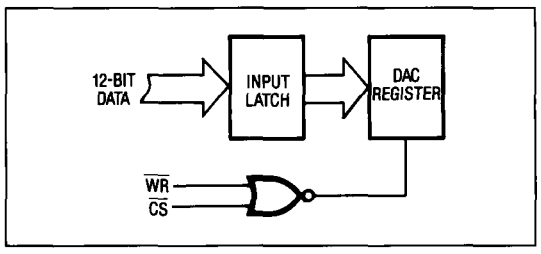



*Figure 2b. MAX502 Input Control Logic*

### Digital-to-Analog Converter

The MAX501/MAX502 have a 12-bit, binary-weighted, current-output DAC with standard R-2R ladder (Figure 3). Binarily weighted currents are switched between AGND and the inverting input of the internal output amplifier. The output amplifier, typically connected to the feedback resistor RFB, converts the output current to a voltage. With RFB connected to VOUT,

$$V_{OUT} = -D \times VREF,$$

where D is the fractional expression of the digital input code divided by full scale. D can vary from 0 to 4095/4096 in unipolar mode.

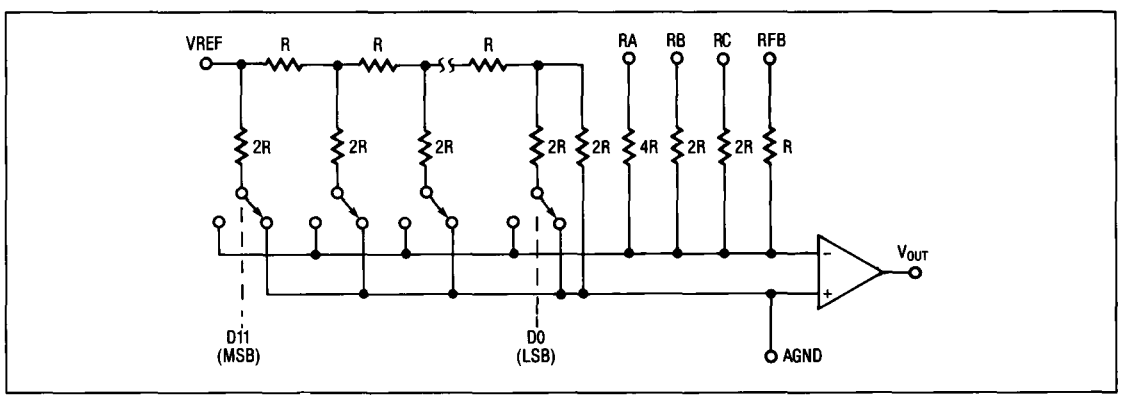



*Figure 3. MAX501/MAX502 Simplified DAC and Amplifier Circuit*

### Output-Buffer Amplifier

The output amplifier is an internally compensated, non-inverting, gain-scalable amplifier that can develop ±10V across a 2kΩ load. Maximum settling time is less than 5µs (to within 0.01% FSR). Input offset voltage is laser trimmed at the wafer level. Slew rate is typically 7V/µs. The gain-setting resistors (RA, RB, and RC) connect to the amplifier inverting terminal. Float unused gain-setting resistors.

### Unipolar Configuration

Figure 4, a typical configuration for the MAX501/MAX502, provides for unipolar-bipolar operation or two-quadrant multiplication when $V_{IN}$ is an AC signal. R1 adjusts gain and R3 adjusts zero offset. For fixed-reference applications, trim the reference voltage and omit R1 and R2. If R1 and R2 are included, you must take into account their gain-temperature coefficient. The typical gain-temperature coefficient of the MAX502 is 1ppm/°C, which corresponds to a gain shift of 1/2LSB over a +100°C temperature range. Table 3 is the code table for unipolar-binary operation.

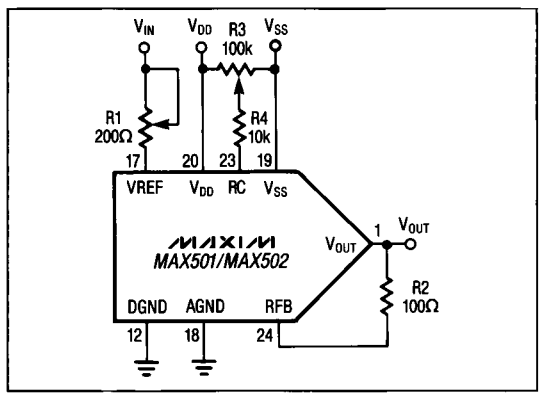



*Figure 4. Unipolar-Binary Operation (2-Quadrant Multiplication)*

**Table 3. MAX501/MAX502 Unipolar-Binary Code Table**

| DIGITAL INPUT | | | ANALOG OUTPUT |
|---|---|---|---|
| 1111 | 1111 | 1111 | $(-V_{IN})\frac{4095}{4096}$ |
| 1000 | 0000 | 0000 | $(-V_{IN})\frac{2048}{4096} = -\frac{1}{2}V_{IN}$ |
| 0000 | 0000 | 0001 | $(-V_{IN})\frac{1}{4096}$ |
| 0000 | 0000 | 0000 | 0V |

### Bipolar Operation

**Figure 5 shows a 4-quadrant, bipolar operation. Gain error may be adjusted by changing the R1 and R2 ratio. These resistors should be ratio-matched to 0.01% to stay within gain-error specifications and to eliminate trimming. The offset value is defined by matching the RB and RC internal resistors. Table 4 is the code table for bipolar-binary operation.**

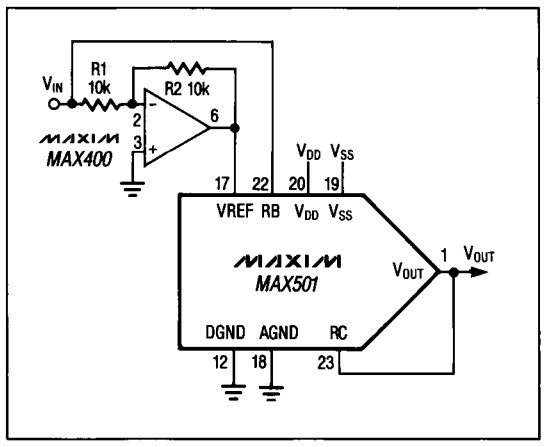



*Figure 5. Bipolar Operation (4-Quadrant Multiplication)*

**Table 4. MAX501/MAX502 Bipolar-Binary Code Table**

| DIGITAL INPUT | | | ANALOG OUTPUT |
|---|---|---|---|
| 1111 | 1111 | 1111 | $(+V_{IN})\frac{2047}{2048}$ |
| 1000 | 0000 | 0001 | $(+V_{IN})\frac{1}{2048}$ |
| 1000 | 0000 | 0000 | 0V |
| 0111 | 1111 | 1111 | $(-V_{IN})\frac{1}{2048}$ |
| 0000 | 0000 | 0000 | $(-V_{IN})\frac{2048}{2048} = V_{IN-}$ |

## Applications Information

### Noise

AC or transient voltages between AGND and DGND can cause noise injection into the analog output. Tie the MAX502 AGND to DGND to ensure both pins are at the same potential. If these ground pins connect to separate backplanes, use two back-to-back diodes to tie the pins together. Also, decouple $V_{DD}$ and $V_{SS}$ to AGND, as µP-based systems generally have noisy grounds that couple into the power supplies.

### Digital Glitches

Any digital word written into the DAC causes a glitch impulse. This impulse couples across the stray capacitance of the DAC switches to the output bus. A glitch impulse on this bus is converted to a voltage by RFB and the output amplifier. The output voltage glitch energy is the product of its duration and its average magnitude (the net area under the curve), and is expressed in (nV)(s). The energy is measured with VREF connected to analog ground and the DAC register alternately loaded with all 0s and all 1s.

### Digital Feedthrough

Most of the MAX501/MAX502's digital inputs are directly connected to the µP bus. These inputs are constantly changing, even when the DAC is not selected. High-frequency logic activity on the data bus can feed through the DAC package capacitance as noise on the DAC output. Figure 6 shows an interface that minimizes digital feedthrough. All data inputs are latched from the busy by $\overline{CS}$. Alternatively, using peripheral interface devices reduces digital feedthrough.

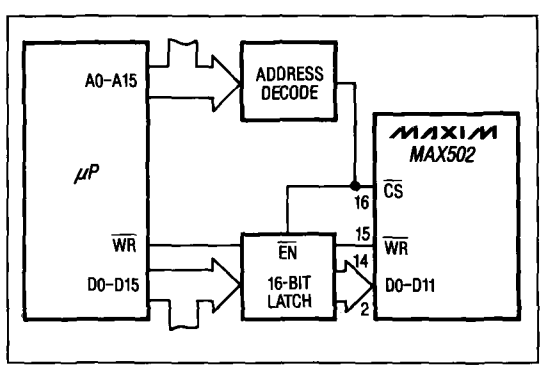



*Figure 6. MAX502 Interface Circuit — Latches Minimize Digital Feedthrough*

## MAX502 Microprocessor Interfacing

### 16-Bit Microprocessor Systems

Figures 7-9 show the MAX502 interfaced with the MC68000, the 8086, and the TMS32010. The MAX502 appears as a memory-mapped peripheral to the processors. In each case, a write instruction loads the MAX502 with the appropriate data. The particular instructions used are as follows:

MC68000: MOVE
8086: MOV
TMS32010: OUT

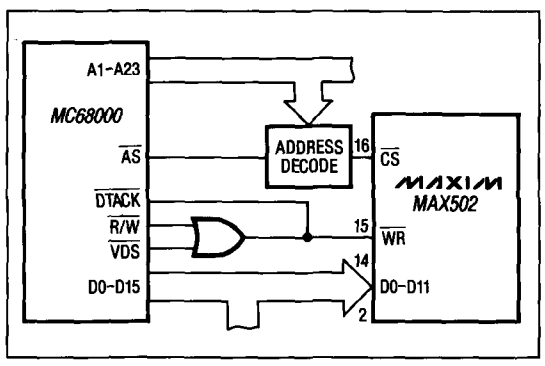



*Figure 7. MAX502 to MC6800 Interface*

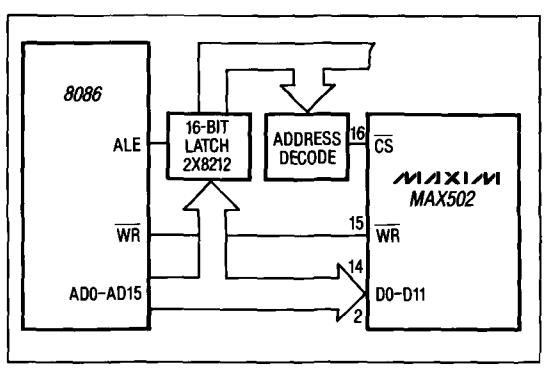



*Figure 8. MAX502 to 8086 Interface*

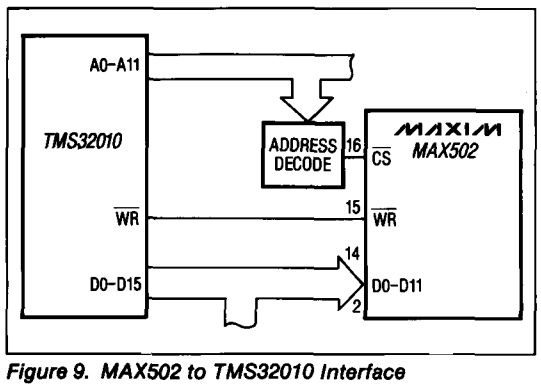



*Figure 9. MAX502 to TMS32010 Interface*

### MAX501 Microprocessor Interfacing

#### 8-Bit Microprocessor Systems

Figure 10 shows an interface circuit for the MAX501 to the 8085A 8-bit μP. The software routine to load data to the device is given in Table 3. Note that transferring 12 data bits requires two write operations. The first of these loads the 4 MSBs into the 7475 latch. The second write operation loads the 8 LSBs plus the 4 MSBs (which are held by the latch) into the DAC.

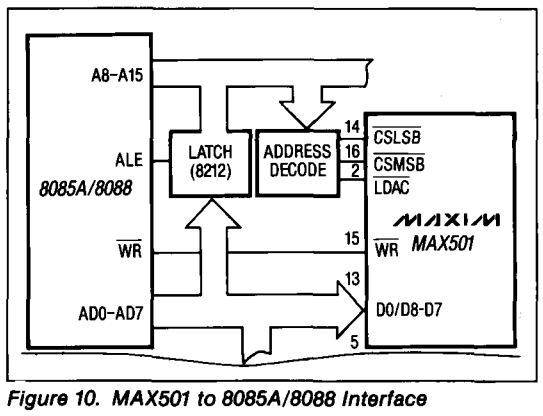
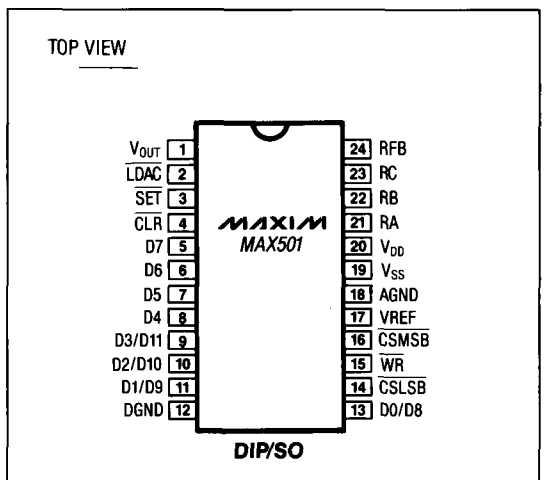



*Figure 10. MAX501 to 8085A/8088 Interface*

## Pin Configurations (continued)




DIP/SO

## Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE | ERROR (LSBs) |
|---|---|---|---|
| MAX502ACNG | 0°C to +70°C | 24 Narrow Plastic DIP | 1/2 |
| MAX502BCNG | 0°C to +70°C | 24 Narrow Plastic DIP | 3/4 |
| MAX502ACWG | 0°C to +70°C | 24 Wide SO | 1/2 |
| MAX502BCWG | 0°C to +70°C | 24 Wide SO | 3/4 |
| MAX502BC/D | 0°C to +70°C | Dice* | 3/4 |
| MAX502AENG | -40°C to +85°C | 24 Narrow Plastic DIP | 1/2 |
| MAX502BENG | -40°C to +85°C | 24 Narrow Plastic DIP | 3/4 |
| MAX502AEWG | -40°C to +85°C | 24 Wide SO | 1/2 |
| MAX502BEWG | -40°C to +85°C | 24 Wide SO | 3/4 |
| MAX502AMRG | -55°C to +125°C | 24 Narrow CERDIP** | 1/2 |
| MAX502BMRG | -55°C to +125°C | 24 Narrow CERDIP** | 3/4 |

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*