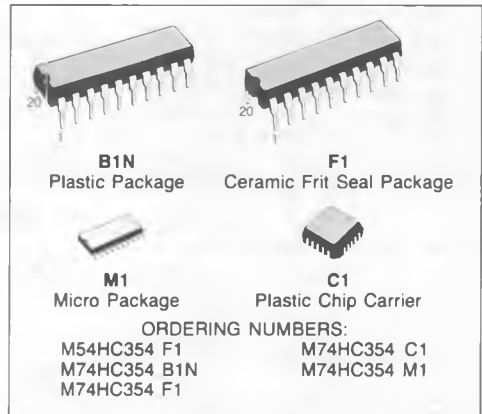


8-CHANNEL MULTIPLEXER/REGISTER (3-STATE)

- **HIGH SPEED**
 $t_{PD} = 33 \text{ ns (TYP.) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 15 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS354



DESCRIPTION

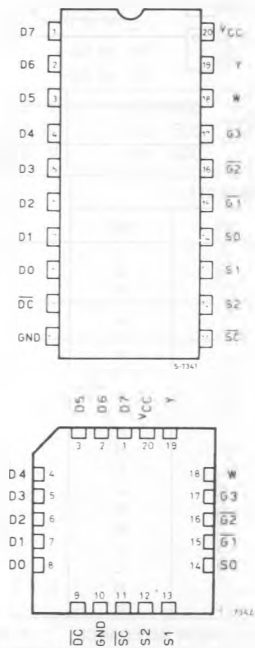
The M54/74HC354 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-state) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.

This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data.

The information at the data inputs (D0 to D7) is stored in the 8-bit latch at the negative pulse on \overline{DC} input. The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on \overline{SC} input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system.

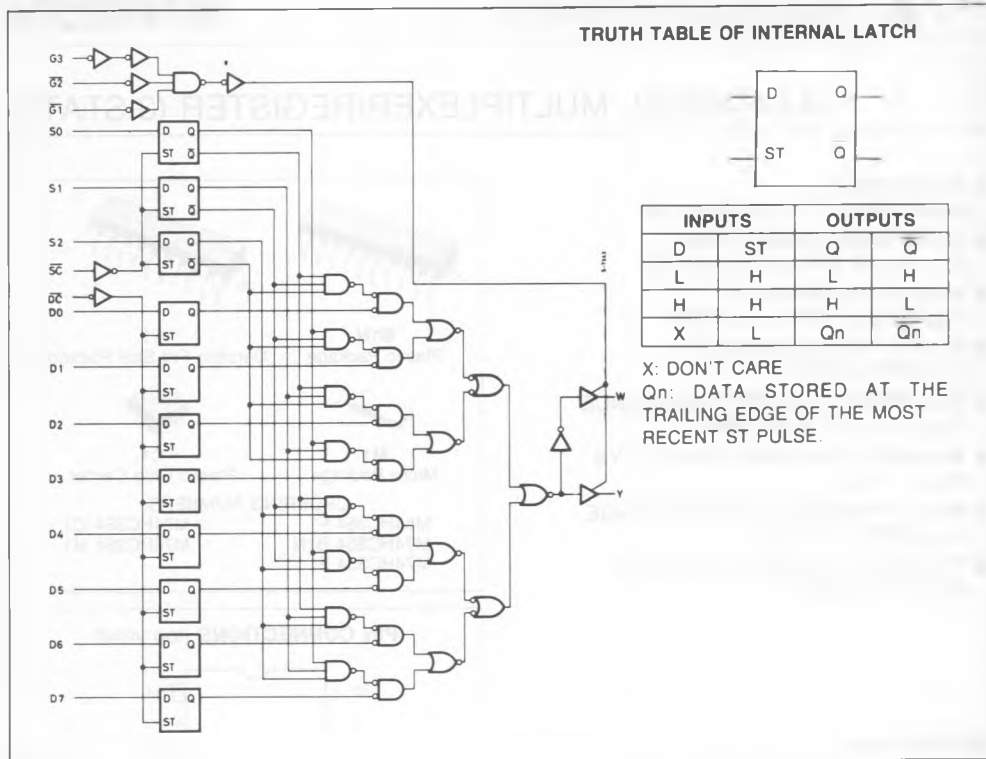
The M54/74HC354 is similar in function to the M54/74HC356, which has an 8-bit flip-flop as the data register instead of an 8-bit latch. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

LOGIC DIAGRAM



TRUTH TABLE

SELECT*			INPUTS			OUTPUT ENABLES			OUTPUTS	
S2	S1	S0	\overline{DC}	$\overline{G1}$, $\overline{G2}$, $\overline{G3}$			W	Y		
				X	X	X			X	H
X	X	X	X	X	X	X	Z	Z		
X	X	X	X	X	X	L	Z	Z		
L	L	L	L	L	L	H	D0	D0		
L	L	L	L	L	L	H	D0n	D0n		
L	L	L	L	L	L	H	D1	D1		
L	L	L	L	L	L	H	D1n	D1n		
L	L	L	L	L	L	H	D2	D2		
L	L	L	L	L	L	H	D2n	D2n		
L	L	L	L	L	L	H	D3	D3		
L	L	L	L	L	L	H	D3n	D3n		
L	L	L	L	L	L	H	D4	D4		
L	L	L	L	L	L	H	D4n	D4n		
L	L	L	L	L	L	H	D5	D5		
L	L	L	L	L	L	H	D5n	D5n		
L	L	L	L	L	L	H	D6	D6		
L	L	L	L	L	L	H	D6n	D6n		
L	L	L	L	L	L	H	D7	D7		
L	L	L	L	L	L	H	D7n	D7n		

X: DON'T CARE - Z: HIGH IMPEDANCE * : THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH SC LOW.
D0n.....D7n: THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7, RESPECTIVELY, BEFORE THE MOST RECENT OF THE LOW-TO-HIGH TRANSITION OF DATA CONTROL.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to 150	$^{\circ}C$

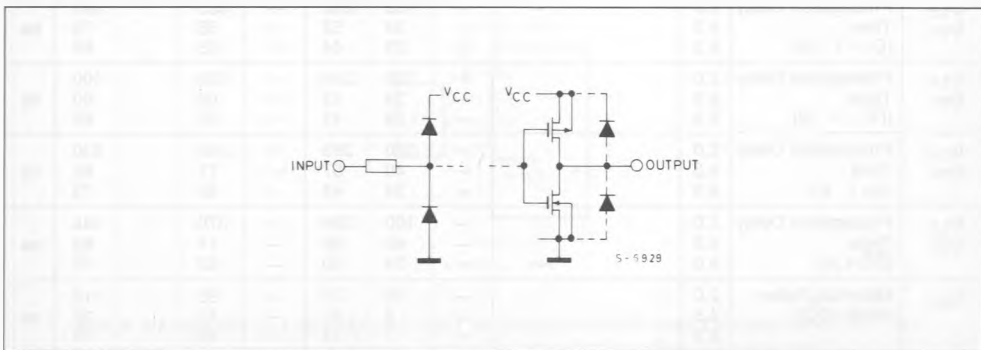
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: \cong 65 $^{\circ}C$ derate to 300 mW by 10 mW/ $^{\circ}C$: 65 $^{\circ}C$ to 85 $^{\circ}C$.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_A	Operating Temperature	74HC Series 54HC Series	-40 to 85 -55 to 125	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	- 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5			4.18	4.31	—	4.13	—	4.10	—	
		6.0			5.68	5.8	—	5.63	—	5.60	—	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I _{OZ}	3 State Output Off-State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND		—	—	±0.5	—	±5	—	±10	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0			—	25	60	—	75	—	90	ns
		4.5			—	7	12	—	15	—	18	
		6.0			—	6	10	—	13	—	15	
t _{PLH} t _{PHL}	Propagation Delay Time (Dn - Y, W)	2.0			—	135	260	—	325	—	390	ns
		4.5			—	34	52	—	65	—	78	
		6.0			—	29	44	—	55	—	66	
t _{PLH} t _{PHL}	Propagation Delay Time (DC - Y, W)	2.0			—	135	265	—	335	—	400	ns
		4.5			—	34	53	—	66	—	80	
		6.0			—	29	45	—	56	—	68	
t _{PLH} t _{PHL}	Propagation Delay Time (Sn-Y, W)	2.0			—	160	285	—	355	—	430	ns
		4.5			—	40	57	—	71	—	86	
		6.0			—	34	48	—	60	—	73	
t _{PLH} t _{PHL}	Propagation Delay Time (SC-Y,N)	2.0			—	160	295	—	370	—	445	ns
		4.5			—	40	59	—	74	—	89	
		6.0			—	34	50	—	63	—	76	
t _{W(L)}	Minimum Pulse Width (DC)	2.0			—	30	75	—	95	—	110	ns
		4.5			—	8	15	—	19	—	22	
		6.0			—	7	13	—	16	—	19	

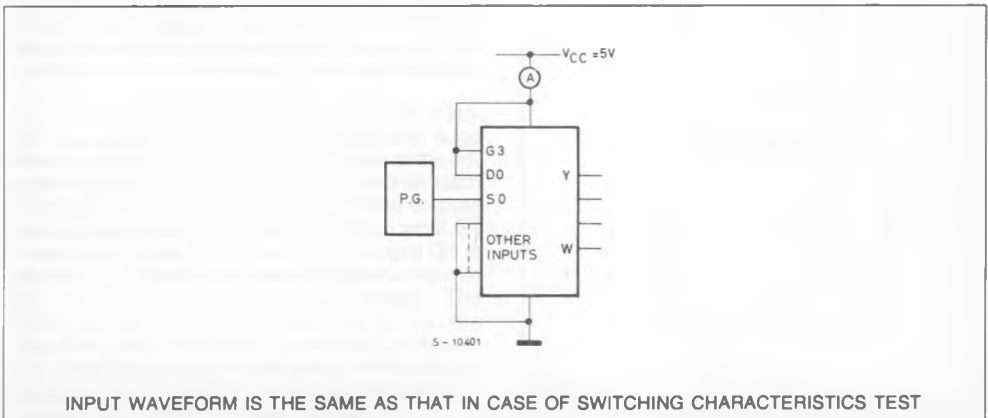
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{W(L)}	Minimum Pulse Width (SC)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t _S	Minimum Set-up Time (Sn)	2.0		—	20	75	—	95		110	ns
		4.5		—	5	15	—	19		22	
		6.0		—	4	13	—	16		19	
t _S	Minimum Set-up Time (Dn)	2.0		—	25	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
t _H	Minimum Hold Time (Sn)	2.0		—	—	5	—	5		5	ns
		4.5		—	—	5	—	5		5	
		6.0		—	—	5	—	5	—	5	
t _H	Minimum Hold Time (Dn)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t _{PZL} t _{PHZ}	Output Enable Time	2.0		—	68	125	—	155		190	
		4.5		—	17	25	—	31		38	
		6.0	R _L = 1kΩ	—	15	21	—	26		32	
t _{PLZ} t _{PHZ}	Output Disable Time	2.0		—	60	155	—	195		235	ns
		4.5		—	22	31	—	39		47	
		6.0	R _L = 1kΩ	—	20	26	—	33		40	
C _{IN}	Input Capacitance			—	5	10	—	10		10	
C _{OUT}	Output Capacitance			—	10	—	—	—			pF
C _{PD} (*)	Power Dissipation Capacitance			—	84	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation.

$$I_{CC}(\text{Opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TEST CIRCUIT I_{CC} (Opr.)

SWITCHING CHARACTERISTICS TEST WAVEFORM

