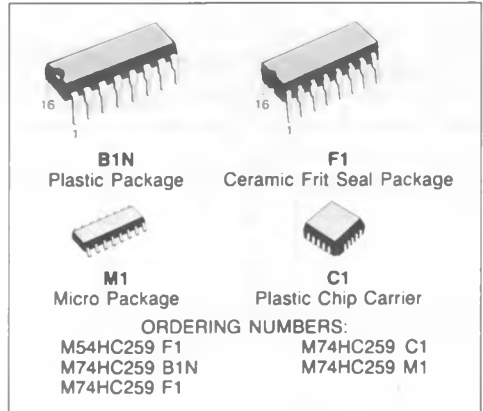


8 BIT ADDRESSABLE LATCH

- **HIGH SPEED**
 $t_{PD} = 13 \text{ ns (TYP.)}$ at $V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A \text{ (MAX.)}$ at $T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS259



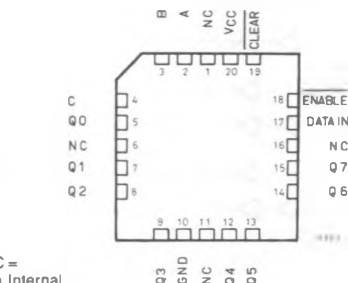
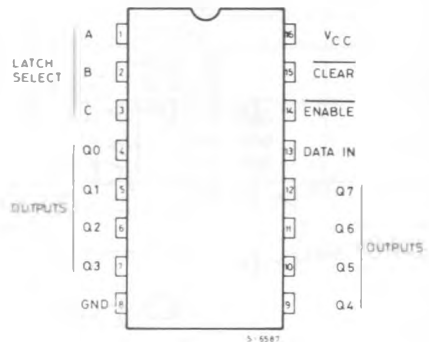
DESCRIPTION

The M54/74HC259 is a high speed CMOS 8 BIT ADDRESSABLE LATCH fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54HC259/M74HC259 has single data input (D) 8 latch outputs (Q0-Q7), 3 address inputs (A, B, and C), common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addresses output. The data is stored on the positive-going edge of the ENABLE pulse. All unaddressed latches will remain unaffected. With ENABLE in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the ENABLE should be held high (inactive) while the address lines are changing. If ENABLE is held high and CLEAR is taken low all eight latches are cleared to the low state. If ENABLE is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to 8 line decoder.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

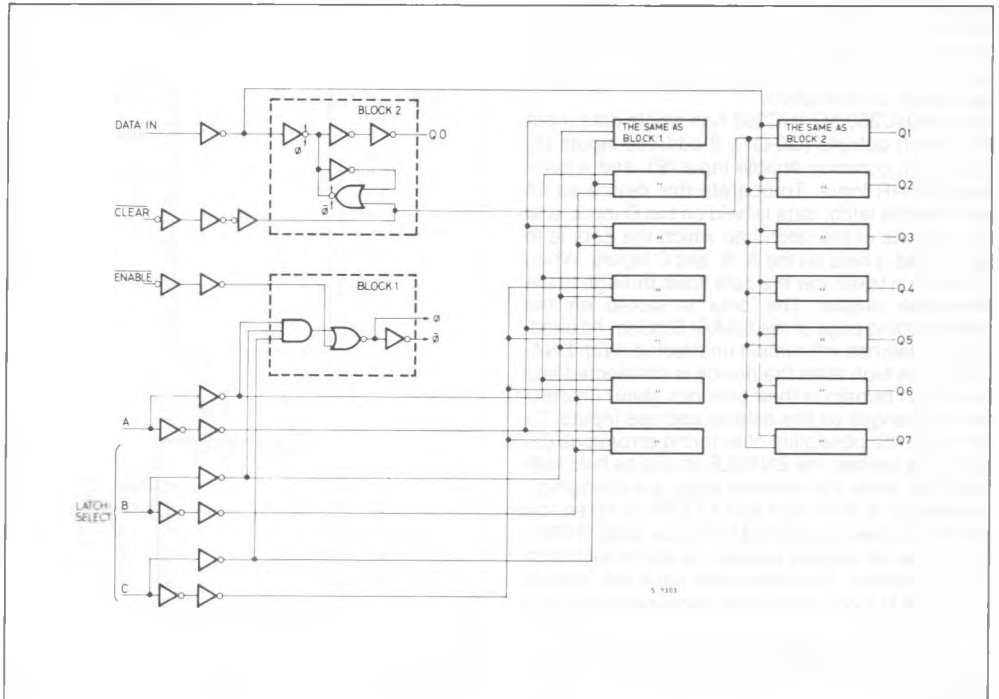
TRUTH TABLE

INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	\bar{G}			
H	L	D	Qi0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO 'L'

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D: THE LEVEL AT THE DATA INPUT
 Qi0: THE LEVEL BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED, (i= 0,1,.....,7).

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to 150	$^{\circ}C$

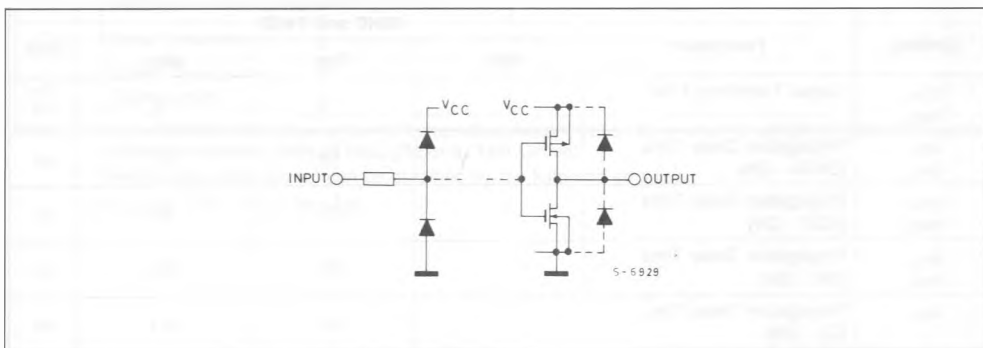
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: \cong 65 $^{\circ}C$ derate to 300 mW by 10 mW/ $^{\circ}C$: 65 $^{\circ}C$ to 85 $^{\circ}C$.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	-40 to 85 -55 to 125	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V _{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	- 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		- 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
6.0		- 5.2 mA	5.68	5.8	—	5.63	—	5.60	—			
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5		—	0.0	0.1	—	0.1	—	0.1		
		6.0		—	0.0	0.1	—	0.1	—	0.1		
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
6.0	5.2 mA	—	0.18	0.26	—	0.33	—	0.40				
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (DATA - QN)		13	21	ns
t _{PLH} t _{PHL}	Propagation Delay Time (ADD - QN)		21	33	ns
t _{PLH} t _{PHL}	Propagation Delay Time (EN - QN)		18	29	ns
t _{PHL}	Propagation Delay Time (CL - QN)		14	23	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	22 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - QN)	2.0 4.5 6.0		— — —	73 16 14	130 26 22	— — —	165 33 28	— — —	195 39 33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ADD - QN)	2.0 4.5 6.0		— — —	115 24 21	190 38 32	— — —	240 48 41	— — —	285 57 48	ns
t_{PLH} t_{PHL}	Propagation Delay Time (EN - QN)	2.0 4.5 6.0		— — —	100 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
t_{PHL}	Propagation Delay Time (CL - QN)	2.0 4.5 6.0		— — —	80 17 15	135 27 23	— — —	170 34 29	— — —	205 41 35	ns
$t_{W(L)}$	Minimum Pulse Width (CL)	2.0 4.5 6.0		— — —	33 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width (EN)	2.0 4.5 6.0		— — —	35 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (DATA)	2.0 4.5 6.0		— — —	15 3 3	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t_s	Minimum Set-up Time (ADD)	2.0 4.5 6.0		— — —	— — —	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
t_h	Minimum Hold Time (DATA)	2.0 4.5 6.0		— — —	— — —	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
t_h	Minimum Hold Time (ADD)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	73	—	—	—			pF

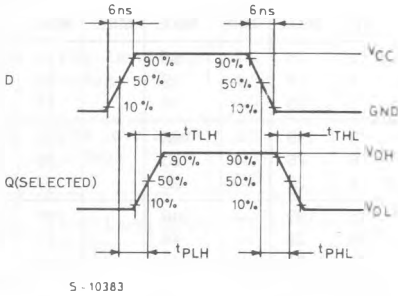
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation.

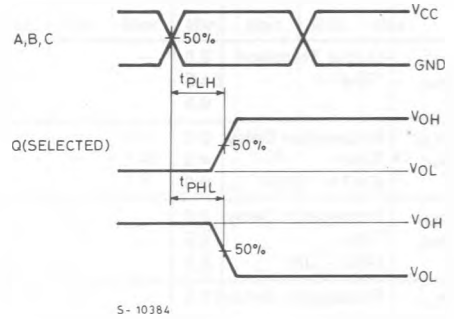
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

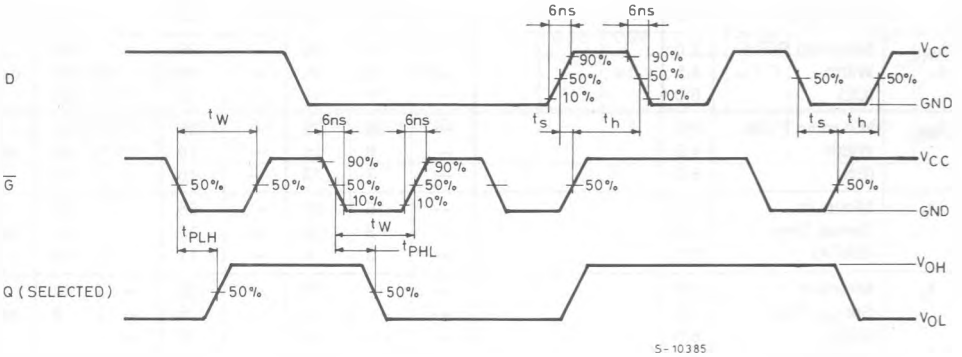
WAVEFORM 1. ($\overline{G} = L, \overline{CLR} = H, A - C = \text{STABLE}$)



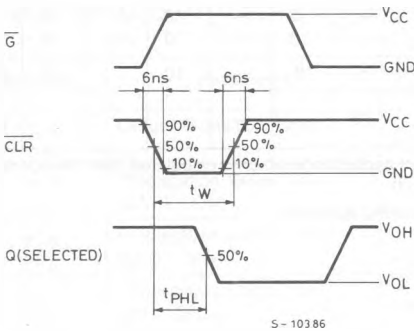
WAVEFORM 2. ($\overline{G} = L$)



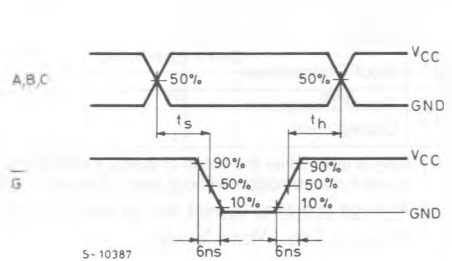
WAVEFORM 3. ($\overline{CLR} = H, A - C = \text{STABLE}$)



WAVEFORM 4. ($D = H, A - C = \text{STABLE}$)



WAVEFORM 5. ($\overline{CLR} = H$)



TEST CIRCUIT I_{CC} (Opr.)