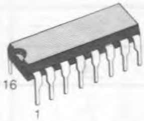
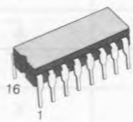
DUAL MONOSTABLE MULTIVIBRATORS

- HIGH SPEED
  t_{PD} = 32 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC} = 4 μA (MAX.) at T_A = 25°C
  ACTIVE STATE I_{CC} = 200 μA (TYP) at V_{CC} = 5V
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 150ns ~ 60s over at V_{CC} = 4.5V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS221



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC221 F1
M74HC221 B1N
M74HC221 F1
M74HC221 C1
M74HC221 M1

DESCRIPTION

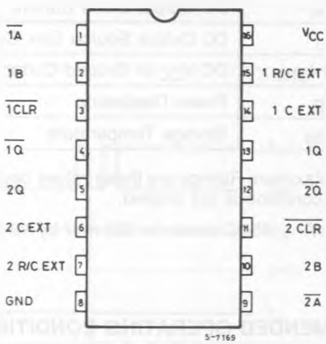
The M54/74HC221 is a high speed CMOS MONOSTABLE multivibrator fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for rising/falling signals, (t_r-t_f-l sec).
The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx. Taking CLR low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx:

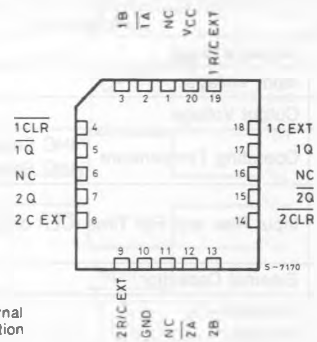
Cx : NO LIMIT

Rx : V_{CC} = 2.0V 5KΩ to 1MΩ
V_{CC} = 3.0V 1KΩ to 1MΩ

All inputs are equipped with protection circuits against static discharge and transient excess voltage

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L ▲	H ▲	INHIBIT
H	X	H	L ▲	H ▲	INHIBIT
L	↑	H	⊓	⊔	OUTPUT ENABLE
L	H	↑	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: DON'T CARE
▲: EXCEPT FOR MONOSTABLE PERIOD

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	DC Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	– 65 to 150	°C

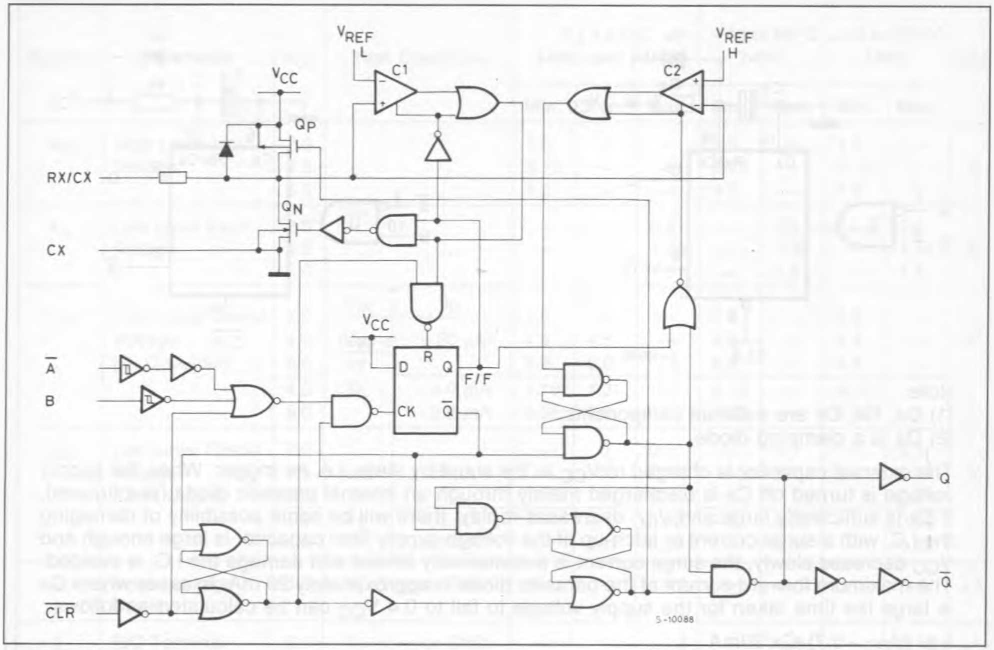
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

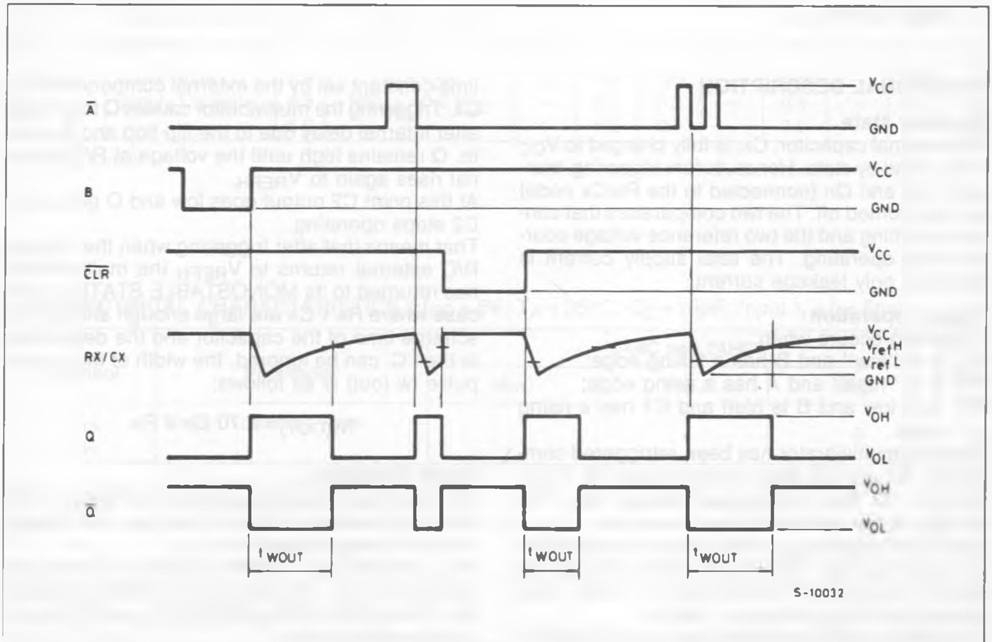
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	– 40 to 85 – 55 to 125	°C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ only)	V_{CC} 2 V: 0 to 1000 4.5V: 0 to 500 6 V: 0 to 400	ns
Cx	External Capacitor	NO LIMITATION	F
Rx	External Resistor	V_{CC} 3 V: 5K to 1M 3 V: 1K to 1M	Ω

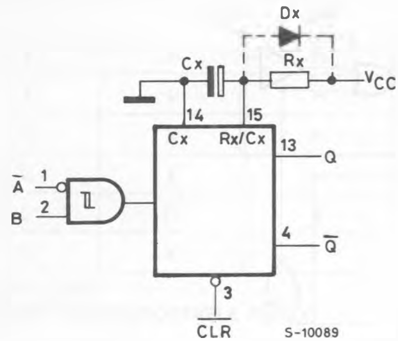
LOGIC DIAGRAM

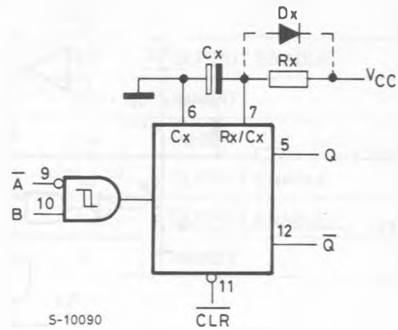


TIMING CHART



BLOCK DIAGRAM





Note:
(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:

$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

Stand-by state

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

Trigger operation

Triggering occurs when:
1st) A is "low" and B has a falling edge;
2nd) B is "high" and A has a rising edge;
3rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.
When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off. At this point C1 stops functioning but C2 continues to operate.
The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx. Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}.
At this point C2 output goes low and O goes low. C2 stops operating.
That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx • Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows:

$$t_{W(OUT)} = 0.70\ Cx \cdot Rx$$

Reset Operation

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.
Also transistor Qp is turned on and Cx is charged quickly to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage (Q, Q Output)		V_{IN}	I_O								V
		2.0	V_{IH} or V_{IL}	−20 μA	1.9	2.0	—	1.9	—	1.9	—	
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_I	R/C Terminal Off-State Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}'	Active-State (1) Supply Current	2.0	$V_I = V_{CC}$ $R/C_{ext} = 0.5\ V_{CC}$		—	40	120	—	160	—	200	μA
		4.5			—	0.1	0.3	—	0.4	—	0.5	mA
		6.0			—	0.2	0.6	—	0.8	—	1.0	mA

(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

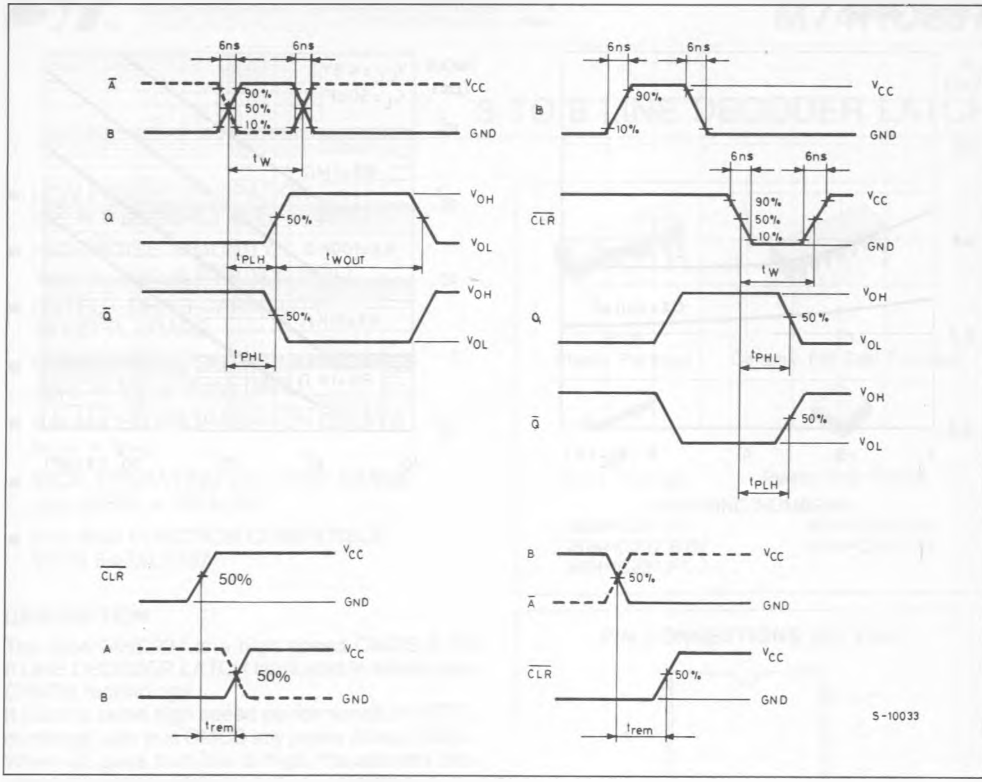
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B TRIGGER - Q, $\overline{Q}$)		32	49	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\overline{Q}$)		35	55	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)		23	37	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

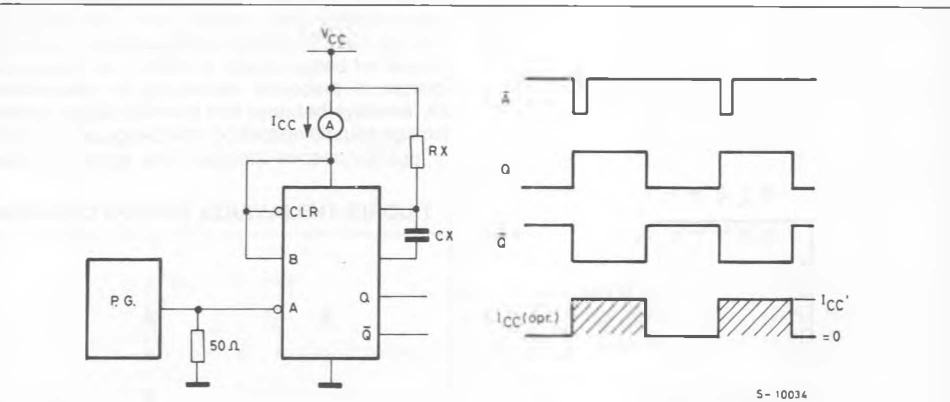
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$,B TRIG. - Q,$\overline{Q}$)	2.0 4.5 6.0		— — —	144 36 31	280 56 48	— — —	350 70 60	— — —	420 84 71	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIG. - Q,$\overline{Q}$)	2.0 4.5 6.0		— — —	164 41 35	310 62 53	— — —	390 78 66	— — —	465 95 79	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q,$\overline{Q}$)	2.0 4.5 6.0		— — —	108 27 23	210 42 36	— — —	265 53 45	— — —	315 63 54	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Trigger Pulse Width	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Clear Pulse Width	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$\Delta t_{W(OUT)}$	Output Pulse Width Error. Between Circuits in Same Package			—	±1	—	—	—	—	—	%
t_{REM}	Minimum Removal Time ($\overline{A}$,B TRIGGER)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time ($\overline{CLR}$ TRIGGER)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{WOUT} (Min).	Minimum Output Pulse Width	2.0 4.5 6.0	Cx = 0pF Rx = 5kpFΩ(V_{CC} = 2V) Rx = 1kΩ(V_{CC} = 4.5,6V)	— — —	490 190 170	1450 290 260	— — —	1825 365 325	— — —	2185 437 373	ns
t_{WOUT}	Output Pulse Width	2.0 4.5 6.0	Cx = 0.01μF Rx = 10kΩ	72 72 72	85 80 80	98 88 88	72 72 72	98 88 88	72 72 72	98 88 88	μs
		2.0 4.5 6.0	Cx = 0.1μF Rx = 10kΩ	0.67 0.67 0.67	0.75 0.73 0.73	0.83 0.79 0.79	0.67 0.67 0.67	0.83 0.79 0.79	0.67 0.67 0.67	0.83 0.79 0.79	ms
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	109	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit). Average operating current can be obtained by equation hereunder:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per monostable) (I_{CC}': Active Supply Current, Duty: %)

SWITCHING CHARACTERISTICS TEST WAVEFORM

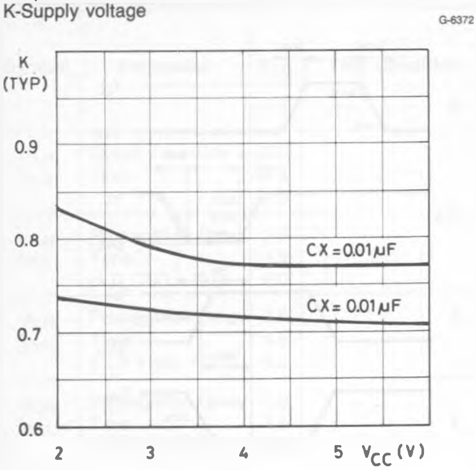


TEST WAVEFORM



Input Transition Time: 6ns
$V_{IH} = V_{CC}$, $V_{IL} = GND$

Output Pulse Width Constant
K-Supply voltage



t_WOUT-Cx Characteristics (Typ).