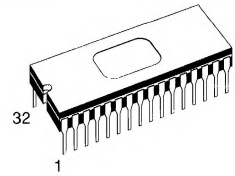
SGS-THOMSON MICROELECTRONICS

M27C2001

2048K (256K x 8) CMOS UV EPROM

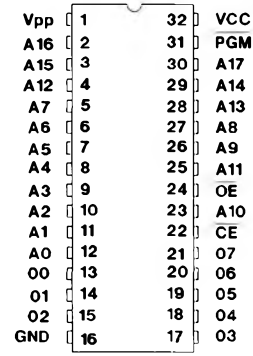
- VERY FAST ACCESS TIME : 120 ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 35 mA
  - Stand by current 200 µA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 24 SECONDS (PRESTO II ALGORITHM).



FDIP32-W

(Ordering information at the end of the datasheet)

Figure 1 : Pin Connection



DESCRIPTION

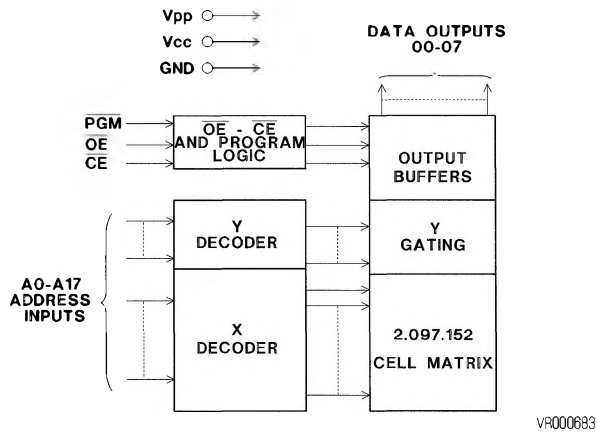
The M27C2001 is a high speed 2,097,152 (organized 262,144 X 8) bit ultraviolet erasable and programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

It is housed in a 32 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

PIN FUNCTIONS

A0-A17	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
O0-O7	DATA INPUT/OUTPUT
NC	NO CONNECTION
V_{CC}	+5V POWER SUPPLY
V_{PP}	PROGRAMMING VOLTAGE

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output Voltages with respect to Ground	-0.6 to + 7.0	V
V_{PP}	Supply Voltage with respect to Ground	-0.6 to + 14.0	V
V_{A9}	Voltage on A9 with respect to Ground	-0.6 to + 13.5	V
V_{CC}	Supply Voltage with respect to Ground	-0.6 to + 7.0	V
T_{bias}	Temperature range under bias	-50 to + 125	°C
T_{stg}	Storage temperature range	- 65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	OUTPUT
READ	L	L	X	X	X	D_{OUT}
OUTPUT DISABLE	L	H	X	X	X	HIGH Z
STANDBY	H	X	X	X	X	HIGH Z
PROGRAM	L	H	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTE : X = Don't Care ; VH = 12V ± 0.5V ; H = High ; L = Low

READ OPERATION
DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for O°C to 70°C Oper. Temp. Range)	**12XF1, 15XF1, 20XF1, 25XF1**		**12F1, 15F1, 20F1, 25F1**	
V_{CC} Power Supply (1)	5V ± 5%		5V ± 10%	

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		35	mA
I_{CC2}	VCC Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	VCC Standby Current - CMOS	$\overline{CE}$ > V_{CC} -0.2 V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input low voltage		-0.3	0.8	V
V_{IH}	Input high voltage		2.0	V_{CC}+ 1.0	V
V_{OL}	Output Low voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC} - 0.7		V V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27C2001								Unit
			-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		50		60		70		100	ns
t_{DF} (2)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	40	0	50	0	60	0	60	ns
t_{OH}	Output hold from address	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		ns

CAPACITANCE (3)

(T_A = 25°C, f = 1MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} Must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

Output Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2v - Outputs : 0.8 and 2v

Figure 3 : AC Testing input/Output Waveform

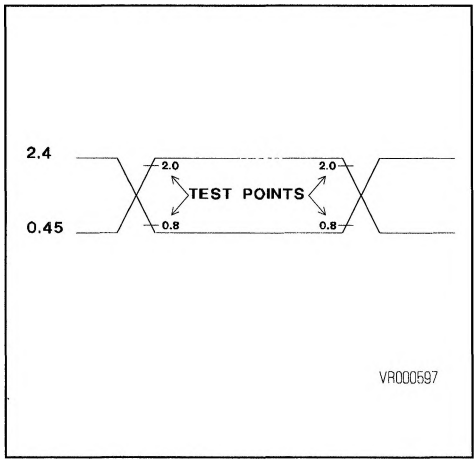


Figure 4 : AC Testing Load Circuit

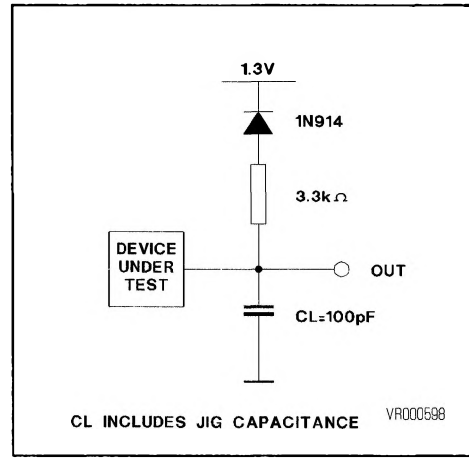
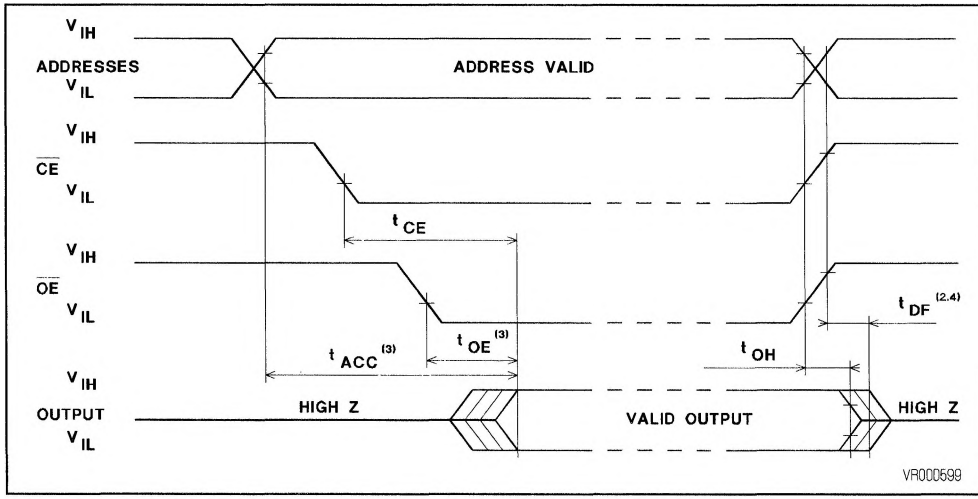


Figure 5 : AC Waveforms



NOTES :
1. Typical values are for TA = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to $t_{\overline{CE}}$ - $t_{\overline{OE}}$ after the falling edge $\overline{CE}$ without impact on $t_{\overline{CE}}$.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

READ MODE

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C2001 has a standby mode which reduces the active current from 35 mA to 0.2 mA. The M27C2001 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current,Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between Vcc and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and GND for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{pp} pin will permanently damage the M27C2001.

When delivered (and after each erasure for UV EPROM), all bits of the M27C2001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C2001 is in the programming mode when Vpp input is at 12.75V, and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. Vcc is specified to be 6.25V ± 0.25V.

PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 24 seconds. Programming with PRESTO II consists of applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C2001s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C2001 may be common. A TTL low level pulse applied to a M27C2001's $\overline{CE}$ input, with PGM low and V_{PP} at 12.75V, will program that M27C2001. A high level $\overline{CE}$ input inhibits the other M27C2001s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, PGM at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C2001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C2001 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C2001, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C2001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C2001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C2001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C2001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C2001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C2001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	1	1	0	0	0	0	1	61

NOTE : A9 = 12V ± 0.5V ; $\overline{CE} = \overline{OE} = V_{IL}$; A1 to A8 = A10 to A17 = V_{IL} ; $V_{PP} = V_{CC} = 5V$

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = 0V to V_{CC}	-10	+10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE}$ = V_{IL}		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

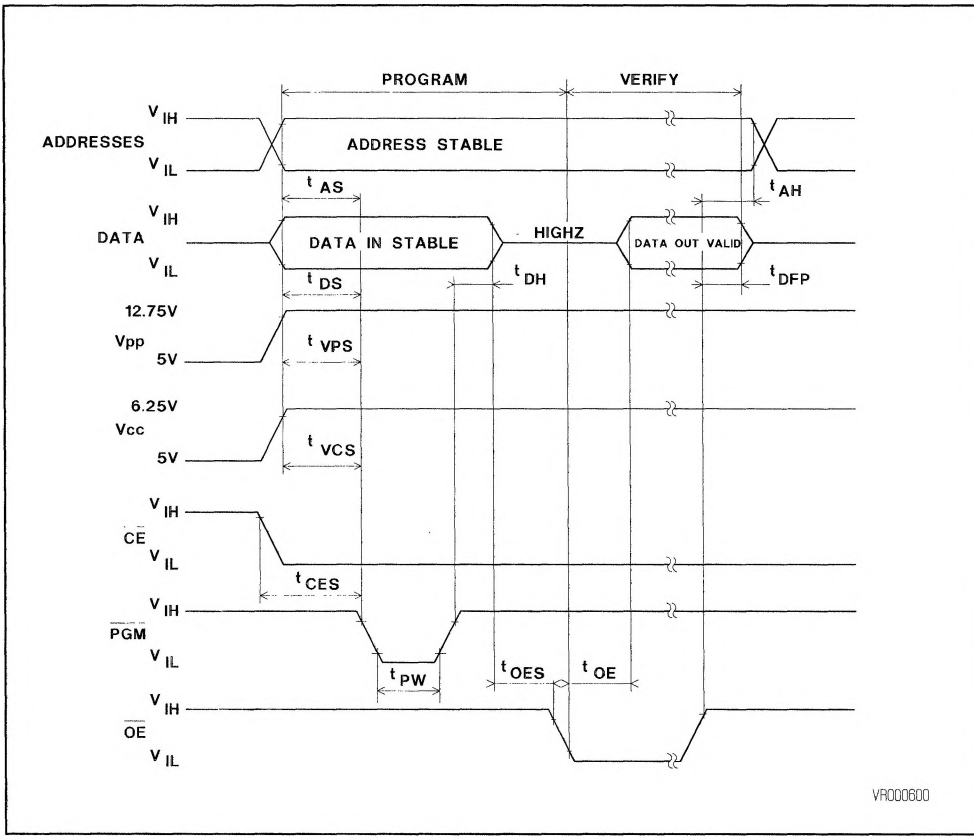
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

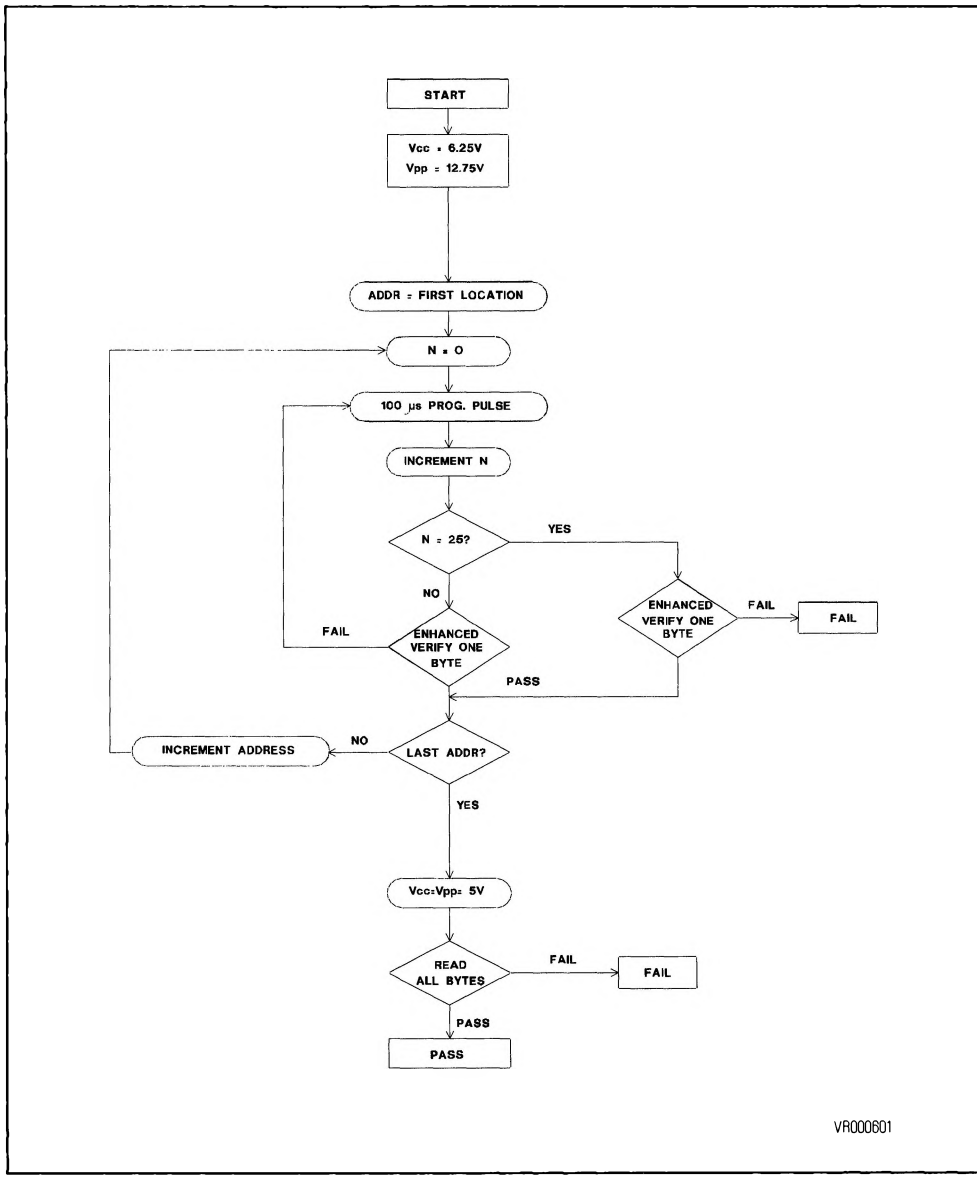
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C2001 a 0.1 µF capacitor is required accross V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart

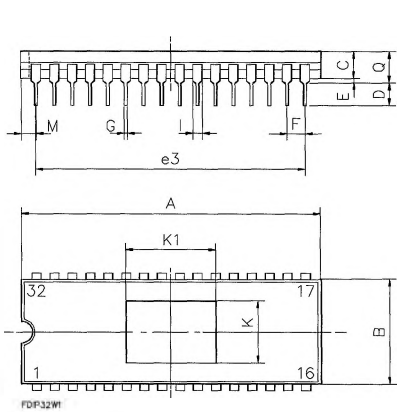


ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp.Range	Package
M27C2001-12XF1	120 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C2001-15XF1	150 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C2001-15F1	150 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C2001-20F1	200 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C2001-25F1	250 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C2001-15XF6	150 ns	5V ± 5 %	-40 to + 85°C	FDIP32-W

PACKAGE MECHANICAL DATA

Figure 8 : 32-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			42.78			1.684
B	14.50		14.90	0.570		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.20		0.070
e3		38.10			1.500	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
K	8.30		8.70	0.327		0.343
K1	12.30		12.70	0.484		0.504