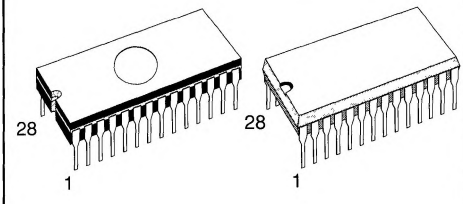
SGS-THOMSON MICROELECTRONICS

M27256

256K (32K x 8) NMOS UV EPROM - OTP ROM

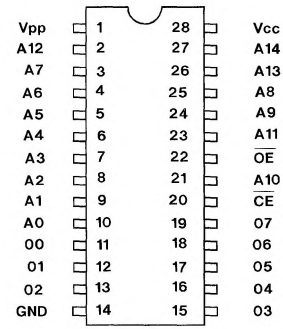
- FAST ACCESS TIME : 170 ns.
- 0 TO + 70°C STANDARD TEMP. RANGE.
- – 40 TO + 85°C EXTENDED TEMP. RANGE.
- SINGLE + 5V POWER SUPPLY.
- ± 10 % V_{CC} TOLERANCE AVAILABLE.
- LOW STANDBY CURRENT (40mA MAX).
- TTL COMPATIBLE DURING READ AND PROGRAM.
- FAST PROGRAMMING ALGORITHM.
- ELECTRONIC SIGNATURE.



FDIP-28 PDIP-28

(Ordering information at the end of the datasheet)

Figure 1 : Pin Configuration



DESCRIPTION

The M27256 is a 262,144-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 32.768 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

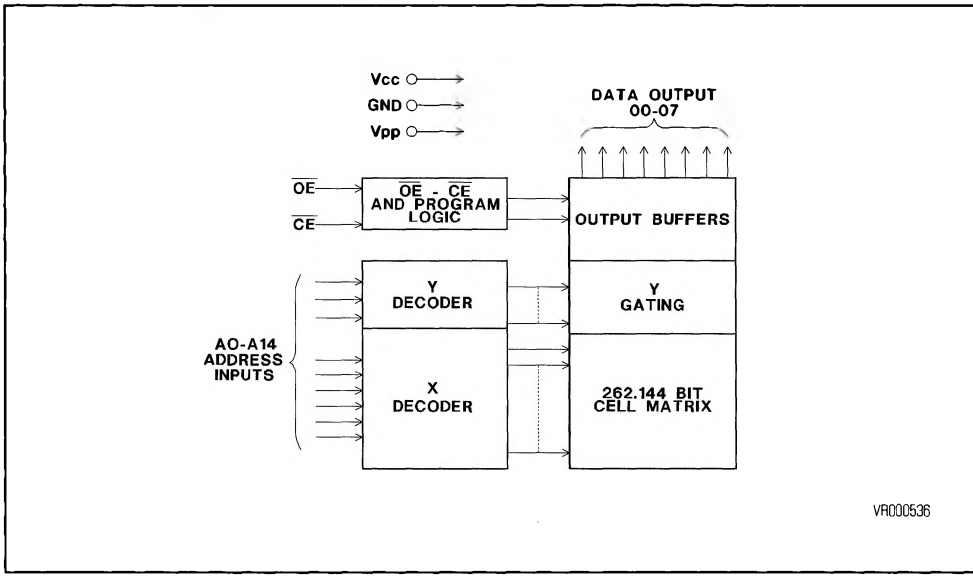
It is housed in a 28 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure

In order to meet production requirements (cost effective solution, this product is also offered in a plastic DIL package).

PIN NAMES

A0-A14	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Values	Unit
V_I	All input or Output voltages with respect to ground	+6.25 to -0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to -0.6	V
T_{AMB}	Ambient temperature under bias /F1 /F6	-10 to +80 -50 to +95	°C °C
T_{STG}	Storage temperature range	-65 to +125	°C
VA9	Voltage on pin 24 with respect to ground	+13.5 to -0.6	V

OPERATING MODES

MODE	PINS						
	$\overline{CE}$	$\overline{OE}$	A9	A0	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
OPTIONAL VERIFY	V_{IL}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{IH}	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL} V_{IL}	V_{IL} V_{IL}	V_H V_H	V_{IL} V_{IH}	V_{CC} V_{CC}	V_{CC} V_{CC}	MAN.CODE DEV.CODE

NOTE : X can be V_{IH} or V_{IL} . V_H = 12V ± 0.5V

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6
Operating Temperature Range	0°C to 70°C	-40°C to 85°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**1F1, 2F1, F1, 3F1, 4F1**	**20F1, 25F1, 30F1, 45F1**
V_{CC} Power Supply (1)	5V ± 5%	5V ± 10%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ (3)	Max.	
I_{LI}	Input Leakage Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V			10	µA
I_{PP1} (2)	V_{PP} Current Read	V_{PP} = 5.5V			5	mA
I_{CC1} (2)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		20	40	mA
I_{CC2} (2)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL} ; V_{PP} = V_{CC}		45	100	mA
V_{IL}	Input low voltage		-0.1		+0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+ 1	V
V_{OL}	Output Low voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = -400 µA	2.4			V
V_{PP} (2)	V_{PP} Read Voltage	V_{CC} = 5V ± 0.25V	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} ± 5%	27256-1		27256-2		27256		27256-3		27256-4		Unit
		V_{CC} ± 10%			27256-20		27256-25		27256-30		27256-45		
		Test Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		170		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output delay	$\overline{OE}$=V_{IL}		170		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		70		75		100		120		150	ns
t_{DF} (4)	$\overline{OE}$ High to Output float	$\overline{CE}$=V_{IL}		35	0	55	0	60	0	105	0	130	ns
t_{OH}	Output hold from address $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		0		ns

CAPACITANCE(5) (T_{AMB} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_{AMB} = 25°C and nominal supply voltages.
4. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
5. Timing parameter is only sampled and not 100% tested.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output Waveform

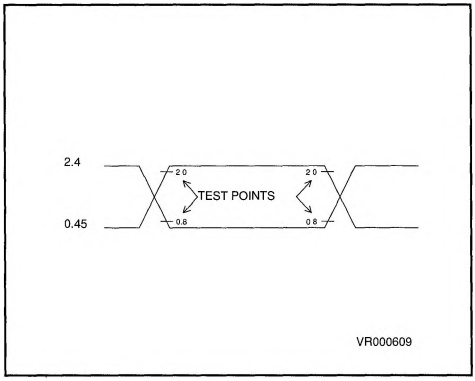


Figure 4 : AC Testing Load Circuit

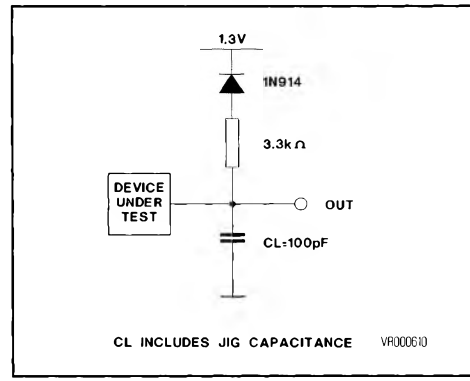
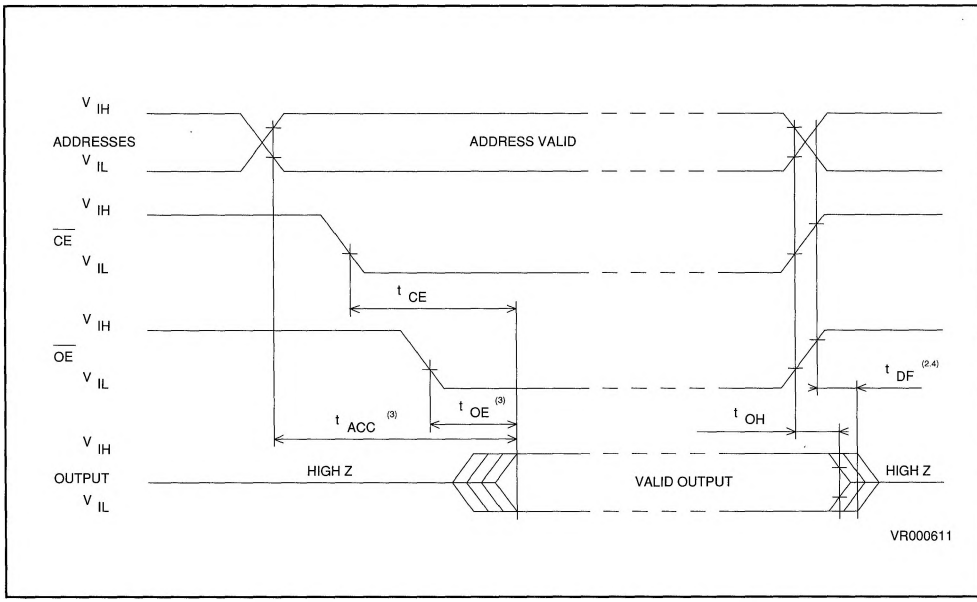


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27256 has a standby mode which reduces the maximum active power current from 100mA to 40mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 13V on pin 1 (V_{PP}) will damage the M27256.

When delivered, (and after each erasure for UV EPROM), all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V.

DEVICE OPERATION (continued)

When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5V.

PROGRAM INHIBIT

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27256. A high level $\overline{CE}$ input inhibits the other M27256s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5V.

OPTIONAL VERIFY

The optional verify may be performed instead of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at 12.5V. The outputs will three-state according to the signal presented to $\overline{OE}$. Therefore, all devices with V_{PP} = 12.5V and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (= 6V) and the normal read mode used to execute a program verify.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27256. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27256, these two identifier bytes are given below.

ERASURE OPERATION

The erasure characteristic of the M27256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27256 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque lables be put over the M27256 window to prevent unintentional erasure. The recommended erasure procedure for the M27256 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27256 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	0	1	0	0	04

PROGRAMMING OPERATION

(T_{AMB} = 25°C ± 5°C, V_{CC}[1] = 6V ± 0.25V, V_{PP}[1] = 12.5V ± 0.3V)

DC AND OPERATING CHARACTERISTICS

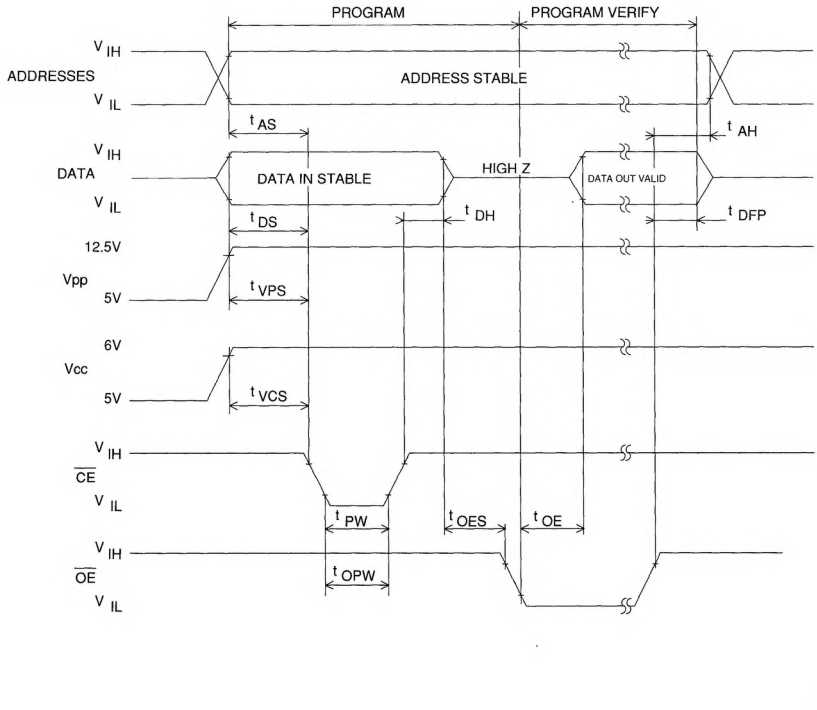
Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = V_{IL} or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE}$ = V_{IL}			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

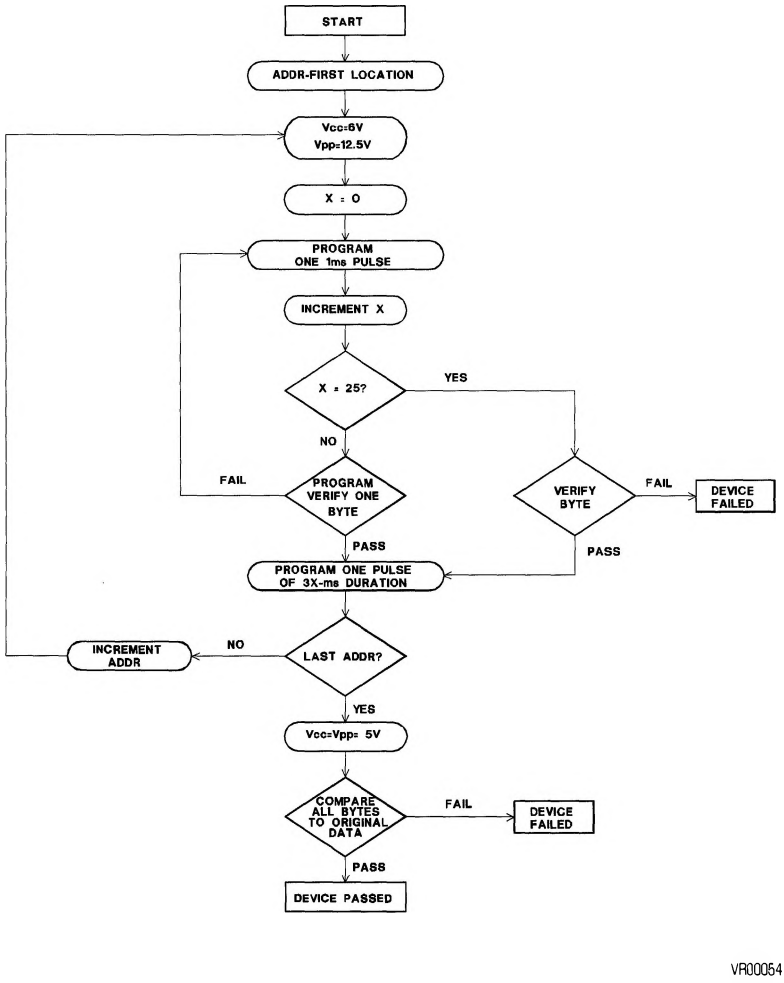
NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1 msec ± 5%.
4. This parameter is only sampled and not 100 % tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27256 a 0.1µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

Figure 7 : Fast Programming Flowchart

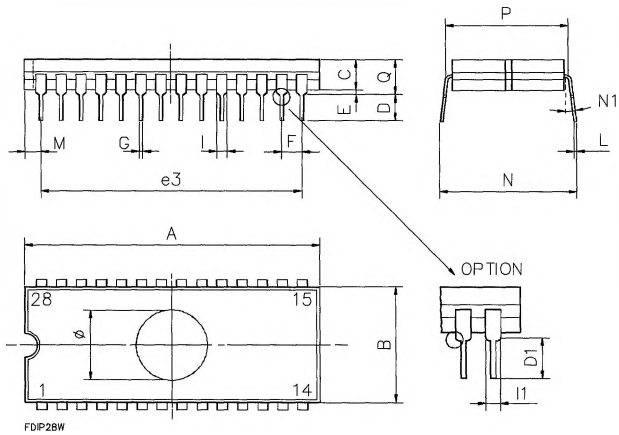


ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27256-1F1	170 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-2F1	200 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256F1	250 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-3F1	300 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-4F1	450 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-20F1	200 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256-25F1	250 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256-30F1	300 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256-45F1	450 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256F6	250 ns	5 V ± 5%	-40 to + 85°C	DIP-28
M27256-4F6	450 ns	5 V ± 5%	-40 to + 85°C	DIP-28

PACKAGE MECHANICAL DATA

Figure 8 : 28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			Inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.199
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.027
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

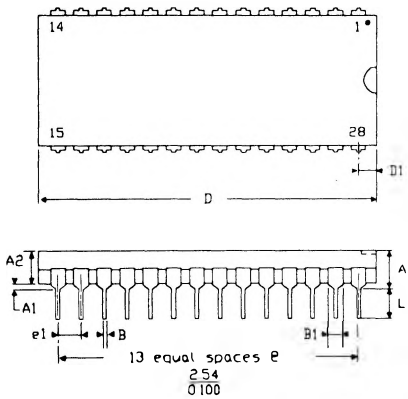
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST27256-20CP	200 ns	5 V ± 10%	0 to +70°C	DIP28
ST27256-25CP	250 ns	5 V ± 10%	0 to +70°C	DIP28

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA

Figure 9 : 28-PIN PLASTIC DIP



VR000287

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			0.025	
B		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						