

# Single and Dual Precision, 17 MHz, Low Noise, CMOS Input Amplifiers

Check for Samples: LMP7711

### **FEATURES**

- Unless otherwise noted, typical values at  $V_S$  = 5V.
- Input offset voltage ±150 µV (max)
- Input bias current 100 fA
- Input voltage noise 5.8 nV/VHz
- Gain bandwidth product 17 MHz
- Supply current (LMP7711) 1.15 mA
- Supply current (LMP7712) 1.30 mA
- Supply voltage range 1.8V to 5.5V

- THD+N @ f = 1 kHz 0.001%
- Operating temperature range -40°C to 125°C
- Rail-to-rail output swing ٠
- Space saving TSOT23 package (LMP7711)
- 10-pin MSOP package (LMP7712) •

### **APPLICATIONS**

- Active filters and buffers •
- Sensor interface applications
- Transimpedance amplifiers

## DESCRIPTION

The LMP7711/LMP7712 are single and dual low noise, low offset, CMOS input, rail-to-rail output precision amplifiers with a high gain bandwidth product and an enable pin. The LMP7711/LMP7712 are part of the LMP™ precision amplifier family and are ideal for a variety of instrumentation applications.

Utilizing a CMOS input stage, the LMP7711/LMP7712 achieve an input bias current of 100 fA, an input referred voltage noise of 5.8 nV/ $\sqrt{Hz}$ , and an input offset voltage of less than ±150  $\mu$ V. These features make the LMP7711/LMP7712 superior choices for precision applications.

Consuming only 1.15 mA of supply current, the LMP7711 offers a high gain bandwidth product of 17 MHz, enabling accurate amplification at high closed loop gains.

The LMP7711/LMP7712 have a supply voltage range of 1.8V to 5.5V, which makes these ideal choices for portable low power applications with low supply voltage requirements. In order to reduce the already low power consumption the LMP7711/LMP7712 have an enable function. Once in shutdown, the LMP7711/LMP7712 draw only 140 nA of supply current.

The LMP7711/LMP7712 are built with National's advanced VIP50 process technology. The LMP7711 is offered in a 6-pin TSOT23 package and the LMP7712 is offered in a 10-pin MSOP.

### **Typical Performance**

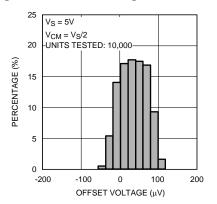


Figure 1. Offset Voltage Distribution

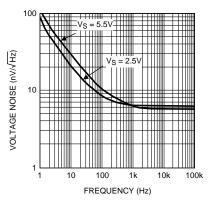
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings (1)

ESD Tolerance <sup>(2)</sup>	
Human Body Model	2000V
Machine Model	200V
Charge-Device Model	1000V
V <sub>IN</sub> Differential	±0.3V
Supply Voltage ( $V_S = V^+ - V^-$ )	6.0V
Voltage on Input/Output Pins	V <sup>+</sup> +0.3V, V <sup>-</sup> -0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature <sup>(3)</sup>	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(3) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

### **Operating Ratings** <sup>(1)</sup>

Supply Voltage $(V_S = V^+ - V^-)$ $0^\circ C \le T_A \le 125^\circ C$ $-40^\circ C \le T_A \le 125^\circ C$ $2.0V$ toPackage Thermal Resistance $(\theta_{JA}^{(2)})$ 6-Pin TSOT23170		
$0^{\circ}C \le T_A \le 125^{\circ}C$ 1.8V to $-40^{\circ}C \le T_A \le 125^{\circ}C$ 2.0V toPackage Thermal Resistance ( $\theta_{JA}^{(2)}$ )706-Pin TSOT23170	Temperature Range <sup>(2)</sup>	−40°C to 125°C
$-40^{\circ}C \le T_A \le 125^{\circ}C$ 2.0V toPackage Thermal Resistance ( $\theta_{JA}^{(2)}$ )1706-Pin TSOT23170	Supply Voltage ( $V_S = V^+ - V^-$ )	
Package Thermal Resistance (θ <sub>JA</sub> <sup>(2)</sup> )   6-Pin TSOT23   170	$0^{\circ}C \le T_{A} \le 125^{\circ}C$	1.8V to 5.5V
6-Pin TSOT23 170	$-40^{\circ}C \le T_{A} \le 125^{\circ}C$	2.0V to 5.5V
	Package Thermal Resistance ( $\theta_{JA}^{(2)}$ )	
10-Pin MSQP 236	6-Pin TSOT23	170°C/W
	10-Pin MSOP	236°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

(2) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.



### **2.5V Electrical Characteristics**

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^{\circ}C$ ,  $V^+ = 2.5V$ ,  $V^- = 0V$ ,  $V_O = V_{CM} = V^+/2$ ,  $V_{EN} = V^+$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Co	Min (1)	Тур (2)	Max (1)	Units	
V <sub>OS</sub>	Input Offset Voltage				±20	±180 <b>±480</b>	μV
TC V <sub>OS</sub>	Input Offset Voltage Temperature Drift (3) (4)	LMP7711 LMP7712		-1.75	-1	±4	µV/°C
I <sub>B</sub>	Input Bias Current	V <sub>CM</sub> = 1.0V	-40°C ≤ TA ≤ 85°C		0.05	1 <b>25</b>	- 0
			-40°C ≤ TA ≤ 125°C		0.05	1 <b>100</b>	рА
I <sub>OS</sub>	Input Offset Current	$V_{CM} = 1.0V$			0.006	0.5 <b>50</b>	pА
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 1.4V$		83 <b>80</b>	100		dB
PSRR	Power Supply Rejection Ratio	$\begin{array}{l} 2.0 V \leq V^+ \leq 5.5 V \\ V^- = 0 V, \ V_{CM} = 0 \end{array}$		85 <b>80</b>	100		dB
		$\begin{array}{l} 1.8 \text{V} \leq \text{V}^+ \leq 5.5 \text{V} \\ \text{V}^- = 0 \text{V}, \ \text{V}_{\text{CM}} = 0 \end{array}$		85	98		uв
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB		-0.3 <b>-0.3</b>		1.5 <b>1.5</b>	V
A <sub>VOL</sub>	Open Loop Voltage Gain	LMP7711, V <sub>O</sub> = 0. R <sub>L</sub> = 2 kΩ to V <sup>+</sup> /2	15 to 2.2V	88 <b>82</b>	98		dB
		LMP7712, V <sub>O</sub> = 0. R <sub>L</sub> = 2 kΩ to V <sup>+</sup> /2	15 to 2.2V	84 <b>80</b>	92		
		LMP7711, V <sub>O</sub> = 0. R <sub>L</sub> = 10 kΩ to V <sup>+</sup> /2	15 to 2.2V 2	92 <b>88</b>	110		
		LMP7712, V <sub>O</sub> = 0. R <sub>L</sub> = 10 kΩ to V <sup>+</sup> /2	15 to 2.2V 2	90 <b>86</b>	95		
V <sub>OUT</sub>	Output Voltage Swing High	$R_L = 2 k\Omega$ to V <sup>+</sup> /2			25	70 <b>77</b>	
		$R_L = 10 \text{ k}\Omega \text{ to } V^+/2$	2		20	60 <b>66</b>	mV from either rai
	Output Voltage Swing Low	$R_L = 2 k\Omega$ to V <sup>+</sup> /2			30	70 <b>73</b>	
		$R_L = 10 \text{ k}\Omega \text{ to } V^+/2$	2		15	60 <b>62</b>	
I <sub>OUT</sub>	Output Current	Sourcing to V <sup>-</sup> V <sub>IN</sub> = 200 mV <sup>(6)</sup>		36 <b>30</b>	52		
		Sinking to V <sup>+</sup> V <sub>IN</sub> = -200 mV <sup>(6)</sup>		7.5 <b>5.0</b>	15		- mA
I <sub>S</sub>	Supply Current	LMP7711 Enable Mode V <sub>EN</sub>		0.95	1.30 <b>1.65</b>		
		LMP7712 (per cha Enable Mode V <sub>EN</sub>	annel)		1.10	1.50 <b>1.85</b>	- mA
		Shutdown Mode (µ V <sub>EN</sub> ≤ 0.4	per channel)		0.03	1 <b>4</b>	μA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(3) Offset voltage average drift is determined by dividing the change in V<sub>OS</sub> at the temperature extremes by the total temperature change.

(4) This parameter is guaranteed by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

(6) The short circuit test is a momentary open loop test.

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## 2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^{\circ}C$ ,  $V^+ = 2.5V$ ,  $V^- = 0V$ ,  $V_O = V_{CM} = V^+/2$ ,  $V_{EN} = V^+$ . Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Тур (2)	Max (1)	Units
SR	Slew Rate	$A_V = +1$ , Rising (10% to 90%)		8.3		
		A <sub>V</sub> = +1, Falling (90% to 10%)		10.3		V/µs
GBW	Gain Bandwidth			14		MHz
e <sub>n</sub>	Input Referred Voltage Noise Density	f = 400 Hz		6.8		nV/√Hz
		f = 1 kHz		5.8		NV/√HZ
i <sub>n</sub>	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz
t <sub>on</sub>	Turn-on Time			140		ns
t <sub>off</sub>	Turn-off Time			1000		ns
V <sub>EN</sub>	Enable Pin Voltage Range	Enable Mode	2.1	2 - 2.5		
		Shutdown Mode		0 - 0.5	0.4	V
I <sub>EN</sub>	Enable Pin Input Current	$V_{EN} = 2.5 V^{(5)}$		1.5	3.0	
		$V_{EN} = 0V^{(5)}$		0.003	0.1	μA
THD+N	Total Harmonic Distortion + Noise	$f = 1 \text{ kHz}, A_V = 1, R_L = 100 \text{ k}\Omega$ V <sub>O</sub> = 0.9 V <sub>PP</sub>		0.003		0/
		$f = 1 \text{ kHz}, A_V = 1, R_L = 600Ω$ V <sub>O</sub> = 0.9 V <sub>PP</sub>		0.004		- %



### **5V Electrical Characteristics**

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^{\circ}C$ ,  $V^+ = 5V$ ,  $V^- = 0V$ ,  $V_{CM} = V^+/2$ ,  $V_{EN} = V^+$ . Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Тур (2)	Max (1)	Units
V <sub>OS</sub>	Input Offset Voltage			±10	±150 <b>±450</b>	μV	
TC V <sub>OS</sub>	Input Offset Voltage Temperataure Drift	LMP7711		-1.75	-1	±4	µV/°C
	(3) (4)	LMP7712			-1	±4	μν/ Ο
IB	Input Bias Current	$V_{CM} = 2.0V$	-40°C ≤ TA ≤ 85°C		0.1	1 <b>25</b>	- pA
			-40°C ≤ TA ≤ 125°C		0.1	1 <b>100</b>	μA
I <sub>OS</sub>	Input Offset Current	$V_{CM} = 2.0V$			0.01	0.5 <b>50</b>	pА
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 3.7V$		85 <b>82</b>	100		dB
PSRR	Power Supply Rejection Ratio	$2.0V \le V^+ \le 5.5V$ $V^- = 0V, V_{CM} = 0$		85 <b>80</b>	100		15
		$1.8V \le V^+ \le 5.5V$ $V^- = 0V, V_{CM} = 0$		85	98		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	-0.3 - <b>0.3</b>		4 <b>4</b>	V	
A <sub>VOL</sub>	Open Loop Voltage Gain	LMP7711, V <sub>O</sub> = 0 R <sub>L</sub> = 2 kΩ to V <sup>+</sup> /2	88 <b>82</b>	107			
		LMP7712, $V_0 = 0$ R <sub>L</sub> = 2 kΩ to V <sup>+</sup> /2	0.3 to 4.7V 2	84 <b>80</b>	90		
		LMP7711, $V_0 = 0$ $R_L = 10 \text{ k}\Omega \text{ to V}^+$	0.3 to 4.7V /2	92 88	110		dB
		LMP7712, $V_0 = 0$ $R_L = 10 \text{ k}\Omega \text{ to V}^+$		90 <b>86</b>	95		
V <sub>OUT</sub>	Output Voltage Swing High	$R_L = 2 k\Omega \text{ to } V^+/2$	2		32	70 <b>77</b>	
		$R_L = 10 \text{ k}\Omega \text{ to V}^+$		22	60 <b>66</b>	mV from either rail	
	Output Voltage Swing Low	$R_{L} = 2 k\Omega \text{ to } V^{+/2}$ (LMP7711)	2		42	70 <b>73</b>	
		$R_{L} = 2 k\Omega \text{ to } V^{+/2}$ (LMP7712)		50	75 <b>78</b>		
		$R_L = 10 \text{ k}\Omega \text{ to V}^+$		20	60 <b>62</b>		
I <sub>OUT</sub>	Output Current	Sourcing to V <sup>-</sup> V <sub>IN</sub> = 200 mV $^{(6)}$		46 <b>38</b>	66		
		Sinking to V <sup>+</sup> V <sub>IN</sub> = -200 mV <sup>(6</sup>		10.5 <b>6.5</b>	23		mA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Offset voltage average drift is determined by dividing the change in V<sub>OS</sub> at the temperature extremes by the total temperature change. This parameter is guaranteed by design and/or characterization and is not tested in production. (3)

(4)

(5) Positive current corresponds to current flowing into the device.

The short circuit test is a momentary open loop test. (6)

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## 5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^{\circ}C$ ,  $V^+ = 5V$ ,  $V^- = 0V$ ,  $V_{CM} = V^+/2$ ,  $V_{EN} = V^+$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Тур (2)	Max (1)	Units		
I <sub>S</sub>	Supply Current	LMP7711 Enable Mode V <sub>EN</sub> ≥ 4.6		1.15	1.40 <b>1.75</b>	<b>m</b> 4		
		LMP7712 (per channel) Enable Mode $V_{EN} \ge 4.6$		1.30	1.70 <b>2.05</b>	– mA		
		Shutdown Mode V <sub>EN</sub> ≤ 0.4 (per channel)		0.14	1 <b>4</b>	μA		
SR	Slew Rate	$A_V = +1$ , Rising (10% to 90%)	6.0	9.5				
		$A_V = +1$ , Falling (90% to 10%)	7.5	11.5		V/µs		
GBW	Gain Bandwidth			17		MHz		
e <sub>n</sub>	Input Referred Voltage Noise Density	f = 400 Hz		7.0	n)/			
		f = 1 kHz		5.8		nV/√Hz		
i <sub>n</sub>	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz		
t <sub>on</sub>	Turn-on Time			110		ns		
t <sub>off</sub>	Turn-off Time			800		ns		
V <sub>EN</sub>	Enable Pin Voltage Range	Enable Mode	4.6	4.5 – 5		v		
		Shutdown Mode		0 - 0.5	0.4	v		
I <sub>EN</sub>	Enable Pin Input Current	V <sub>EN</sub> = 5V <sup>(5)</sup>		5.6	10			
		$V_{EN} = 0V^{(5)}$		0.005	0.2	μA		
THD+N	Total Harmonic Distortion + Noise	$      f = 1 \text{ kHz},  \text{A}_{\text{V}} = 1,  \text{R}_{\text{L}} = 100  \text{k} \Omega                                   $		0.001		97		
		$      f = 1 \text{ kHz},  \text{A}_{\text{V}} = 1,  \text{R}_{\text{L}} = 600 \Omega \\ \text{V}_{\text{O}} = 4  \text{V}_{\text{PP}} $		0.004		%		

## **Connection Diagram**



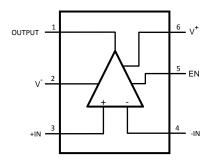
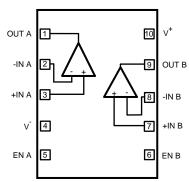
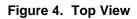


Figure 3. Top View







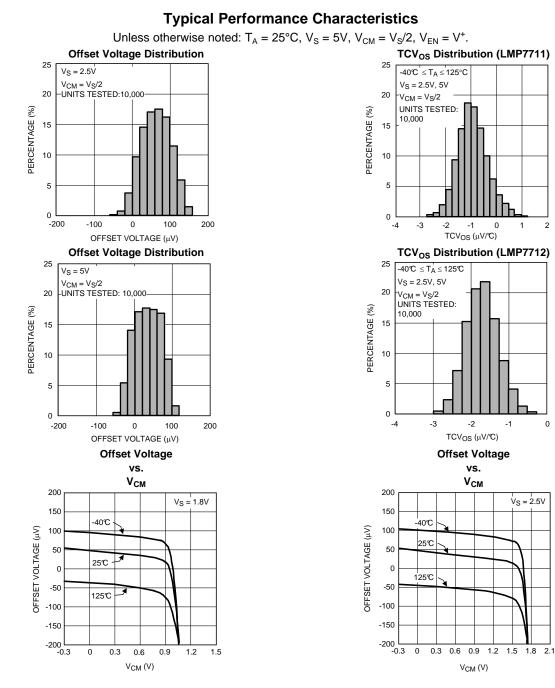


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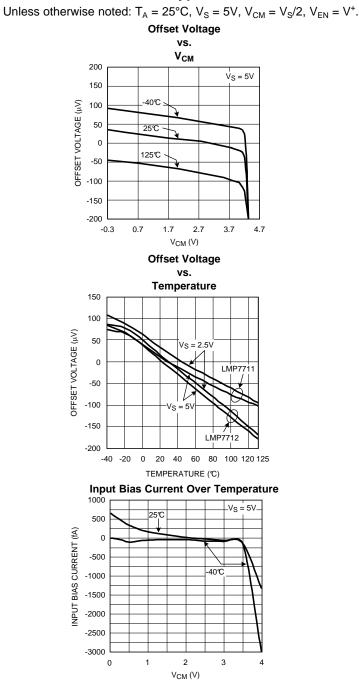
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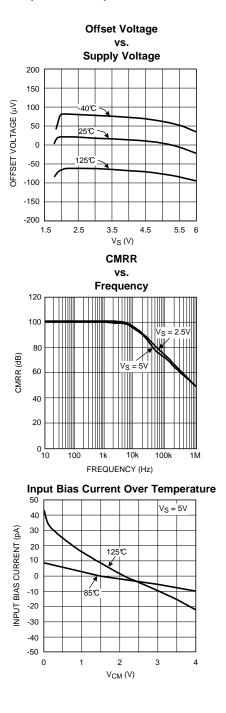


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### **Typical Performance Characteristics (continued)**



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Unless otherwise noted:  $T_A = 25^{\circ}C$ ,  $V_S = 5V$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ . Supply Current Supply Current vs. vs. Supply Voltage (LMP7711) Supply Voltage (LMP7712) 2 2 . 125℃ 1.6 1.6 ŧ SUPPLY CURRENT (mA) SUPPLY CURRENT (mA) 125℃ . 25℃ 25℃ 1.2 1.2 f -40℃ 0.8 0.8 4o℃ 0.4 0.4 0 0 2.5 3.5 4.5 5.5 2.5 3.5 4.5 5.5 1.5 1.5 V<sub>S</sub> (V) V<sub>S</sub>(V) **Supply Current** vs. Supply Voltage (Shutdown) Crosstalk Rejection Ratio (LMP7712) 160 1.8 CROSSTALK REJECTION RATIO (dB) 1.6 140 125℃ 1.4 SUPPLY CURRENT (µA) 120 1.2 100 1 80 0.8 60 0.6 25℃ 40 0.4 0.2 20 -40° 0 0 100k 1M 2.5 3.5 1k 10k 10M 100M 1.5 4.5 5.5  $V_{S}(V)$ FREQUENCY (Hz) **Supply Current Supply Current** vs. vs. Enable Pin Voltage (LMP7711) Enable Pin Voltage (LMP7711) 2.4 1.5 V<sub>S</sub> = 5V  $V_{S} = 2.5V$ 125℃ 125°C 1.3 1.9 SUPPLY CURRENT (mA) SUPPLY CURRENT (mA) 1.1 25℃ 25℃ 0.9 1.4 -40℃ 0.7 -40℃ 0.9 0.5 -40℃ 0.3 0.4 125°C 0.1 -0.1 C -0.1 0 0.5 1 1.5 2 2.5 1 2 3 4

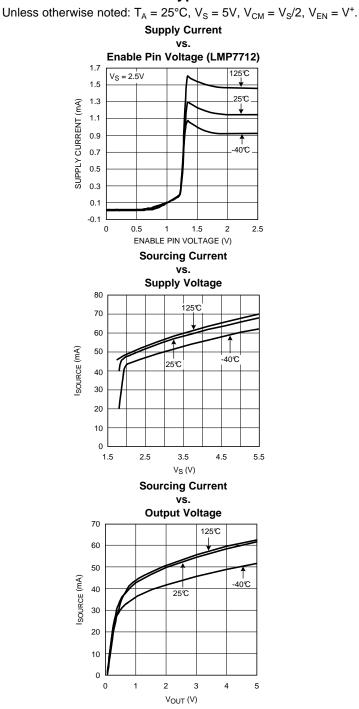
## **Typical Performance Characteristics (continued)**

ENABLE PIN VOLTAGE (V)

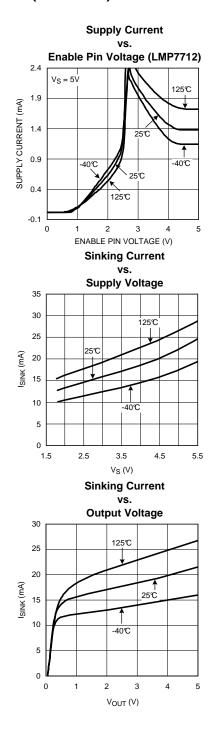
ENABLE PIN VOLTAGE (V)

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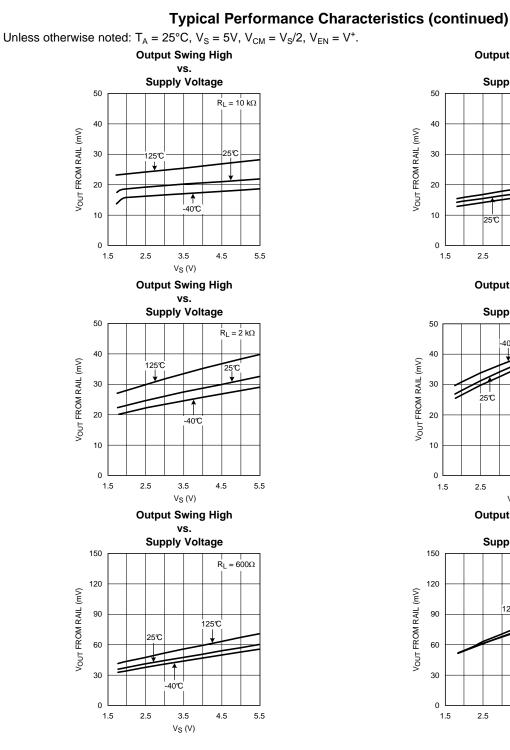


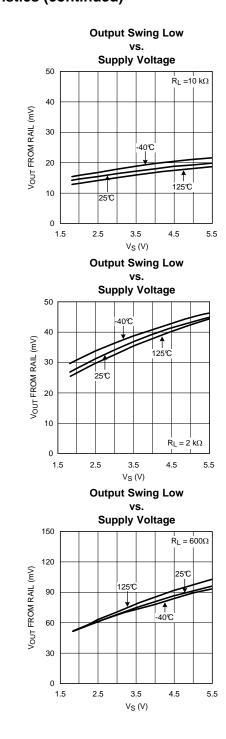
### Typical Performance Characteristics (continued)



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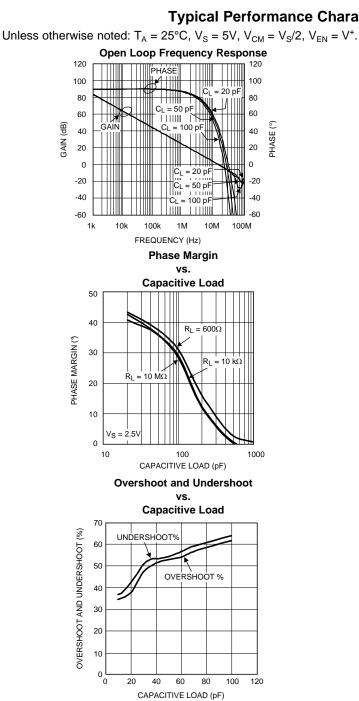
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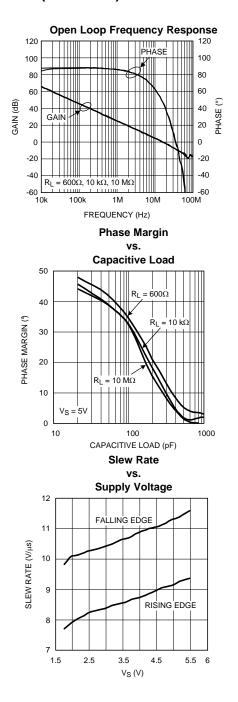






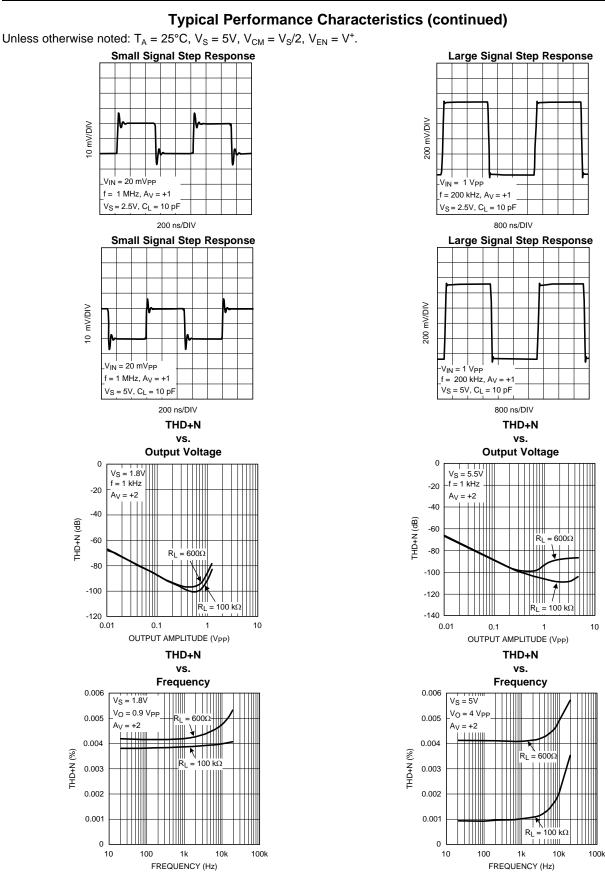




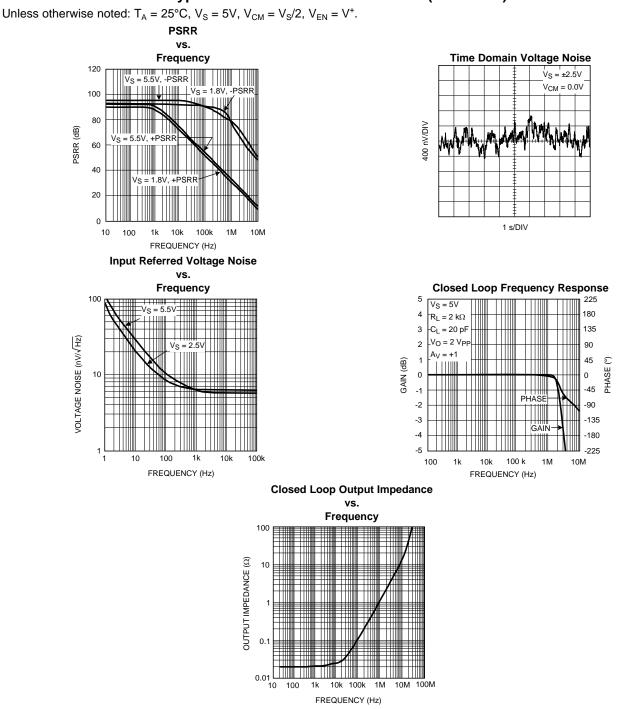


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## **Typical Performance Characteristics (continued)**

### **Application Notes**

### LMP7711/LMP7712

The LMP7711/LMP7712 are single and dual, low noise, low offset, rail-to-rail output precision amplifiers with a wide gain bandwidth product of 17 MHz and low supply current. The wide bandwidth makes the LMP7711/LMP7712 ideal choices for wide-band amplification in portable applications. The low supply current along with the enable feature that is built-in on the LMP7711/LMP7712 allows for even more power efficient designs by turning the device off when not in use.

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## LMP7711

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The LMP7711/LMP7712 are superior for sensor applications. The very low input referred voltage noise of only 5.8 nV/ $\sqrt{Hz}$  at 1 kHz and very low input referred current noise of only 10 fA/  $\sqrt{Hz}$  mean more signal fidelity and higher signal-to-noise ratio.

The LMP7711/LMP7712 have a supply voltage range of 1.8V to 5.5V over a wide temperature range of 0°C to 125°C. This is optimal for low voltage commercial applications. For applications where the ambient temperature might be less than 0°C, the LMP7711/LMP7712 are fully operational at supply voltages of 2.0V to 5.5V over the temperature range of -40°C to 125°C.

The outputs of the LMP7711/LMP7712 swing within 25 mV of either rail providing maximum dynamic range in applications requiring low supply voltage. The input common mode range of the LMP7711/LMP7712 extends to 300 mV below ground. This feature enables users to utilize this device in single supply applications.

The use of a very innovative feedback topology has enhanced the current drive capability of the LMP7711/LMP7712, resulting in sourcing currents as much as 47 mA with a supply voltage of only 1.8V.

The LMP7711 is offered in the space saving TSOT23 package and the LMP7712 is offered in a 10-pin MSOP. These small packages are ideal solutions for applications requiring minimum PC board footprint.

National Semiconductor is heavily committed to precision amplifiers and the market segments they serves. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

### CAPACITIVE LOAD

The unity gain follower is the most sensitive configuration to capacitive loading. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will be either underdamped or the amplifier will oscillate.

The LMP7711/LMP7712 can directly drive capacitive loads of up to 120 pF without oscillating. To drive heavier capacitive loads, an isolation resistor,  $R_{ISO}$  in Figure 5, should be used. This resistor and  $C_L$  form a pole and hence delay the phase lag or increase the phase margin of the overall system. The larger the value of  $R_{ISO}$ , the more stable the output voltage will be. However, larger values of  $R_{ISO}$  result in reduced output swing and reduced output current drive.

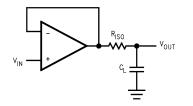


Figure 5. Isolating Capacitive Load

### INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP7711/LMP7712 enhance this performance by having the low input bias current of only 50 fA, as well as, a very low input referred voltage noise of 5.8 nV/ $\sqrt{Hz}$ . In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the LMP7711/LMP7712. Figure 6 shows typical input common mode input capacitance of the LMP7711/LMP7712.



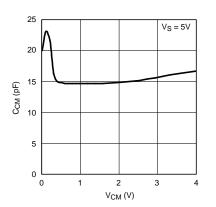


Figure 6. Input Common Mode Capacitance

This input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and under DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and also causes gain peaking. In order to compensate for the input capacitance, care must be taken in choosing feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in Figure 7 is simply  $-R_2/R_1$ .

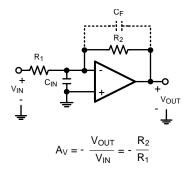


Figure 7. Compensating for Input Capacitance

For the time being, ignore  $C_F$ . The AC gain of the circuit in Figure 7 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0}{R_1}R_1}\right)^{+} \frac{s^2}{\left(\frac{A_0}{C_{IN}R_2}\right)^{-}}\right]}$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}} \left[ \frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4A_0C_{IN}}{R_2}} \right]$$
(2)

As shown in Equation 2, as the values of  $R_1$  and  $R_2$  are increased, the magnitude of the poles are reduced, which in turn decreases the bandwidth of the amplifier. Figure 8 shows the frequency response with different value resistors for  $R_1$  and  $R_2$ . Whenever possible, it is best to chose smaller feedback resistors.

(1)



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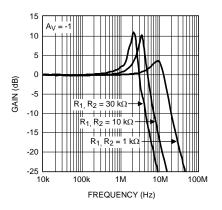


Figure 8. Closed Loop Frequency Response

As mentioned before, adding a capacitor to the feedback path will decrease the peaking. This is because  $C_F$  will form yet another pole in the system and will prevent pairs of poles, or complex conjugates from forming. It is the presence of pairs of poles that cause the peaking of gain. Figure 9 shows the frequency response of the schematic presented in Figure 7 with different values of  $C_F$ . As can be seen, using a small value capacitor significantly reduces or eliminates the peaking.

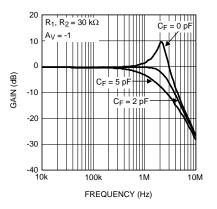


Figure 9. Closed Loop Frequency Response

### TRANSIMPEDANCE AMPLIFIER

In many applications, the signal of interest is a very small amount of current that needs to be detected. Current that is transmitted through a photodiode is a good example. Barcode scanners, light meters, fiber optic receivers, and industrial sensors are some typical applications utilizing photodiodes for current detection. This current needs to be amplified before it can be further processed. This amplification is performed using a current-to-voltage converter configuration or transimpedance amplifier. The signal of interest is fed to the inverting input of an op amp with a feedback resistor in the current path. The voltage at the output of this amplifier will be equal to the negative of the input current times the value of the feedback resistor. Figure 10 shows a transimpedance amplifier configuration.  $C_D$  represents the photodiode parasitic capacitance and  $C_{CM}$  denotes the common-mode capacitance of the amplifier. The presence of all of these capacitances at higher frequencies might lead to less stable topologies at higher frequencies. Care must be taken when designing a transimpedance amplifier to prevent the circuit from oscillating.

With a wide gain bandwidth product, low input bias current and low input voltage and current noise, the LMP7711/LMP7712 are ideal for wideband transimpedance applications.



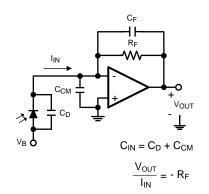


Figure 10. Transimpedance Amplifier

A feedback capacitance  $C_F$  is usually added in parallel with  $R_F$  to maintain circuit stability and to control the frequency response. To achieve a maximally flat, 2<sup>nd</sup> order response,  $R_F$  and  $C_F$  should be chosen by using Equation 3

$$C_{F} = \sqrt{\frac{C_{IN}}{GBWP * 2 \pi R_{F}}}$$
(3)

Calculating C<sub>F</sub> from Equation 3 can sometimes result in capacitor values which are less than 2 pF. This is especially the case for high speed applications. In these instances, its often more practical to use the circuit shown in Figure 11 in order to allow more sensible choices for C<sub>F</sub>. The new feedback capacitor, C'<sub>F</sub>, is (1+  $R_{\rm B}/R_{\rm A}$ ) C<sub>F</sub>. This relationship holds as long as  $R_{\rm A} << R_{\rm F}$ .

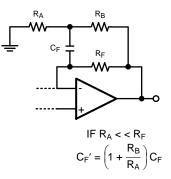


Figure 11. Modified Transimpedance Amplifier

### SENSOR INTERFACE

The LMP7711/LMP7712 have low input bias current and low input referred noise, which make them ideal choices for sensor interfaces such as thermopiles, Infra Red (IR) thermometry, thermocouple amplifiers, and pH electrode buffers.

Thermopiles generate voltage in response to receiving radiation. These voltages are often only a few microvolts. As a result, the operational amplifier used for this application needs to have low offset voltage, low input voltage noise, and low input bias current. Figure 12 shows a thermopile application where the sensor detects radiation from a distance and generates a voltage that is proportional to the intensity of the radiation. The two resistors,  $R_A$  and  $R_B$ , are selected to provide high gain to amplify this signal, while  $C_F$  removes the high frequency noise.



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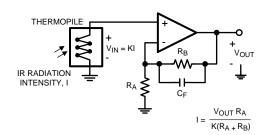


Figure 12. Thermopile Sensor Interface

#### **PRECISION RECTIFIER**

Rectifiers are electrical circuits used for converting AC signals to DC signals. Figure 13 shows a full-wave precision rectifier. Each operational amplifier used in this circuit has a diode on its output. This means for the diodes to conduct, the output of the amplifier needs to be positive with respect to ground. If  $V_{IN}$  is in its positive half cycle then only the output of the bottom amplifier will be positive. As a result, the diode on the output of the bottom amplifier will show at the output of the circuit. If  $V_{IN}$  is in its negative half cycle then the output of the top amplifier will be positive, resulting in the diode on the output of the top amplifier conducting and, delivering the signal on the amplifier's output to the circuits output.

For  $R_2/R_1 \ge 2$ , the resistor values can be found by using the equation shown in Figure 13. If  $R_2/R_1 = 1$ , then  $R_3$  should be left open, no resistor needed, and  $R_4$  should simply be shorted.

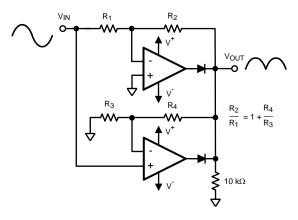


Figure 13. Precision Rectifier



### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	•	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Samples
	(1)		Drawing			(2)		(3)	(Requires Login)
LMP7711MK	ACTIVE	SOT	DDC	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMP7711MK/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMP7711MKE/NOPB	ACTIVE	SOT	DDC	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMP7711MKX	ACTIVE	SOT	DDC	6	3000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMP7711MKX/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMP7712MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMP7712MME/NOPB	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMP7712MMX	ACTIVE	VSSOP	DGS	10	3500	TBD	CU SNPB	Level-1-260C-UNLIM	
LMP7712MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.





19-Nov-2012

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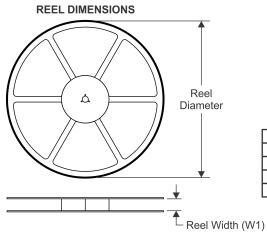
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# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7711MK	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MK/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MKE/NOPB	SOT	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MKX	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MKX/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7712MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7712MME/NOPB	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7712MMX	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7712MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

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# PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7711MK	SOT	DDC	6	1000	203.0	190.0	41.0
LMP7711MK/NOPB	SOT	DDC	6	1000	203.0	190.0	41.0
LMP7711MKE/NOPB	SOT	DDC	6	250	203.0	190.0	41.0
LMP7711MKX	SOT	DDC	6	3000	206.0	191.0	90.0
LMP7711MKX/NOPB	SOT	DDC	6	3000	206.0	191.0	90.0
LMP7712MM/NOPB	VSSOP	DGS	10	1000	203.0	190.0	41.0
LMP7712MME/NOPB	VSSOP	DGS	10	250	203.0	190.0	41.0
LMP7712MMX	VSSOP	DGS	10	3500	349.0	337.0	45.0
LMP7712MMX/NOPB	VSSOP	DGS	10	3500	349.0	337.0	45.0

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187 variation BA.



DDC (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



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