PRELIMINARY PRODUCT SPECIFICATIONS

SHARP

Integrated Circuits Group

LH28F64BNHG-PBSL60

Synchronus Dual Work Flash Memory

64M (4M × 16)

(Model No.: LHF64N08)

Spec No.: FM02X010

Issue Date: October 24, 2002

SHARP

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To;

PRELIMINARY

SPECIFICATIONS

Product Type 64Mbit Flash Memory

LH28F640BNHG—PBSL60

Model No. (LHF64N08)

This device specification is subject to change without notice.

* This specifications contains 38 pages including the cover and appendix.

CUSTOMERS ACCEPTANCE

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

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LH28F640BNHG-PBSL60
64Mbit (4Mbit×16)
Synchronous Dual Work Flash MEMORY

- 64M density with 16Bit I/O Interface
- High Performance Reads
  - 60/20ns 8-Word Page Mode
  - 52MHz Synchronous Burst Mode
- Configurative 4-Plane Dual Work
  - Flexible Partitioning
  - Read operations during Block Erase or (Page Buffer) Program
  - Status Register for Each Partition
- Low Power Operation
  - 1.7V Read and Write Operations
  - V_{CCQ} for Input/Output Power Supply Isolation
  - Automatic Power Savings Mode Reduces I_{CCR} in Static Mode
- Enhanced Code + Data Storage
  - 5µs Typical Erase/Program Suspends
- OTP (One Time Program) Block
  - 4-Word Factory-Programmed Area
  - 4-Word User-Programmable Area
- High Performance Program with Page Buffer
  - 16-Word Page Buffer
  - 5µs/Word (Typ.) at 12V V_{PP}
- Operating Temperature -40°C to +85°C
- Advanced Factory Programming Mode
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- Flexible Blocking Architecture
  - Eight 4K-word Parameter Blocks
  - One-hundred and twenty-seven 32K-word Main Blocks
  - Bottom Parameter Location
- Enhanced Data Protection Features
  - Individual Block Lock and Block Lock-Down with Zero-Latency
  - All blocks are locked at power-up or device reset.
  - Absolute Protection with $V_{PP} \leq V_{PPLK}$
  - Block Erase, Advanced Factory Program, (Page Buffer) Word Program Lockout during Power Transitions
- Automated Erase/Program Algorithms
  - 1.8V Low-Power 22µs/Word (Typ.) Programming
  - 12V No Glue Logic 9µs/Word (Typ.) Production Programming and 0.5s Erase (Typ.)
- Cross-Compatible Command Support
  - Basic Command Set
  - Common Flash Interface (CFI)
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- 0.75mm pitch 56-Ball CSP
- ETOX^{TM*} Flash Technology
- Not designed or rated as radiation hardened
- CMOS Process (P-type silicon substrate)

The product, which is 4-Plane Synchronous Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC}=1.7V-1.95V and V_{PP}=0.9V-1.95V or 11.7V-12.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode and synchronous burst mode. It allows code execution directly from Flash, thus eliminating time consuming wait states. Furthermore, its newly configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as an unique number.

* ETOX is a trademark of Intel Corporation.

0.75mm pitch
56-BALL CSP
PINOUT
11mm x 8mm
TOP VIEW

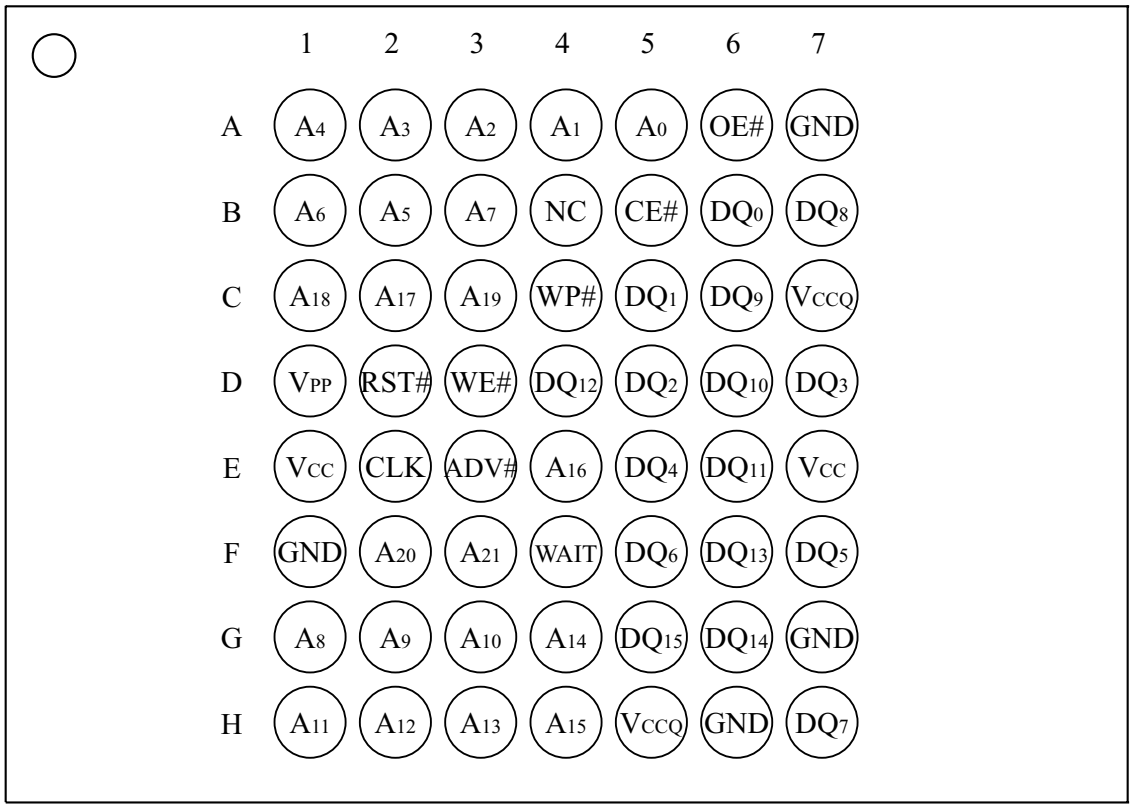


Figure 1. 0.75mm pitch 56-Ball CSP Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{21}	INPUT	ADDRESS INPUTS: Inputs for addresses. 64M: A_0-A_{21}
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code and read/partition configuration register code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
CLK	INPUT	CLOCK: Synchronizes the memory to the system bus operating frequency in synchronous burst mode. The first rising (or falling if RCR.6 is "0") edge latches the address when ADV# is V_{IL} or upon a rising ADV# edge. This is used only for synchronous burst mode.
ADV#	INPUT	ADDRESS VALID: Addresses are input to the memory when ADV# is low (V_{IL}). Addresses are latched on ADV#'s rising edge during read and write operations.
RST#	INPUT	RESET: When low (V_{IL}), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to asynchronous read array mode. RST# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first).
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and not locked-down. When WP# is V_{IH}, lock-down is disabled.
WAIT	OUTPUT	WAIT: Indicates data valid in synchronous burst modes. The read configuration register bit 10 (RCR.10, WT) determines its polarity. With CE# at V_{IL}, WAIT's active output is V_{OL} or V_{OH}. WAIT is High-Z if CE# is V_{IH}. WAIT is not gated by OE#. WAIT is used only for synchronous burst mode.
V_{PP}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, advanced factory program, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin. Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum. Use of this pin at 12V beyond these limits may reduce block cycling capability or cause permanent damage.

Table 1. Pin Descriptions (Continued)

Symbol	Type	Name and Function
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (1.7V-1.95V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V_{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (1.7V-1.95V): Power supply for all input/output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

Table 2. Simultaneous Operation Modes Allowed with Four Planes[1, 2]

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Advanced Factory Program	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Advanced Factory Program			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

NOTES:

1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition. Only one partition can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.
   It is not possible to do burst reads that cross partition boundaries.

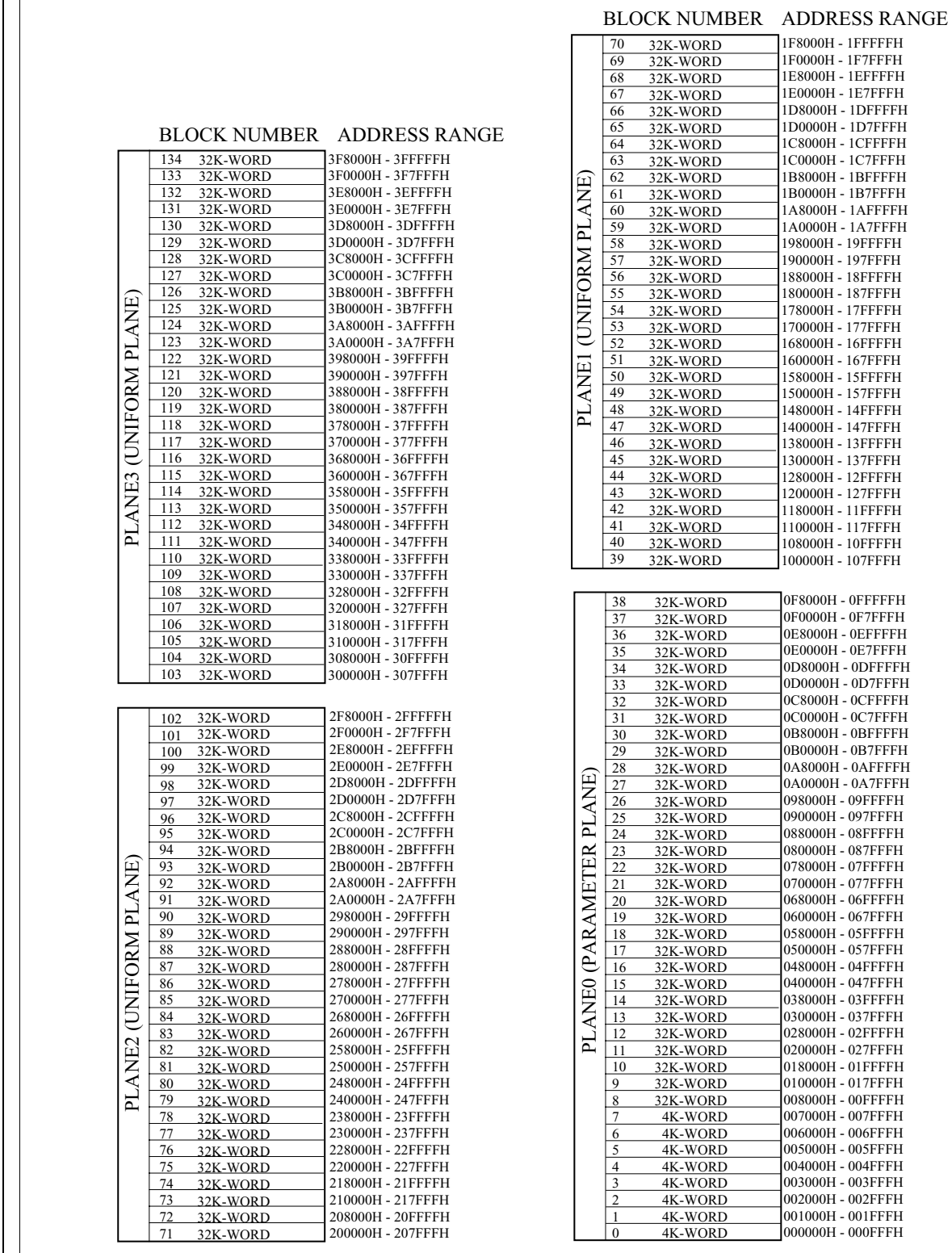


Figure 2. Memory Map (Bottom Parameter)

Table 3. Identifier Codes and OTP Address for Read Operation

	Code	Address [A_{15}-A_0]	Data [DQ_{15}-DQ_0]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	1
Device Code	Bottom Parameter Device Code	0001H	00BBH	1, 2
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ_0 = 0	3
	Block is Locked		DQ_0 = 1	3
	Block is not Locked-Down		DQ_1 = 0	3
	Block is Locked-Down		DQ_1 = 1	3
Device Configuration Code	Read Configuration Register	0005H	RCRC	1, 4
	Partition Configuration Register	0006H	PCRC	1, 5
OTP	OTP Lock	0080H	OTP-LK	1, 6
	OTP	0081-0088H	OTP	1, 7

NOTES:
1. The address A_{21}-A_{16} are shown in below table for reading the manufacturer code, device code, device configuration code and OTP data.
2. Bottom parameter device has its parameter blocks in the plane0 (The lowest address).
3. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes/OTP command (90H) has been written.
   DQ_{15}-DQ_2 are reserved for future implementation.
4. RCRC=Read Configuration Register Code.
5. PCRC=Partition Configuration Register Code.
6. OTP-LK=OTP Block Lock configuration.
7. OTP=OTP Block data.

Table 4. Identifier Codes and OTP Address for Read Operation on Partition Configuration(1) (64M-bit device)

Partition Configuration Register (2)			Address (64M-bit device)
PCR.10	PCR.9	PCR.8	[A_{21}-A_{16}]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

NOTES:
1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
2. Refer to Table 15 for the partition configuration register.

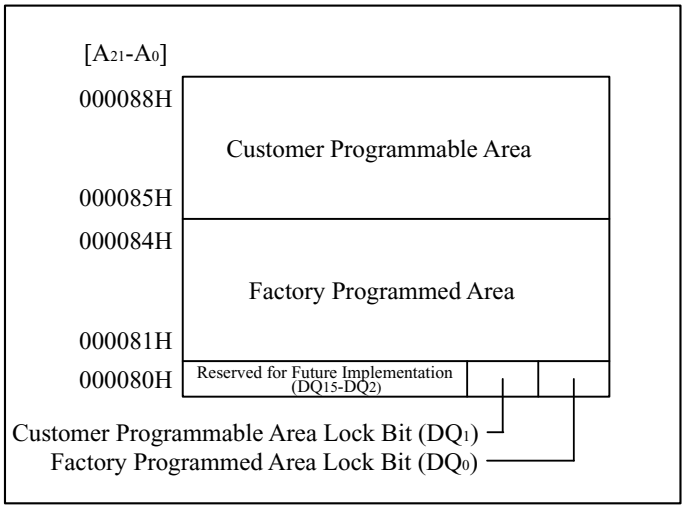


Figure 3. OTP Block Address Map for OTP Program
(The area outside 80H~88H cannot be used.)

Table 5. Bus Operation[1, 2]

Mode	Notes	RST#	CE#	OE#	WE#	ADV#	WP#	Address	V_{PP}	DQ_{0-15}	WAIT
Read Arra;y	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{OUT}	See NOTE 8
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High Z	V_{IL} or V_{IH}
Standby		V_{IH}	V_{IH}	X	X	X	X	X	X	High Z	High Z
Reset	3	V_{IL}	X	X	X	X	X	X	X	High Z	High Z
Read Identifier Codes/OTP	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	See Table 3 and Table 4	X	See Table 3 and Table 4	V_{IL} or V_{IH}
Read Query	6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	See Appendix	X	See Appendix	V_{IL} or V_{IH}
Write	4,5,6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	X	X	X	D_{IN}	V_{IL} or V_{IH}

NOTES:
1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, (page buffer) program or OTP program are reliably executed when $V_{PP}=V_{PPH1/2}$ and V_{CC}=1.7V-1.95V.
   Command writes involving advanced factory program are reliably executed when $V_{PP}=V_{PPH2}$ and V_{CC}=1.7V-1.95V.
5. Refer to Table 6 for valid D_{IN} during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Appendix of LH28F640BN series for more information about query code.
8. WAIT indicates data valid in synchronous burst modes. WAIT is used only for synchronous burst mode.

Table 6. Command Definitions(11)

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data	Oper(1)	Addr(2)	Data(3)
Read Array	1		Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Advanced Factory Program	2	5,9	Write	X	30H	Write	X	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8,9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
OTP Program	2	9	Write	OA	C0H	Write	OA	OD
Set Read Configuration Register	2		Write	RCRC	60H	Write	RCRC	03H
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

NOTES:

1. Bus operations are defined in Table 5.
2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
   X=Any valid address within the device.
   PA=Address within the selected partition.
   IA=Identifier codes address (See Table 3 and Table 4).
   QA=Query codes address. Refer to Appendix of LH28F640BN series for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See Figure 3).
   RCRC=Read configuration register code presented on the addresses A_0-A_{15}.
   PCRC=Partition configuration register code presented on the address A_0-A_{15}.
3. ID=Data read from identifier codes. (See Table 3 and Table 4).
   QD=Data read from query database. Refer to Appendix of LH28F640BN series for details.
   SRD=Data read from status register. See Table 10 and Table 11 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
   OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, read configuration register code, partition configuration register code and the data within OTP block (See Table 3 and Table 4).
   The Read Query command is available for reading CFI (Common Flash Interface) information.

5. Block erase, advanced factory program or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to Appendix of LH28F640BN series for details.
8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Advanced factory program and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is V_{IL}. When WP# is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 7. Functions of Block Lock[5] and Block Lock-Down

Current State					Erase/Program Allowed [2]
State	WP#	DQ_1[1]	DQ_0[1]	State Name	
[000]	0	0	0	Unlocked	Yes
[001][3]	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101][3]	1	0	1	Locked	No
[110][4]	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

NOTES:
1. DQ_0=1: a block is locked; DQ_0=0: a block is unlocked.
   DQ_1=1: a block is locked-down; DQ_1=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, advanced factory program and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation.
4. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function which is different from those described above.

Table 8. Block Locking State Transitions upon Command Write[4]

Current State				Result after Lock Command Written (Next State)		
State	WP#	DQ_1	DQ_0	Set Lock[1]	Clear Lock[1]	Set Lock-down[1]
[000]	0	0	0	[001]	No Change	[011][2]
[001]	0	0	1	No Change[3]	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111][2]
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111][2]
[111]	1	1	1	No Change	[110]	No Change

NOTES:
1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that WP# is not changed and fixed V_{IL} or V_{IH}.

Table 9. Block Locking State Transitions upon WP# Transition(4)

Previous State	Current State				Result after WP# Transition (Next State)	
	State	WP#	DQ_1	DQ_0	WP#=0→1(1)	WP#=1→0(1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110](2)	[011]	0	1	1	[110]	-
Other than [110](2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011](3)
-	[111]	1	1	1	-	[011]

NOTES:
1. "WP#=0→1" means that WP# is driven to V_{IH} and "WP#=1→0" means that WP# is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

Table 10. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BES	PBPAFPOPS	VPPS	PBPSS	DPS	PPES
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE STATUS (BES)
1 = Error in Block Erase
0 = Successful Block Erase

SR.4 = (PAGE BUFFER) PROGRAM, ADVANCED FACTORY PROGRAM AND OTP PROGRAM STATUS (PBPAFPOPS)
1 = Error in (Page Buffer) Program, Advanced Factory Program or OTP Program
0 = Successful (Page Buffer) Program, Advanced Factory Program or OTP Program

SR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} LOW Detect, Operation Abort
0 = V_{PP} OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
1 = (Page Buffer) Program Suspended
0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
1 = Erase or Program Attempted on a Locked Block, Operation Abort
0 = Unlocked

SR.0 = PARTITION PROGRAM AND ERASE STATUS (PPES)
1 = Another Partition is busy.
AFP: Program or Verify busy.
0 = Depending on status of SR.7.
The addressed partition is busy or no partition is busy.
AFP: Program or Verify done, AFP ready.

NOTES:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 to determine block erase, advanced factory program, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase, advanced factory program, (page buffer) program, set/clear block lock bit, set block lock-down bit, set read configuration register, set partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Advanced Factory Program, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1}$, V_{PPH2} or V_{PPLK}.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Advanced Factory Program, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8 are reserved for future use and should be masked out when polling the status register.

If SR.7="0" and SR.0="0", the addressed partition is busy and other partition is not busy. In AFP Mode, it indicates that the device is finished programming or verifying data or is ready for data.

If SR.7="0" and SR.0="1", another partition is busy (the addressed partition is not busy). In AFP Mode, it indicates that the device is programming or verifying data.

If SR.7="1" and SR.0="0", no partition is busy. In AFP Mode, it indicates that the device has exited AFP mode.

SR.7="1" and SR.0="1" will not occur.

Table 11. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)
1 = Page Buffer Program available
0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Table 12. Read Configuration Register Definition

RM	R	FC2	FC1	FC0	WT	DOC	WC
15	14	13	12	11	10	9	8
BS	CC	R	R	BW	BL2	BL1	BL0
7	6	5	4	3	2	1	0

RCR.15 = READ MODE (RM)
- 0 = Synchronous Burst Reads Enabled
- 1 = Asynchronous Reads Enabled (Default)

RCR.14 = RESERVED FOR FUTURE ENHANCEMENTS (R)

RCR.13-11 = FREQUENCY CONFIGURATION (FC2-0)
- 000 = Code 0 reserved for future use
- 001 = Code 1 reserved for future use
- 010 = Code 2
- 011 = Code 3
- 100 = Code 4
- 101 = Code 5
- 110 = Code 6 reserved for future use
- 111 = Code 7 reserved for future use (Default)

RCR.10 = WAIT SIGNAL POLARITY (WT)
- 0 = WAIT signal is active low
- 1 = WAIT signal is active high (Default)

RCR.9 = DATA OUTPUT CONFIGURATION (DOC)
- 0 = Hold Data for One Clock
- 1 = Hold Data for Two Clocks (Default)

RCR.8 = WAIT CONFIGURATION (WC)
- 0 = WAIT Asserted During Delay
- 1 = WAIT Asserted One Data Cycle Before Delay (Default)

RCR.7 = BURST SEQUENCE (BS)
- 0 = Intel Burst Order
- 1 = Linear Burst Order (Default)

RCR.6 = CLOCK CONFIGURATION (CC)
- 0 = Burst Starts and Data Output on Falling Clock Edge
- 1 = Burst Starts and Data Output on Rising Clock Edge (Default)

RCR.5-4 = RESERVED FOR FUTURE ENHANCEMENTS (R)

RCR.3 = BURST WRAP (BW)
- 0 = Wrap Burst Reads within Burst Length set by RCR.2-0
- 1 = No Wrap Burst Reads within Burst Length set by RCR.2-0 (Default).

RCR.2-0 = BURST LENGTH (BL2-0)
- 001 = 4 Word Burst
- 010 = 8 Word Burst
- 011 = Reserved for future use
- 111 = Continuous (Linear) Burst (Default)

NOTES:

Read configuration register affects the read operations from main and parameter blocks. Read operations for status register, query code, identifier codes, OTP block and device configuration codes support single read cycles.

RCR.14, RCR.5 and RCR.4 bits are reserved for future use and should be masked out when checking the read configuration register.

Refer to Frequency Configuration in Table 13 and Figure 4 for information about the frequency configuration RCR.13-11.

Undocumented combinations of bits RCR.13-11 are reserved for future implementations and should not be used.

Data is not ready when WAIT is active.

Refer to Figure 5 for information about Data Output configuration RCR.9.

Refer to Table 14 for information about Burst Wrap configuration RCR.3.

In the asynchronous page mode, the burst length always equals 8 words.

All the bits in the read configuration register are set to "1" after power-up or device reset.

When the bit RCR.15 is set to "1", other bits are invalid.

Table 13. Frequency Configuration Settings

Read Configuration Register			Frequency Configuration Code	Input Clock Frequency (V_{CC}=1.7V-1.95V)
RCR.13	RCR.12	RCR.11		60ns
0	1	0	2	≤ 40MHz
0	1	1	3	≤ 52MHz
1	0	0	4	≤ 66MHz
1	0	1	5	TBD

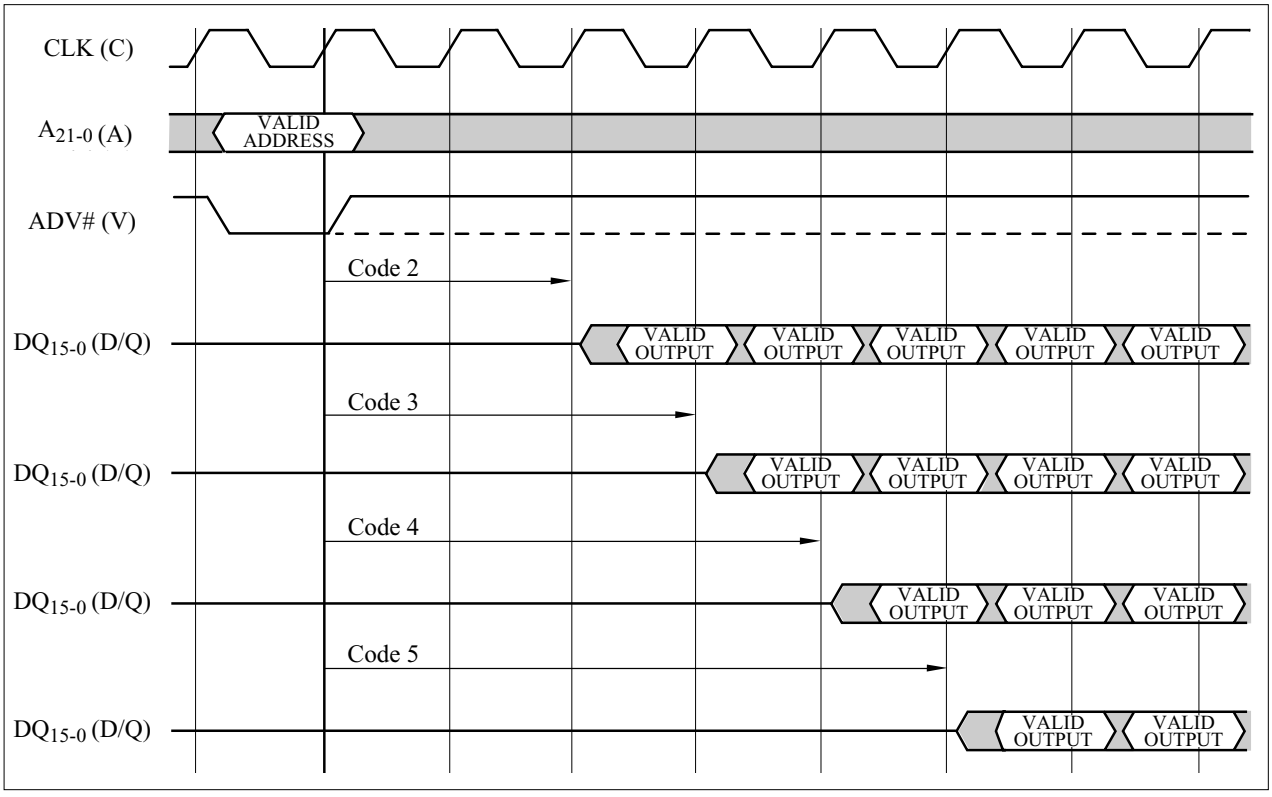


Figure 4. Frequency Configuration

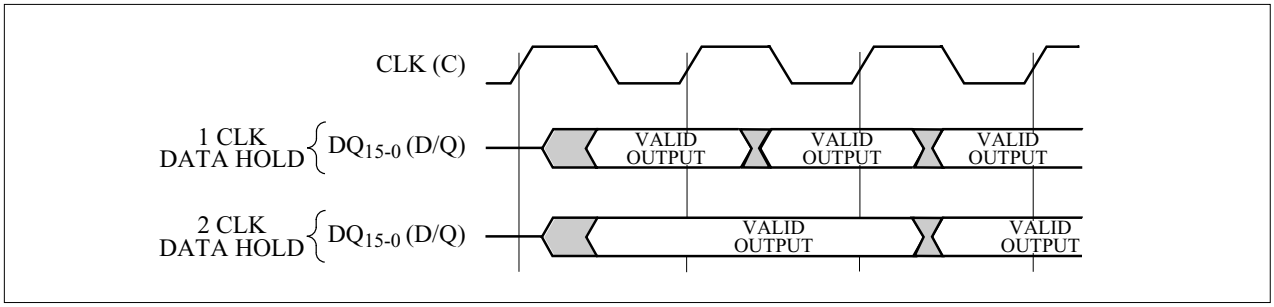


Figure 5. Data Output Configuration

Table 14. Read Sequence and Burst Length

Starting Address [Decimal]	Burst Wrap(1) (RCR.3=)	Burst Addressing Sequence [Decimal]				
		4-Word Burst Length (RCR.2-0=001)		8-Word Burst Length (RCR.2-0=010)		Cotinuous Burst (RCR.2-0=111)
		Linear	Intel	Linear	Intel	Linear
0	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6…
1	0	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7…
2	0	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8…
3	0	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9…
4	0	4-5-6-7	4-5-6-7	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10…
5	0	5-6-7-4	5-4-7-6	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11…
6	0	6-7-4-5	6-7-4-5	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12…
7	0	7-4-5-6	7-6-5-4	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮	⋮
14	0	14-15-12-13	14-15-12-13	14-15-8-9-10-11-12-13	14-15-12-13-10-11-8-9	14-15-16-17-18-19-20…
15	0	15-12-13-14	15-14-13-12	15-8-9-10-11-12-13-14	15-14-13-12-11-10-9-8	15-16-17-18-19-20-21…
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	0-1-2-3	NA	0-1-2-3-4-5-6-7	NA	0-1-2-3-4-5-6…
1	1	1-2-3-4	NA	1-2-3-4-5-6-7-8	NA	1-2-3-4-5-6-7…
2	1	2-3-4-5	NA	2-3-4-5-6-7-8-9	NA	2-3-4-5-6-7-8…
3	1	3-4-5-6	NA	3-4-5-6-7-8-9-10	NA	3-4-5-6-7-8-9…
4	1	4-5-6-7	NA	4-5-6-7-8-9-10-11	NA	4-5-6-7-8-9-10…
5	1	5-6-7-8	NA	5-6-7-8-9-10-11-12	NA	5-6-7-8-9-10-11…
6	1	6-7-8-9	NA	6-7-8-9-10-11-12-13	NA	6-7-8-9-10-11-12…
7	1	7-8-9-10	NA	7-8-9-10-11-12-13-14	NA	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮	⋮
14	1	14-15-16-17	NA	14-15-16-17-18-19-20-21	NA	14-15-16-17-18-19-20…
15	1	15-16-17-18	NA	15-16-17-18-19-20-21-22	NA	15-16-17-18-19-20-21…

NOTE:

1. The burst wrap bit (RCR.3) determines whether 4- or 8-word burst-accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses.

Table 15. Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

000 = No partitioning. Dual Work is not allowed.

001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)

010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.

100 = Plane 0-2 are merged into one partition. (default in a top parameter device)

011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.

See Figure 6 for the detail on partition configuration.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.

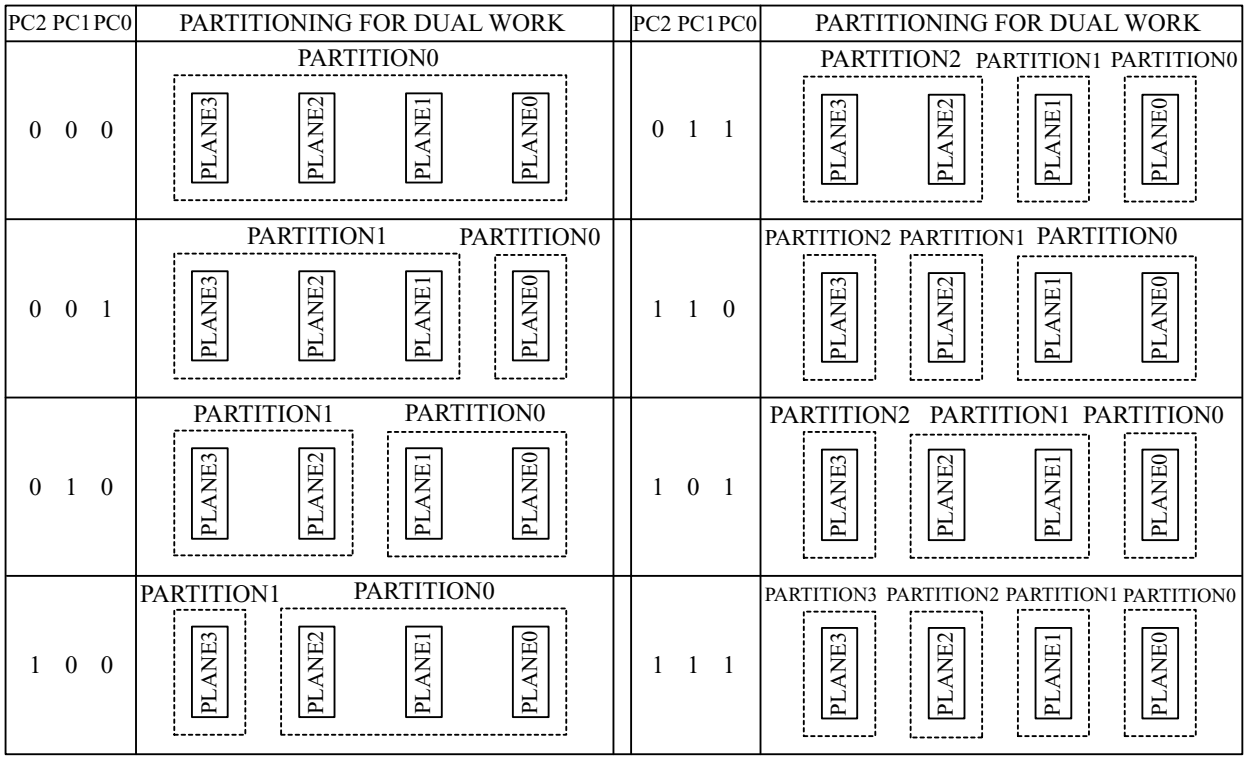


Figure 6. Partition Configuration

1 Electrical Specifications

1.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ...-40°C to +85°C (1)

Storage Temperature

During under Bias..... -40°C to +85°C

During non Bias..... -65°C to +125°C

Voltage On Any Pin

(except V_{CC} and V_{PP})..... -0.5V to V_{CC}+0.5V (2)

V_{CC} and V_{CCQ} Supply Voltage ..... -0.2V to +2.45V (2)

V_{PP} Supply Voltage .....-0.2V to +12.6V (2, 3, 4)

Output Short Circuit Current.....100mA (5)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Maximum DC voltage on V_{PP} may overshoot to +13.0V for periods <20ns.
4. V_{PP} erase/program voltage is normally 1.7V-1.95V. Applying 11.7V-12.3V to V_{PP} during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. V_{PP} may be connected to 11.7V-12.3V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	-40	+25	+85	°C	
V_{CC} Supply Voltage	V_{CC}	1.7	1.8	1.95	V	1
I/O Supply Voltage	V_{CCQ}	1.7	1.8	1.95	V	1
V_{PP} Voltage when Used as a Logic Control	V_{PPH1}	0.90	1.8	1.95	V	1
V_{PP} Supply Voltage	V_{PPH2}	11.7	12	12.3	V	1, 2
Main Block Erase Cycling: $V_{PP}=V_{PPH1}$		100,000			Cycles	
Parameter Block Erase Cycling: $V_{PP}=V_{PPH1}$		100,000			Cycles	
Main Block Erase Cycling: $V_{PP}=V_{PPH2}$, 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: $V_{PP}=V_{PPH2}$, 80 hrs.				1,000	Cycles	
Maximum V_{PP} hours at V_{PPH2}				80	Hours	

NOTES:

1. See DC Characteristics tables for voltage range-specific specification.
2. Applying V_{PP}=11.7V-12.3V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to V_{PP}=11.7V-12.3V is not allowed and can cause damage to the device.

1.2.1 Capacitance(1) (T_A=+25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0.0V		6	8	pF
CE# Input Capacitance	C_{CE}	V_{IN}=0.0V		10	12	pF
Output Capacitance	C_{OUT}	V_{OUT}=0.0V		10	12	pF

NOTE:
1. Sampled, not 100% tested.

1.2.2 AC Input/Output Conditions

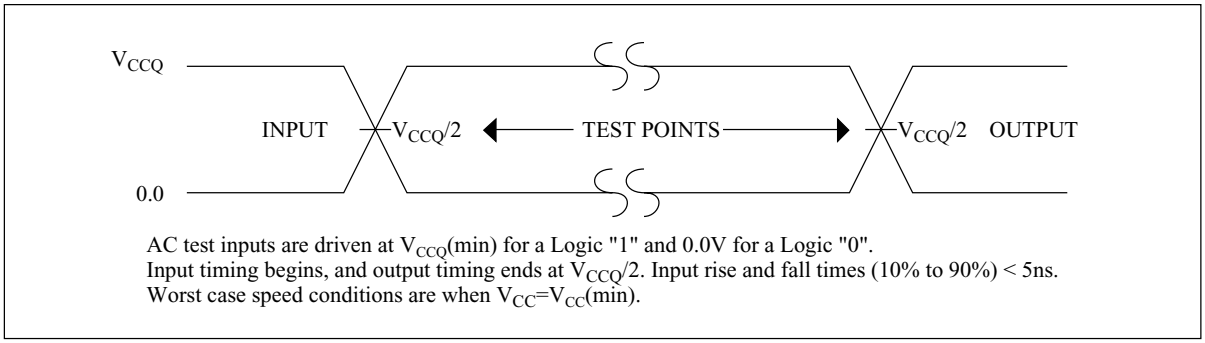


Figure 7. Transient Input/Output Reference Waveform for V_{CC}=1.7V-1.95V

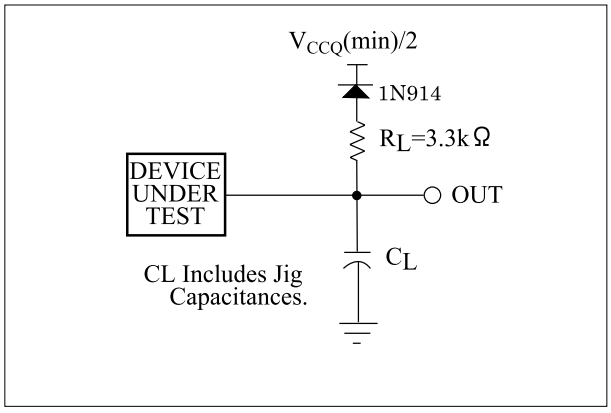


Figure 8. Transient Equivalent Testing Load Circuit

Table 16. Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=1.7V-1.95V	50

1.2.3 DC Characteristics

V_{CC}=1.7V-1.95V

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	-1.0		+1.0	µA	V_{CC}=V_{CC}Max., V_{CCQ}=V_{CCQ}Max., V_{IN}/V_{OUT}=V_{CCQ} or GND
I_{LO}	Output Leakage Current		1	-1.0		+1.0	µA	
I_{CCS}	V_{CC} Standby Current		1		4	20	µA	V_{CC}=V_{CC}Max., CE#=RST#= V_{CCQ}±0.2V, WP#, ADV#= V_{CCQ} or GND
I_{CCAS}	V_{CC} Automatic Power Savings Current		1,5		4	20	µA	V_{CC}=V_{CC}Max., CE#=GND±0.2V, WP#, ADV#= V_{CCQ} or GND
I_{CCD}	V_{CC} Reset Power-Down Current		1		4	20	µA	RST#=GND±0.2V
I_{CCR}	Average V_{CC} Read Current Normal Mode		1,7		15	25	mA	V_{CC}=V_{CC}Max., CE#=V_{IL}, OE#=V_{IH}, f=5MHz
	Average V_{CC} Read Current Page Mode	8 Word Read	1,7		5	10	mA	
	Average V_{CC} Read Current Synchronous CLK=40MHz	Burst Length=4	1,3,8		10	15	mA	V_{CC}=V_{CC}Max., CE#=V_{IL}, OE#=V_{IH}, f=40MHz
		Burst Length=8	1,3,8		10	15	mA	
		Burst Length= Continuous	1,3,8		20	25	mA	
	Average V_{CC} Read Current Synchronous CLK=52MHz	Burst Length=4	1,3,8		15	20	mA	V_{CC}=V_{CC}Max., CE#=V_{IL}, OE#=V_{IH}, f=52MHz
		Burst Length=8	1,3,8		15	20	mA	
		Burst Length= Continuous	1,3,8		25	30	mA	
I_{CCW}	V_{CC} (Page Buffer) Program, Advanced Factory Program Current		1,6,8		20	60	mA	V_{PP}=V_{PPH1}
			1,6,8		10	20	mA	V_{PP}=V_{PPH2}
I_{CCE}	V_{CC} Block Erase Current		1,6,8		10	30	mA	V_{PP}=V_{PPH1}
			1,6,8		4	10	mA	V_{PP}=V_{PPH2}
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current		1,2,8		10	200	µA	CE#=V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current		1,7,8		2	5	µA	V_{PP}≤V_{CC}
I_{PPW}	V_{PP} (Page Buffer) Program, Advanced Factory Program Current		1,6,7,8		2	5	µA	V_{PP}=V_{PPH1}
			1,6,7,8		10	30	mA	V_{PP}=V_{PPH2}
I_{PPE}	V_{PP} Block Erase Current		1,6,7,8		2	5	µA	V_{PP}=V_{PPH1}
			1,6,7,8		5	15	mA	V_{PP}=V_{PPH2}

DC Characteristics (Continued)

V_{CC}=1.7V-1.95V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{PPWS}	V_{PP} (Page Buffer) Program Suspend Current	1,7,8		2	5	µA	$V_{PP}=V_{PPH1}$
		1,7,8		10	200	µA	$V_{PP}=V_{PPH2}$
I_{PPES}	V_{PP} Block Erase Suspend Current	1,7,8		2	5	µA	$V_{PP}=V_{PPH1}$
		1,7,8		10	200	µA	$V_{PP}=V_{PPH2}$
V_{IL}	Input Low Voltage	6	-0.4		0.4	V	
V_{IH}	Input High Voltage	6	V_{CCQ} -0.4		V_{CCQ} + 0.4	V	
V_{OL}	Output Low Voltage	6			0.1	V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., I_{OL}=100µA
V_{OH}	Output High Voltage	6	V_{CCQ} -0.1			V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., I_{OH}=-100µA
V_{PPLK}	V_{PP} Lockout during Normal Operations	4,6,7			0.4	V	
V_{PPH1}	V_{PP} during Block Erase, (Page Buffer) Program or OTP Program Operations	7	0.9	1.8	1.95	V	
V_{PPH2}	V_{PP} during Block Erase, Advanced Factory Program, (Page Buffer) Program or OTP Program Operations	7	11.7	12	12.3	V	
V_{LKO}	V_{CC} Lockout Voltage		1.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC}=1.8V and T_A=+25°C unless V_{CC} is specified.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
3. The burst wrap bit (RCR.3) determines whether 4- or 8-word burst-accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses.
4. Block erase, advanced factory program, (page buffer) program and OTP program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max.) and V_{PPH1}(min.), between V_{PPH1}(max.) and V_{PPH2}(min.) and above V_{PPH2}(max.).
5. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
6. Sampled, not 100% tested.
7. V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, advanced factory program, (page buffer) program and OTP program cannot be executed and should not be attempted.
   Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{CC} power bus.
   Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum.
8. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.

1.2.4 AC Characteristics - Read-Only Operations(1)

V_{CC}=1.7V-1.95V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{CLK}	CLK Period		19		ns
t_{CH} (t_{CL})	CLK High (Low) Time		5		ns
t_{CHCL} (t_{CLCH})	CLK Fall (Rise) Time			3	ns
t_{AVCH}	Address Setup to CLK		9		ns
t_{VLCH}	ADV# Setup to CLK		10		ns
t_{ELCH}	CE# Setup to CLK		9		ns
t_{CHQV}	CLK to Output Delay			14	ns
t_{CHQX}	Output Hold from CLK		3		ns
t_{CHAX}	Address Hold from CLK		10		ns
t_{CHTV}	CLK to WAIT Valid			14	ns
t_{ELTV}	CE# Low to WAIT Valid			14	ns
t_{EHTZ}	CE# High to WAIT High Z			20	ns
t_{EHEL}	CE# High between Subsequent Synchronous Reads	3	15		ns
t_{AVVH}	Address Setup to ADV#		10		ns
t_{ELVH}	CE# Setup to ADV#		10		ns
t_{AVAV}	Read Cycle Time		60		ns
t_{AVQV}	Address to Output Delay			60	ns
t_{ELQV}	CE# to Output Delay	4		60	ns
t_{VLQV}	ADV# to Output Delay			60	ns
t_{VLVH}	ADV# Pulse Width Low		10		ns
t_{VHVL}	ADV# Pulse Width High		10		ns
t_{VHAX}	Address Hold from ADV#		9		ns
t_{APA}	Page Address Access Time			20	ns
t_{GLQV}	OE# to Output Delay	4		20	ns
t_{PHQV}	RST# High to Output Delay			150	ns
t_{EHQZ}, t_{GHQZ}	CE# or OE# to Output in High Z, Whichever Occurs First	2		15	ns
t_{ELQX}	CE# to Output in Low Z	2	0		ns
t_{GLQX}	OE# to Output in Low Z	2	0		ns
t_{OH}	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. Applies only to subsequent synchronous reads.
4. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact to t_{ELQV}.

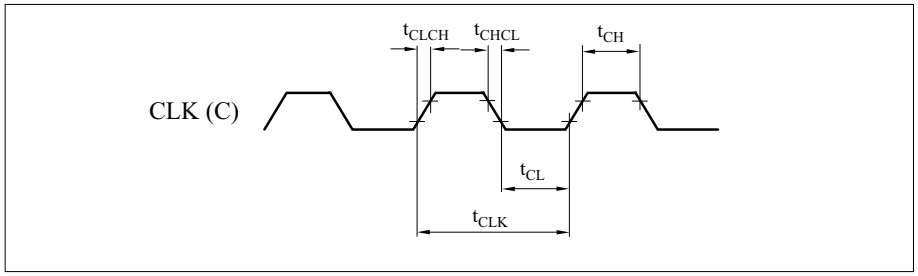


Figure 9. AC Waveform for CLK Input

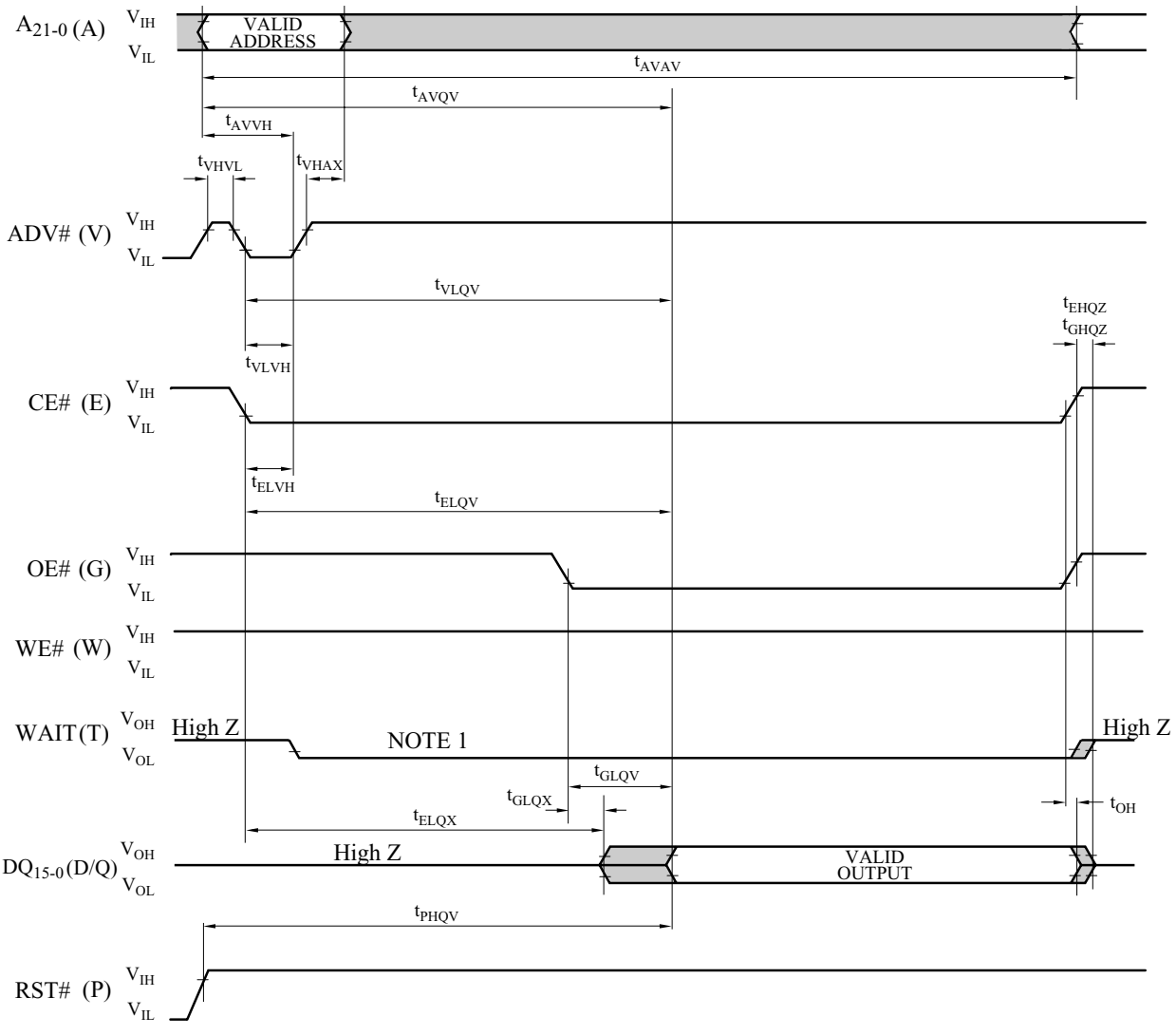
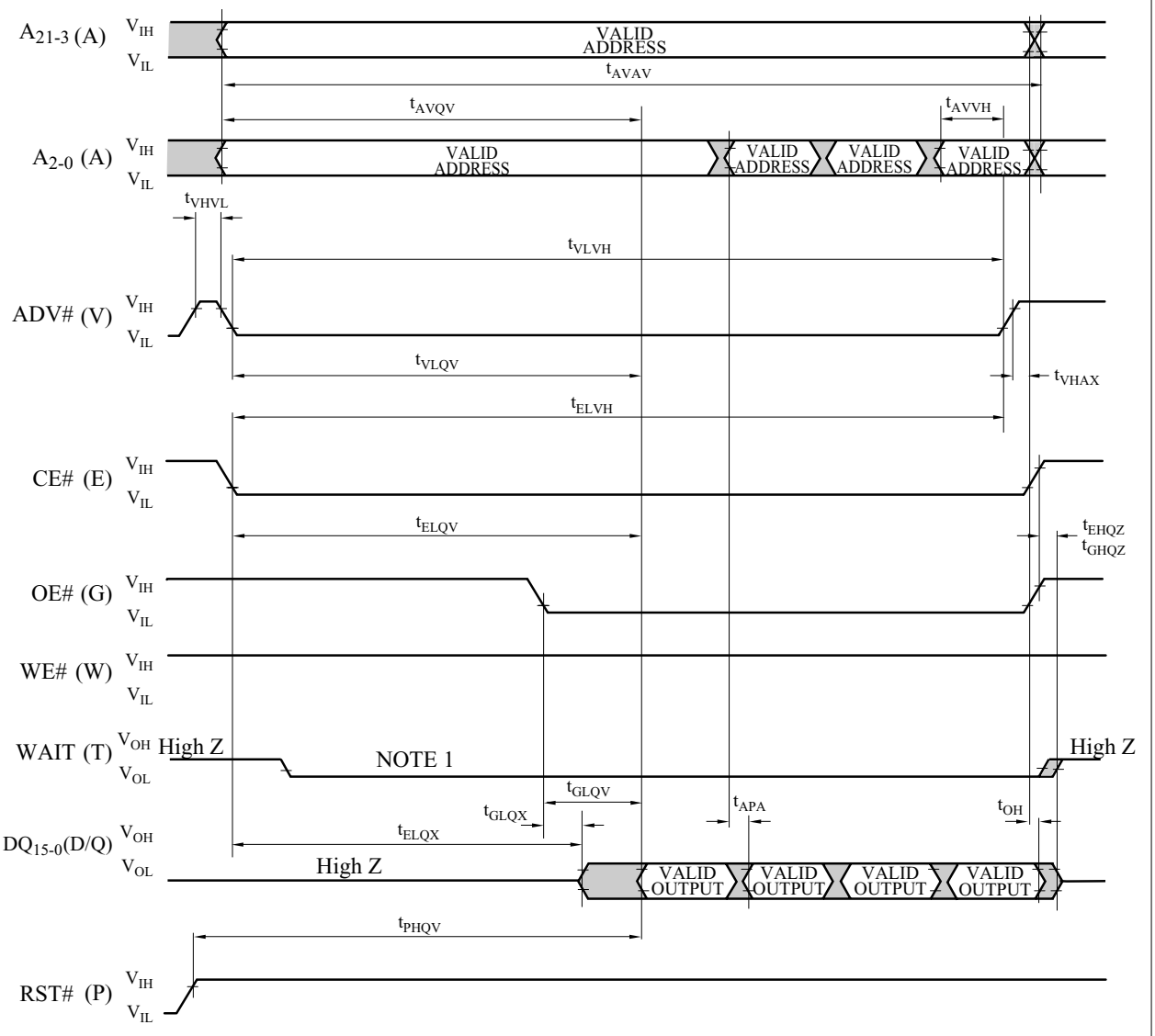
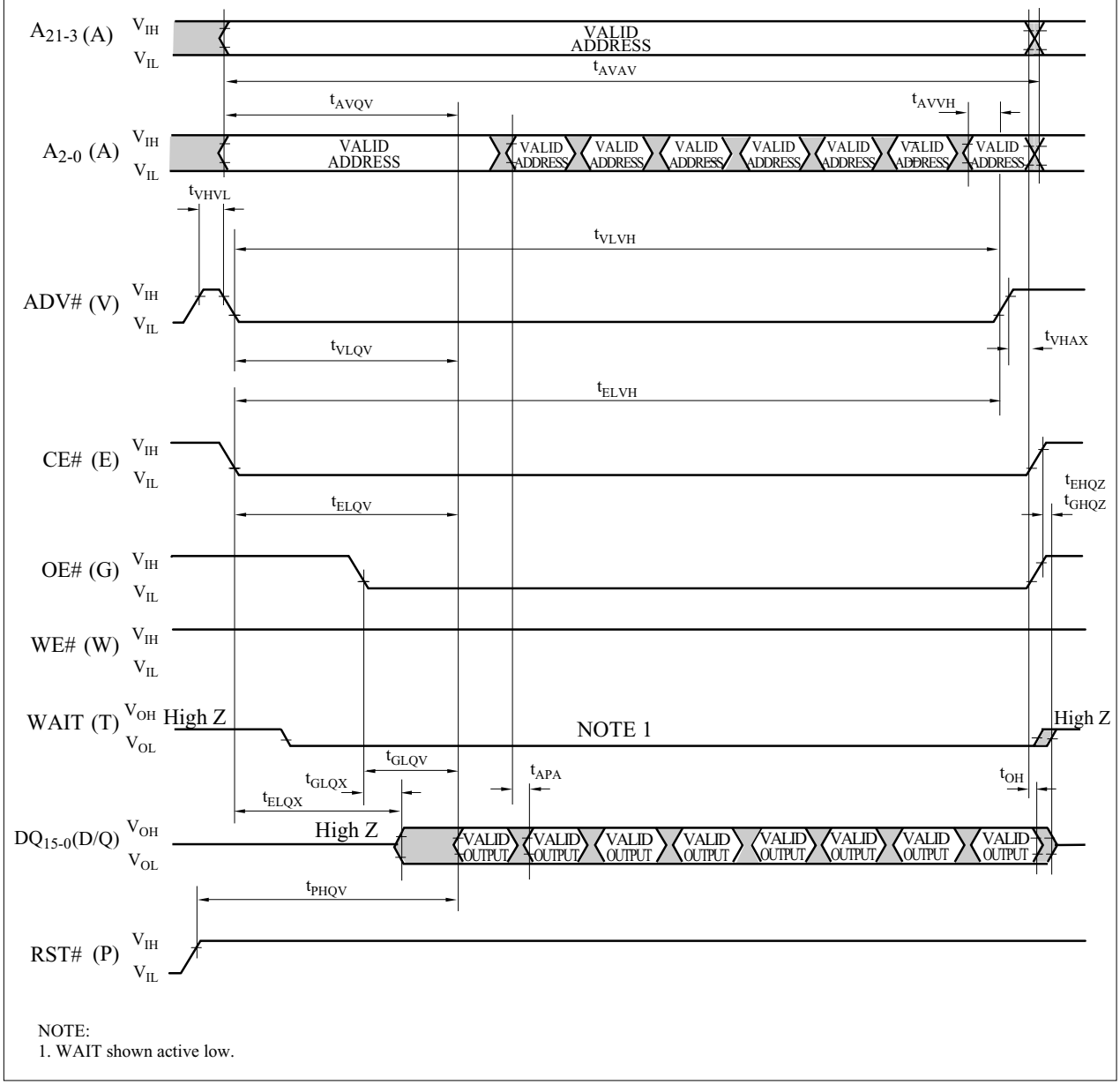


Figure 10. AC Waveform for Single Asynchronous Read Operations
from Status Register, Identifier Codes, OTP Block or Query Code



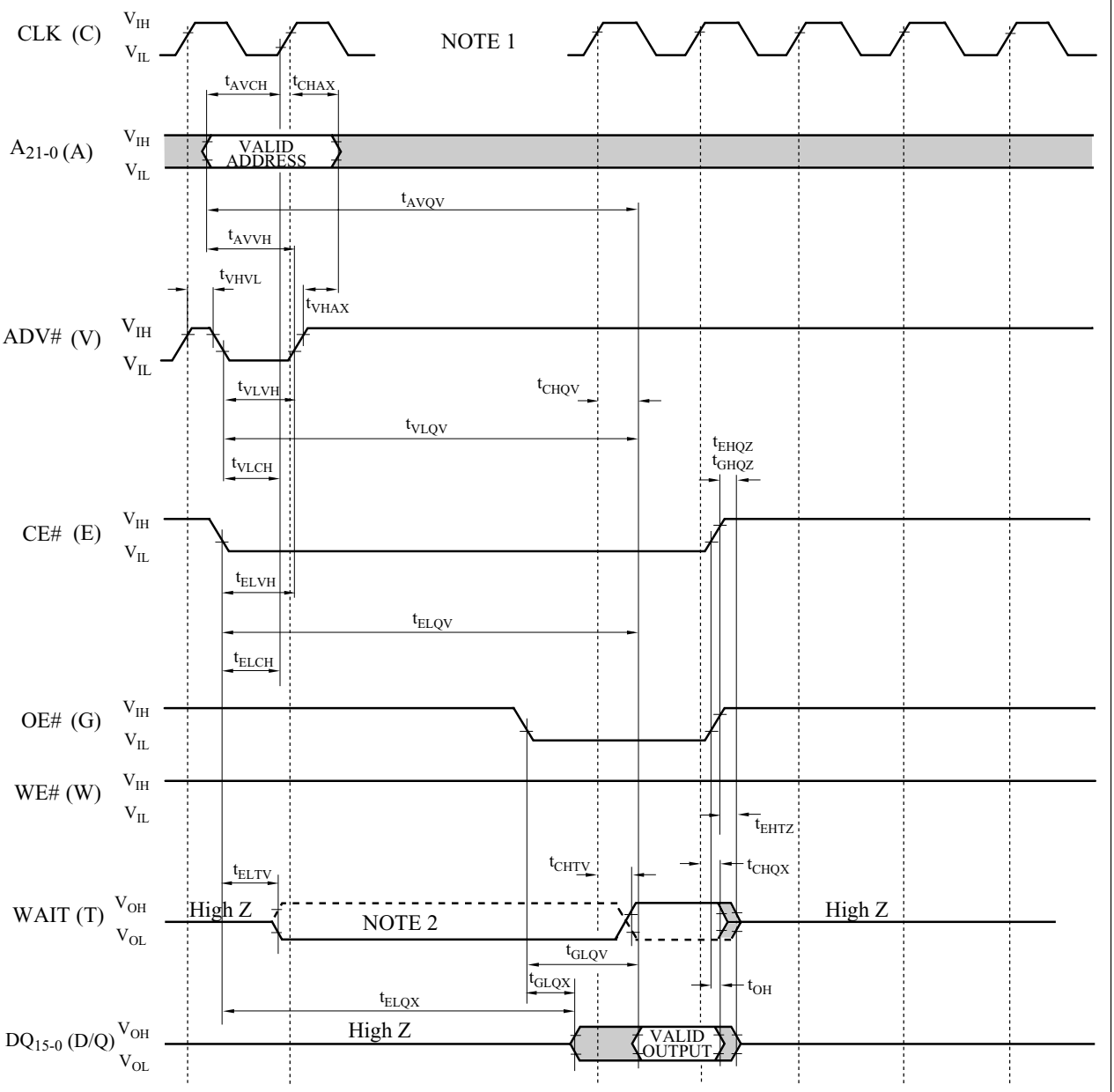
NOTE:
1. WAIT shown active low.

Figure 11. AC Waveform for Asynchronous 4-Word Page Mode
Read Operations from Main Blocks or Parameter Blocks



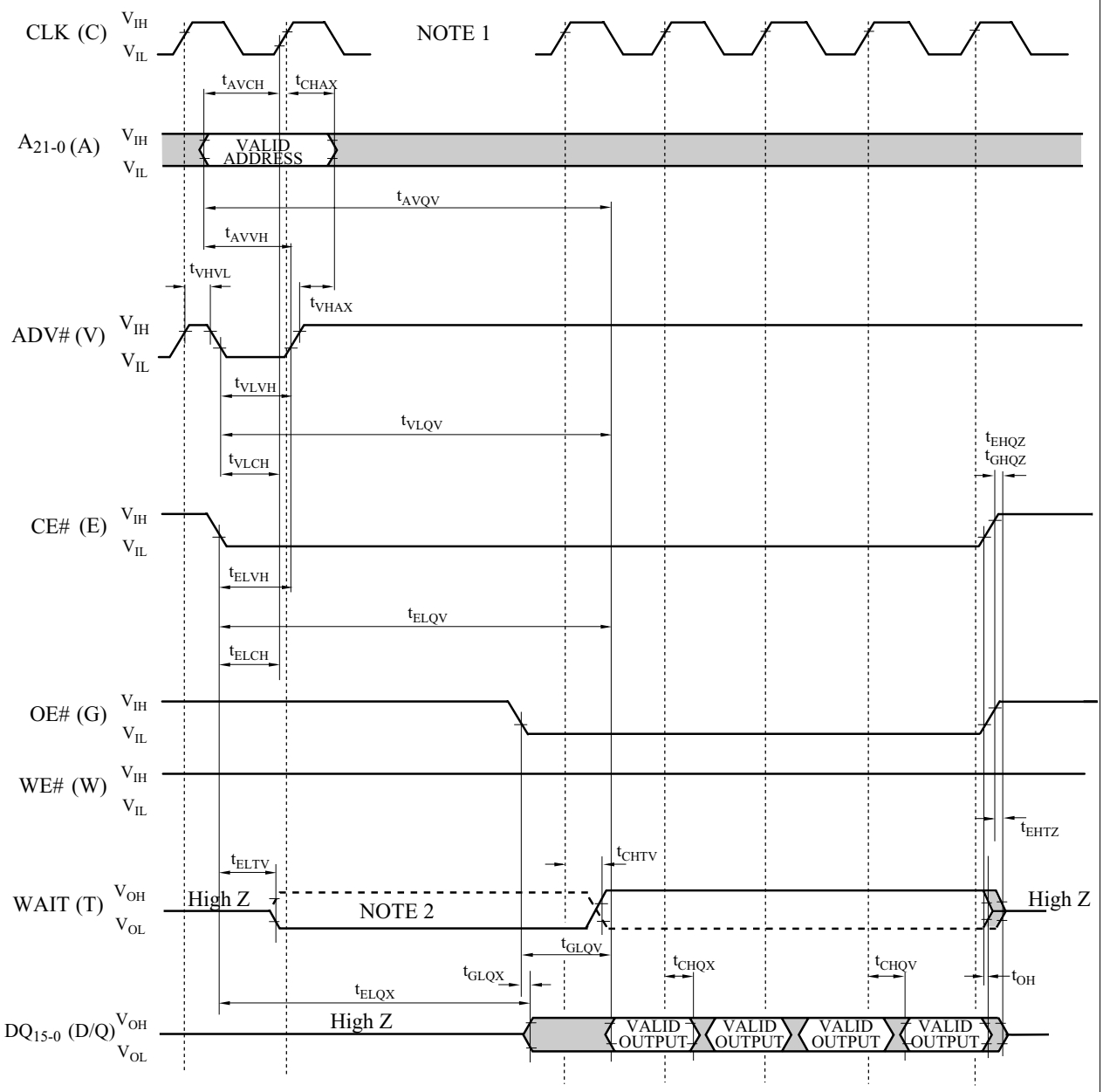
NOTE:
1. WAIT shown active low.

Figure 12. AC Waveform for Asynchronous 8-Word Page Mode
Read Operations from Main Blocks or Parameter Blocks



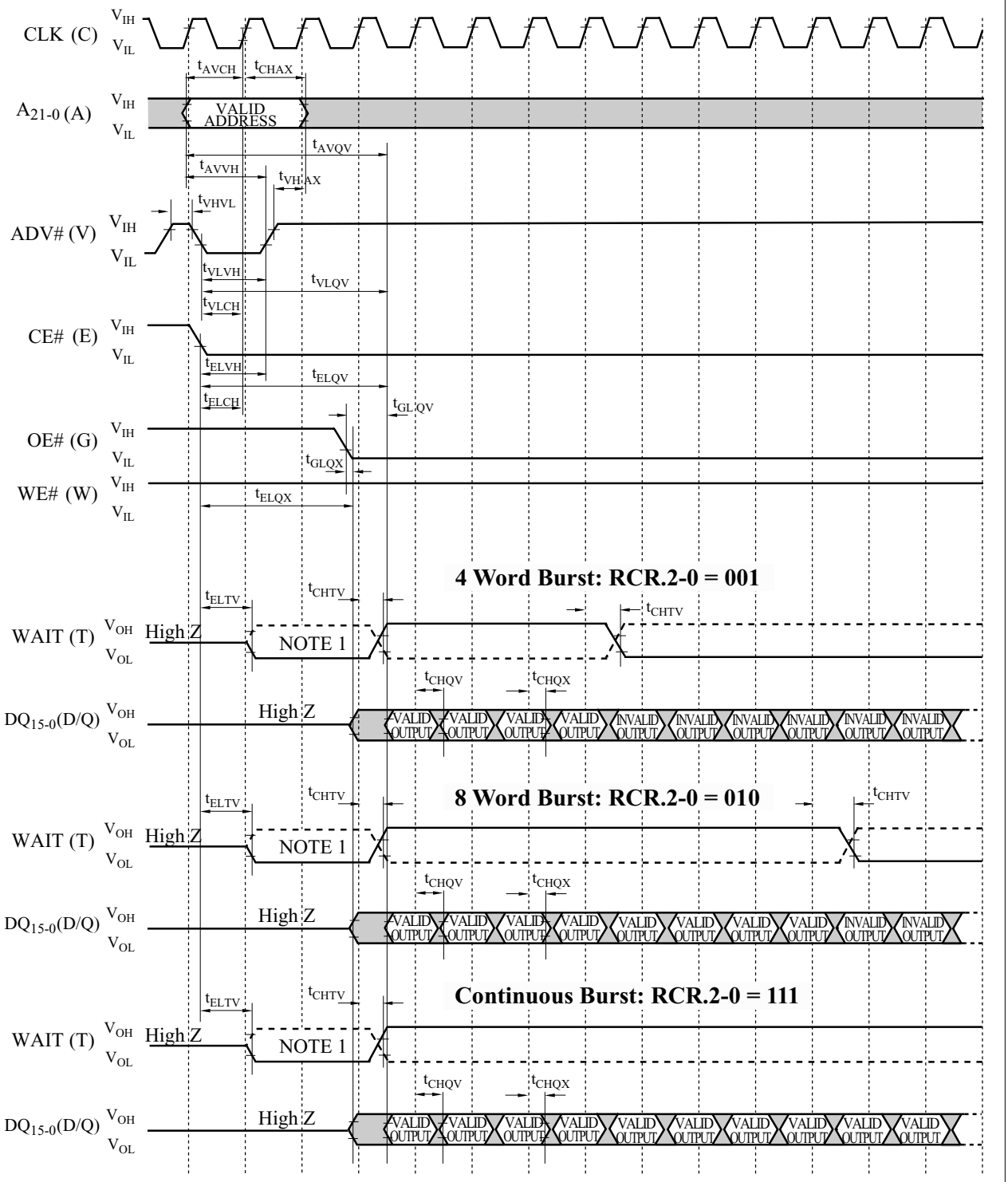
NOTE:
1. Depending upon the frequency configuration code in the read configuration register, insert clock cycles:
   Frequency Configuration Code 2, insert two clock cycles
   Frequency Configuration Code 3, insert three clock cycles
   Frequency Configuration Code 4, insert four clock cycles
   Frequency Configuration Code 5, insert five clock cycles
2. WAIT (shown active low) configuration allows assertion one CLK cycle before or during an output delay.

Figure 13. AC Waveform for Single Synchronous Read Operations
from Status Register, Identifier Codes, OTP Block or Query Code



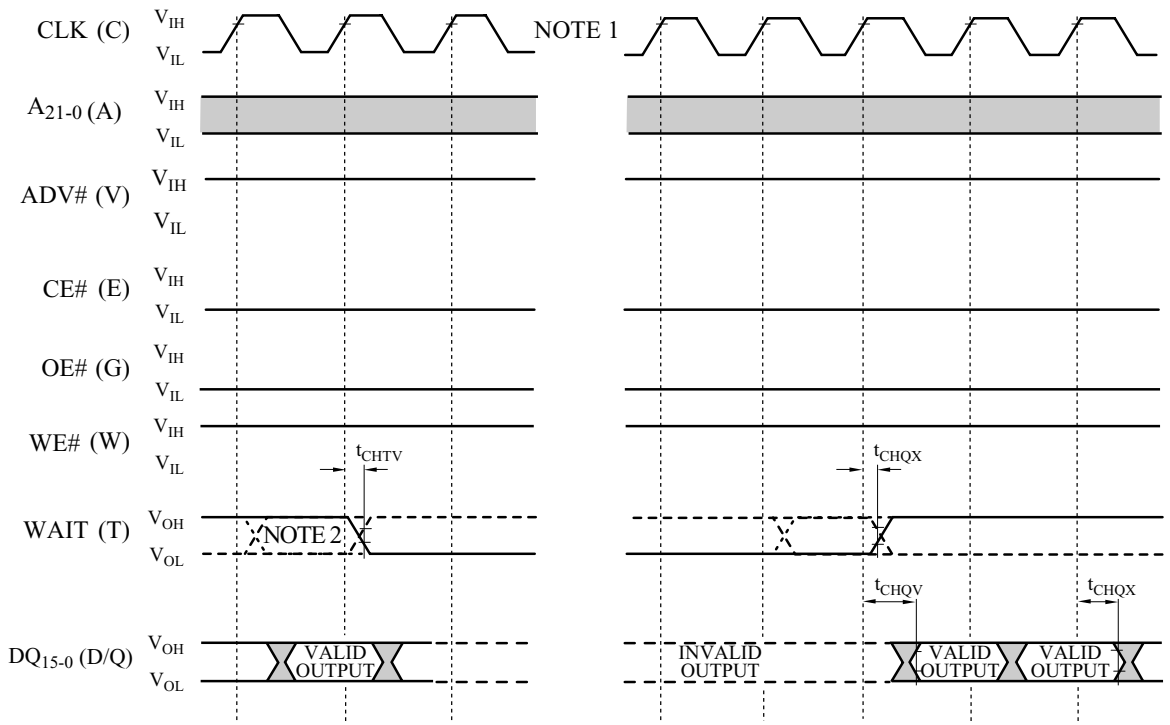
NOTE:
1. Depending upon the frequency configuration code in the read configuration register, insert clock cycles:
   Frequency Configuration Code 2, insert two clock cycles
   Frequency Configuration Code 3, insert three clock cycles
   Frequency Configuration Code 4, insert four clock cycles
   Frequency Configuration Code 5, insert five clock cycles
2. WAIT (shown active low) configuration allows assertion one CLK cycle before or during an output delay.

Figure 14. AC Waveform for Synchronous Burst Mode Read Operations
from Main Blocks or Parameter Blocks (4 Word Burst: RCR.2-0=001)



NOTE:
1. WAIT (shown active low) configuration allows assertion one CLK cycle before or during an output delay.

Figure 15. AC Waveform for Synchronous Burst Mode Read Operations
from Main Blocks or Parameter Blocks (Frequency Configuration: RCR.13-11=010)



NOTES:
1. This delay occurs only in continuous burst mode or 4-, 8-word burst with no-wrap mode.
2. WAIT (shown active low) configuration allows assertion one CLK cycle before or during an output delay.

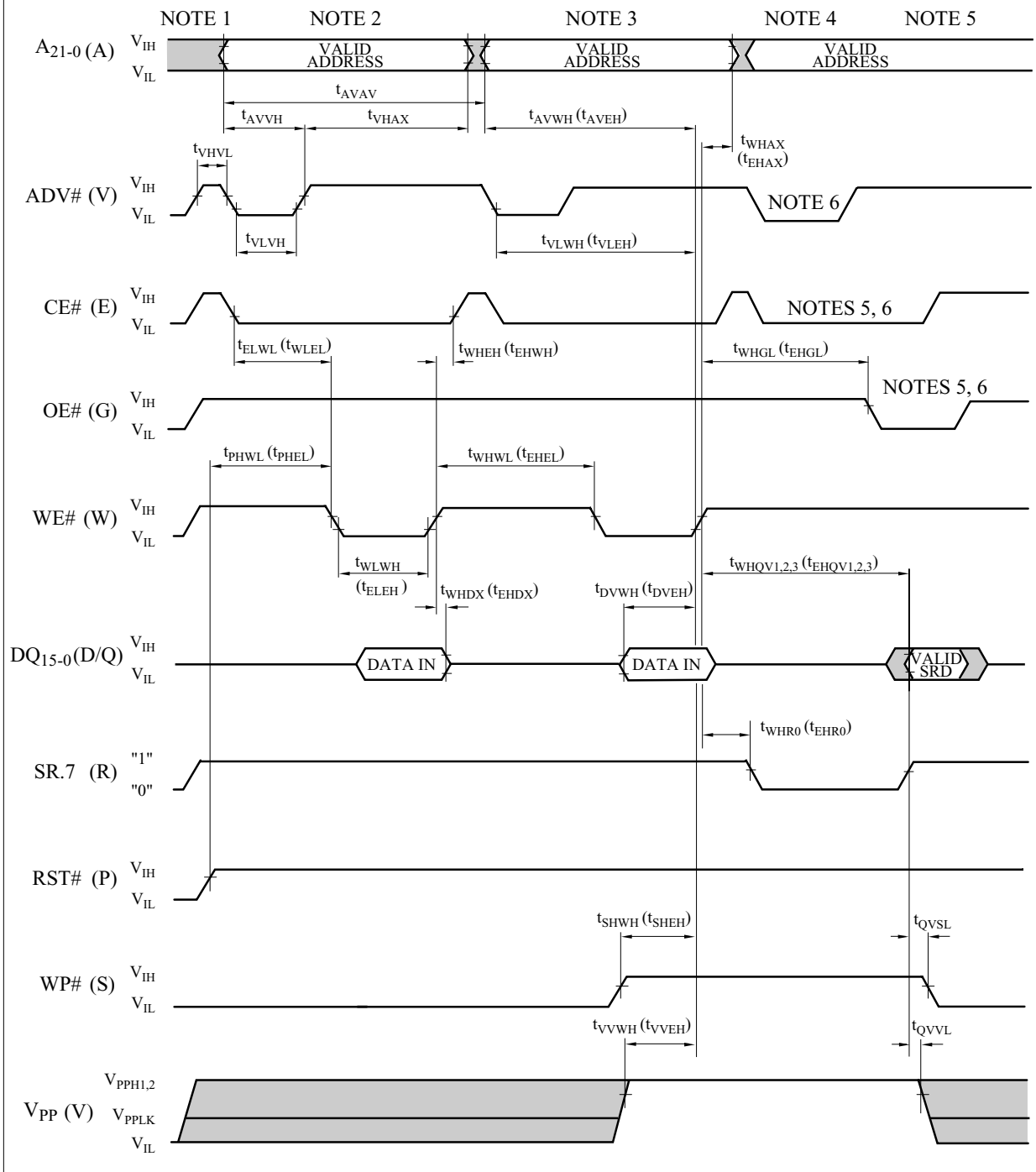
Figure 16. AC Waveform for an Output Delay when Continuous Burst Read with Data Output Configurations Set to One Clock

1.2.5 AC Characteristics - Write Operations[1, 2]

V_{CC}=1.7V-1.95V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		60		ns
t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (CE#) Going Low	3	150		ns
t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Going Low		0		ns
t_{WLWH} (t_{ELEH})	WE# (CE#) Pulse Width	4	40		ns
t_{VLVH}	ADV# Pulse Width		10		ns
t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) Going High	8	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) Going High	8	40		ns
t_{VLWH} (t_{VLEH})	ADV# Setup to WE# (CE#) Going High		40		ns
t_{AVVH}	Address Setup to ADV# Going High		10		ns
t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		0		ns
t_{VHAX}	Address Hold from ADV# High		9		ns
t_{WHWL} (t_{EHEL})	WE# (CE#) Pulse Width High	5	20		ns
t_{SHWH} (t_{SHEH})	WP# High Setup to WE# (CE#) Going High	3	0		ns
t_{VVWH} (t_{VVEH})	V_{PP} Setup to WE# (CE#) Going High	3	200		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		30		ns
t_{QVSL}	WP# High Hold from Valid SRD	3, 6	0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD	3, 6	0		ns
t_{WHR0} (t_{EHR0})	WE# (CE#) High to SR.7 Going "0"	3, 7		t_{AVQV}+ 19	ns

NOTES:
1. The timing characteristics for reading the status register during block erase, advanced factory program, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling edge of CE# or WE# (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. V_{PP} should be held at $V_{PP}=V_{PPH1/2}$ until determination of block erase, (page buffer) program or OTP program success (SR.1/3/4/5=0) and held at $V_{PP}=V_{PPH2}$ until determination of advanced factory program success (SR.0/1/3/4=0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command=t_{AVQV}+100ns.
8. Refer to Table 6 for valid address and data for block erase, advanced factory program, (page buffer) program, OTP program or lock bit configuration.



NOTES:
1. V_{CC} power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, OE#, CE# and ADV# must be driven active, and WE# de-asserted.

Figure 17. AC Waveform for Write Operations

1.2.6 Reset Operations

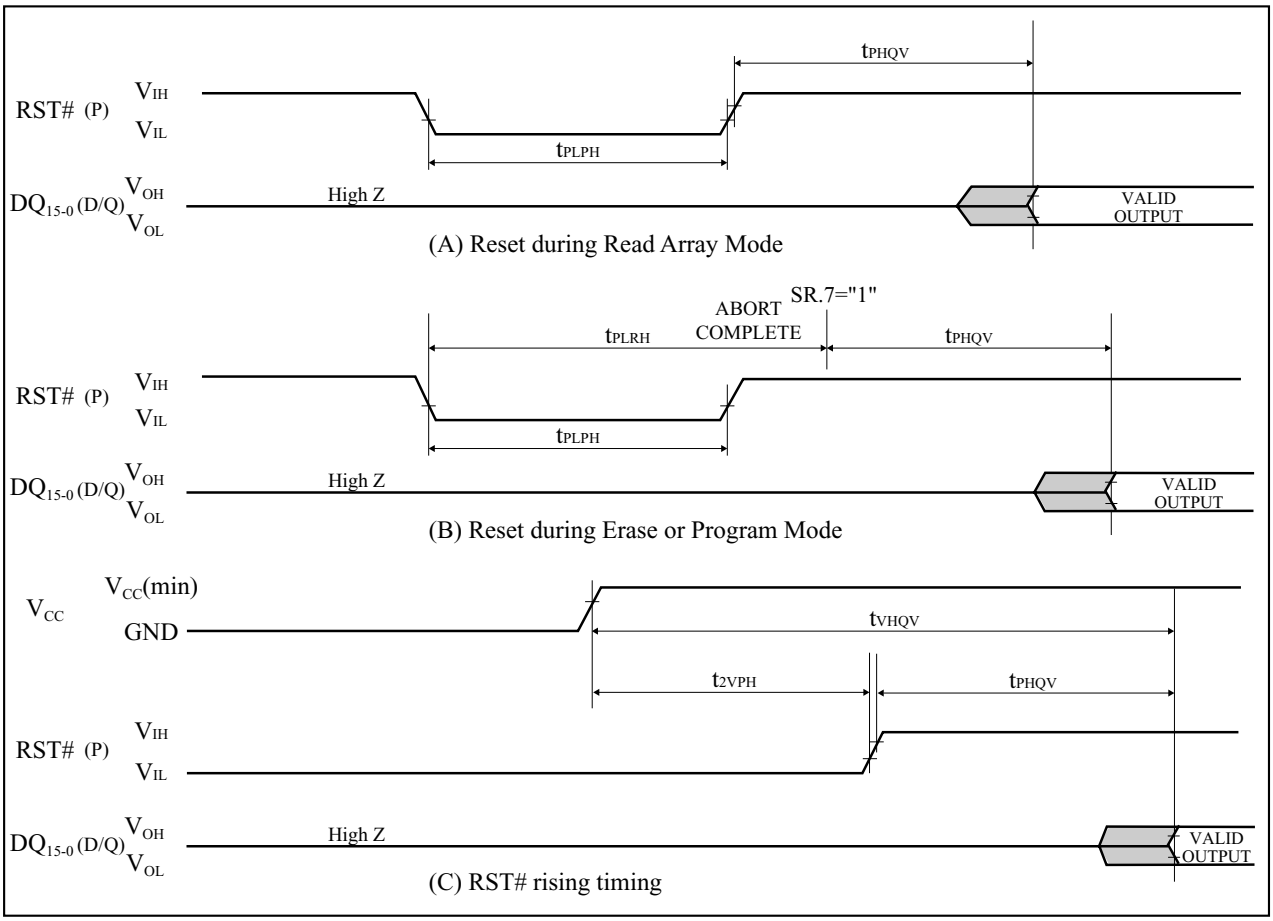


Figure 18. AC Waveform for Reset Operations

Reset AC Specifications (V_{CC}=1.7V-1.95V, T_A=-40°C to +85°C)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RST# Low to Reset during Read (RST# should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	RST# Low to Reset during Erase or Program	1, 3, 4		20	µs
t_{2VPH}	V_{CC} 1.7V to RST# High	1, 3, 5	100		ns
t_{VHQV}	V_{CC} 1.7V to Output Delay	3		1	ms

NOTES:
1. A reset time, t_{PHQV}, is required from the later of SR.7 going "1" or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RST# asserted while a block erase, advanced factory program, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RST# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

1.2.7 Block Erase, Advanced Factory Program, (Page Buffer) Program and OTP Program Performance(3)

V_{CC}=1.7V-1.95V, T_A=-40°C to +85°C

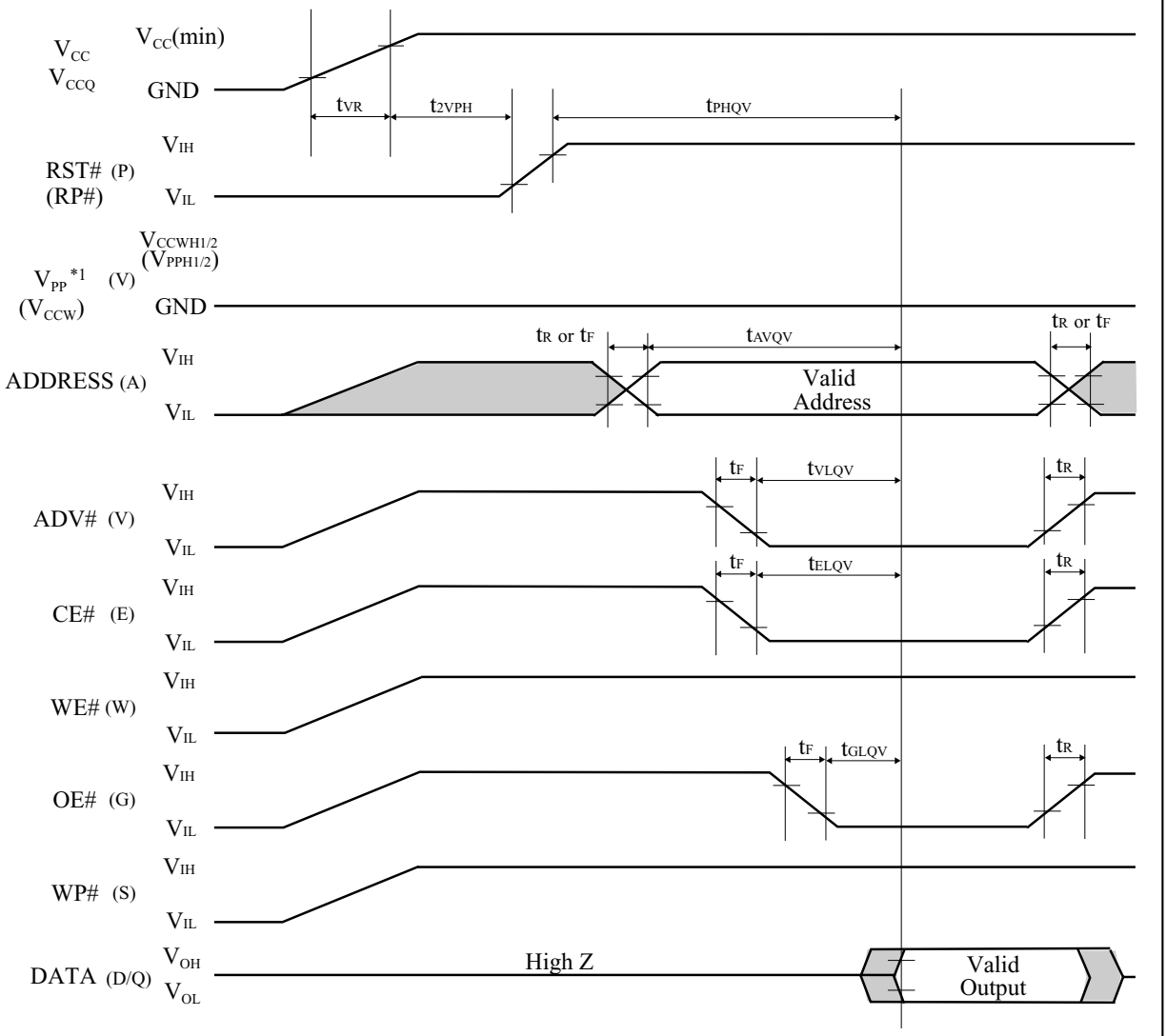
Symbol	Parameter	Notes	PBP (Page Buffer) is Used, AFP (Advanced Factory Program) is Used or not	$V_{PP}=V_{PPH1}$ (In System)			$V_{PP}=V_{PPH2}$ (In Manufacturing)			Unit
				Min.	Typ.(1)	Max.(2)	Min.	Typ.(1)	Max.(2)	
t_{WPB}	4K-Word Parameter Block Program Time	2	-		0.09	0.23		0.04	0.07	s
		2	PBP		0.05	0.2		0.02	0.06	s
		2, 6, 7	AFP		-	-		0.015	-	s
t_{WMB}	32K-Word Main Block Program Time	2	-		0.72	1.8		0.31	0.6	s
		2	PBP		0.34	1.4		0.17	0.5	s
		2, 6	AFP		-	-		0.12	-	s
t_{WHQV1}/ t_{EHQV1}	Word Program Time	2	-		22	150		9	130	µs
		2	PBP		10	100		5	90	µs
		2, 6	AFP		-	-		3.5	16	µs
t_{WHOV1}/ t_{EHOV1}	OTP Program Time	2	-		72	800		27	185	µs
t_{WHQV2}/ t_{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	2.5		0.2	2.5	s
t_{WHQV3}/ t_{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	4		0.5	4	s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10		5	10	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20		5	20	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			µs
t_{ARES}	Latency Time for AFP Set-Up	2, 6	AFP		-	-		-	5	µs
	Latency for AFP Verify Transition	2, 6	AFP		-	-		2.7	5.6	µs
	Latency for AFP Verify	2, 6	AFP		-	-		1.7	130	µs

NOTES:
1. Typical values measured at V_{CC}=1.8V, V_{PP}=1.8V or 12V, and T_A=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1".
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.
6. AFP mode is allowed only when T_A=+20°C to +30°C.
7. In AFP mode, eight 4K-word parameter blocks are programmed at a time. Specification shown above is the program time per each 4K-word parameter block.

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the design, which applies V_{PP} (V_{CCW}) to 0V during read operations and $V_{PPH1/2}$ ($V_{CCWH1/2}$) during write or erase operations.
See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

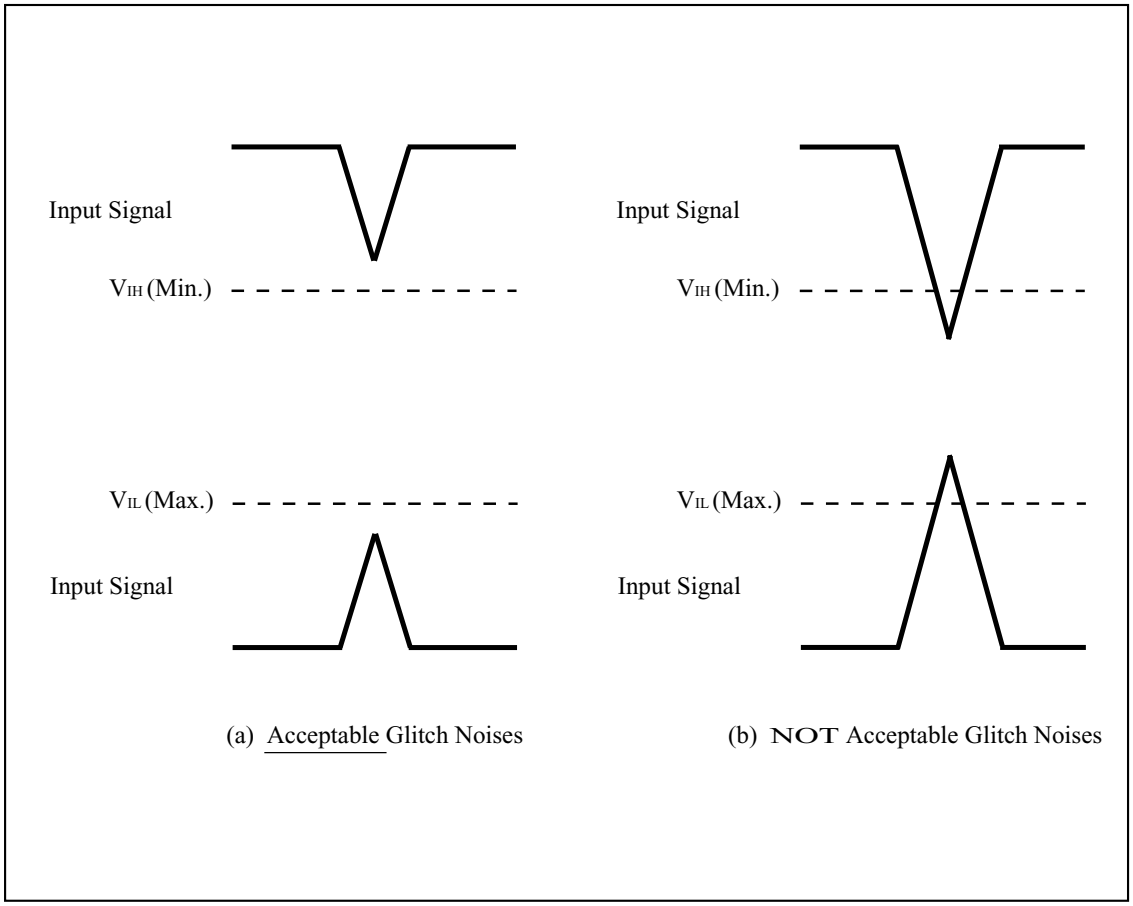


Figure A-2. Waveform for Glitch Noises

See the “DC CHARACTERISTICS“ described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

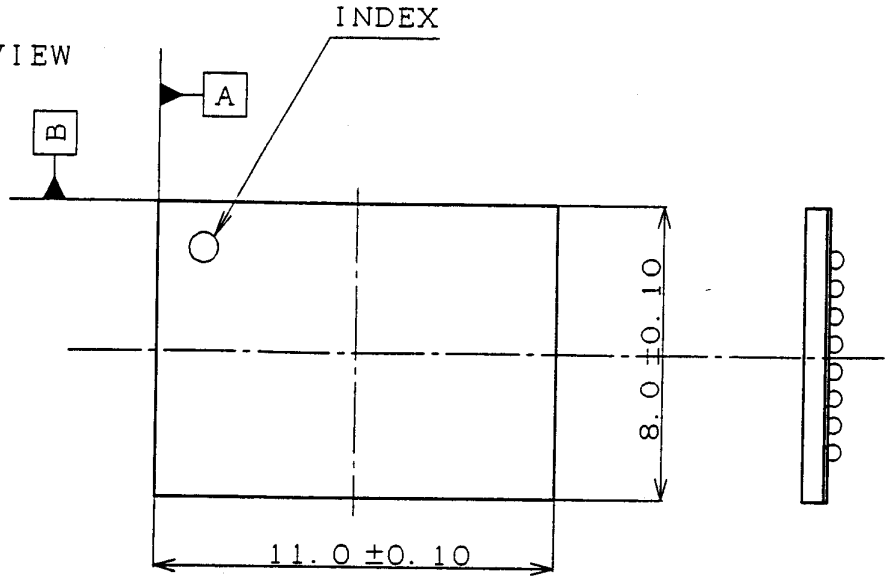
A-2 RELATED DOCUMENT INFORMATION(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

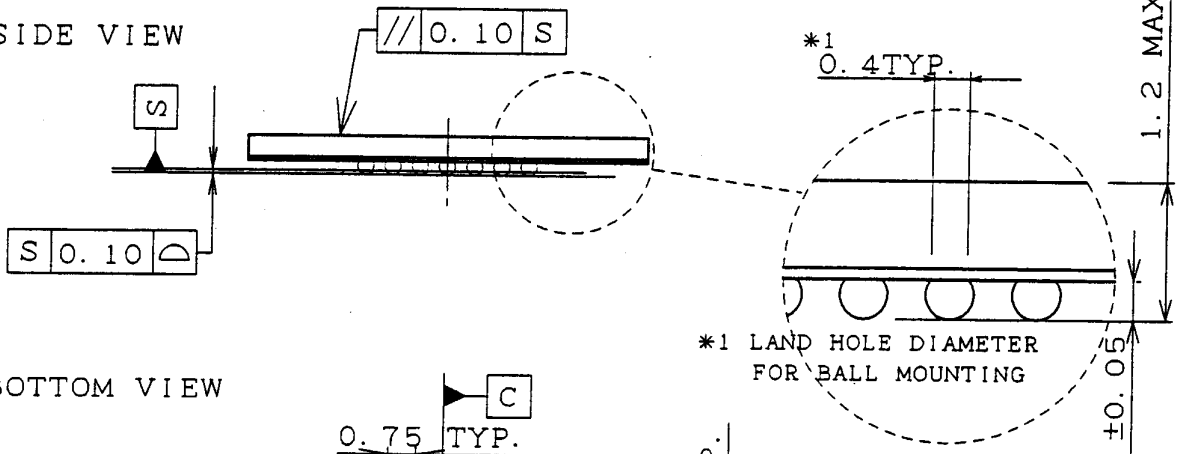
NOTE:
1. International customers should contact their local SHARP or distribution sales office.

SHARP

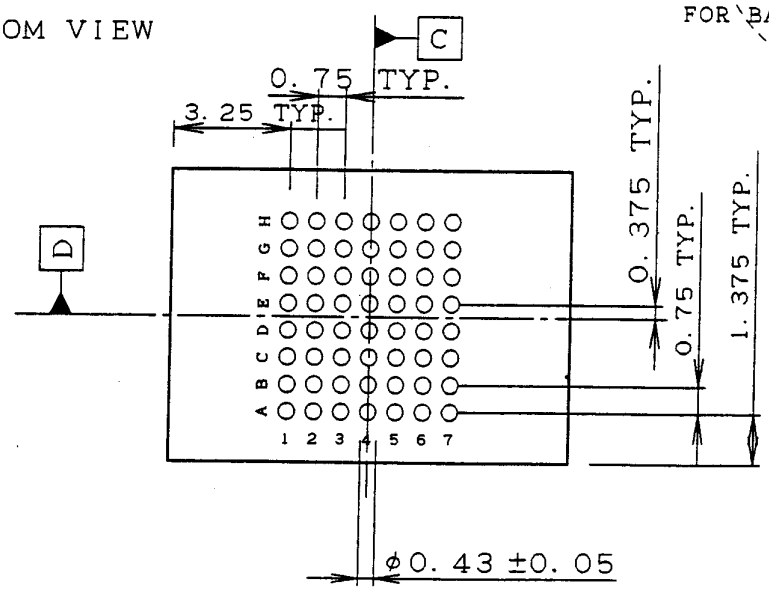
TOP VIEW



SIDE VIEW



BOTTOM VIEW



⊕	φ0.30 Ⓜ	S	AB
⊕	φ0.15 Ⓜ	S	CD

改訂日 DATE	改訂記事 REVISE	担当 CHARGE
日付 DATE	2002. 10. 28	

設計 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVE
Y. Mats				

尺度 SCALE	5/1
単位 UNIT	1=1/1mm
端子マトリクス MATRIX	7 × 8
端子数 COUNTS	56
端子ピッチ PITCH	0.75

シャープ株式会社
IC事業本部
実装プロセス技術部
SHARP CORPORATION

適用機種 APPLICABLE MODEL	
名称 NAME	CSP056-P-0811 (FBGA056-P-0811) (0.75 Pitch)
コード CODE	
図番 DRAWING No.	AA2231

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