LH28F128BFHED-PWTL90

Flash Memory

128M (8M × 16)

(Model No.: LHF12F01)

Spec No.: EL142079

Issue Date: February 26, 2002

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  (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

    - Office electronics
    - Instrumentation and measuring equipment
    - Machine tools
    - Audiovisual equipment
    - Home appliance
    - Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment <u>which demands high reliability</u>, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

    - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
    - Mainframe computers
    - Traffic control systems
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    - Rescue and security equipment
    - Other safety devices and safety equipment, etc.

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    - Aerospace equipment
    - Communications equipment for trunk lines
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    - Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

LH28F128BFHED-PWTL90
128Mbit (8Mbit×16)
Page Mode Dual Work Flash MEMORY

- 128M density with 16Bit I/O Interface
  - 2 Bank Enable (BE_0#, BE_1#) Control
- High Performance Reads
  - 90/35ns 8-Word Page Mode
- Configurative 8-Plane Dual Work
  - Flexible Partitioning
  - Read operations during Block Erase or (Page Buffer) Program
  - Status Register for Each Partition
- Low Power Operation
  - 2.7V Read and Write Operations
  - Automatic Power Savings Mode Reduces I_{CCR} in Static Mode
- Enhanced Code + Data Storage
  - 5μs Typical Erase/Program Suspends
- OTP (One Time Program) Block
  - 4-Word Factory-Programmed Area
  - 4-Word User-Programmable Area
- High Performance Program with Page Buffer
  - 16-Word Page Buffer
  - 5μs/Word (Typ.) at 12V V_{PP}
- Operating Temperature -40°C to +85°C
- CMOS Process (P-type silicon substrate)
- Flexible Blocking Architecture
  - Sixteen 4K-word Parameter Blocks
  - Two-hundred and fifty-four 32K-word Main Blocks
  - Top and Bottom Parameter Location
- Enhanced Data Protection Features
  - Individual Block Lock and Block Lock-Down with Zero-Latency
  - All blocks are locked at power-up or device reset.
  - Absolute Protection with $V_{PP} \leq V_{PPLK}$
  - Block Erase, Bank Erase, (Page Buffer) Word Program Lockout during Power Transitions
- Automated Erase/Program Algorithms
  - 3.0V Low-Power 11μs/Word (Typ.) Programming
  - 12V No Glue Logic 9μs/Word (Typ.) Production Programming and 0.5s Erase (Typ.)
- Cross-Compatible Command Support
  - Basic Command Set
  - Common Flash Interface (CFI)
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- 48-Lead TSOP
- ETOX^{TM*} Flash Technology
- Not designed or rated as radiation hardened

The product, which is 8-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC}=2.7V-3.6V and V_{PP}=1.65V-3.6V or 11.7V-12.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states. Furthermore, its newly configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

* ETOX is a trademark of Intel Corporation.

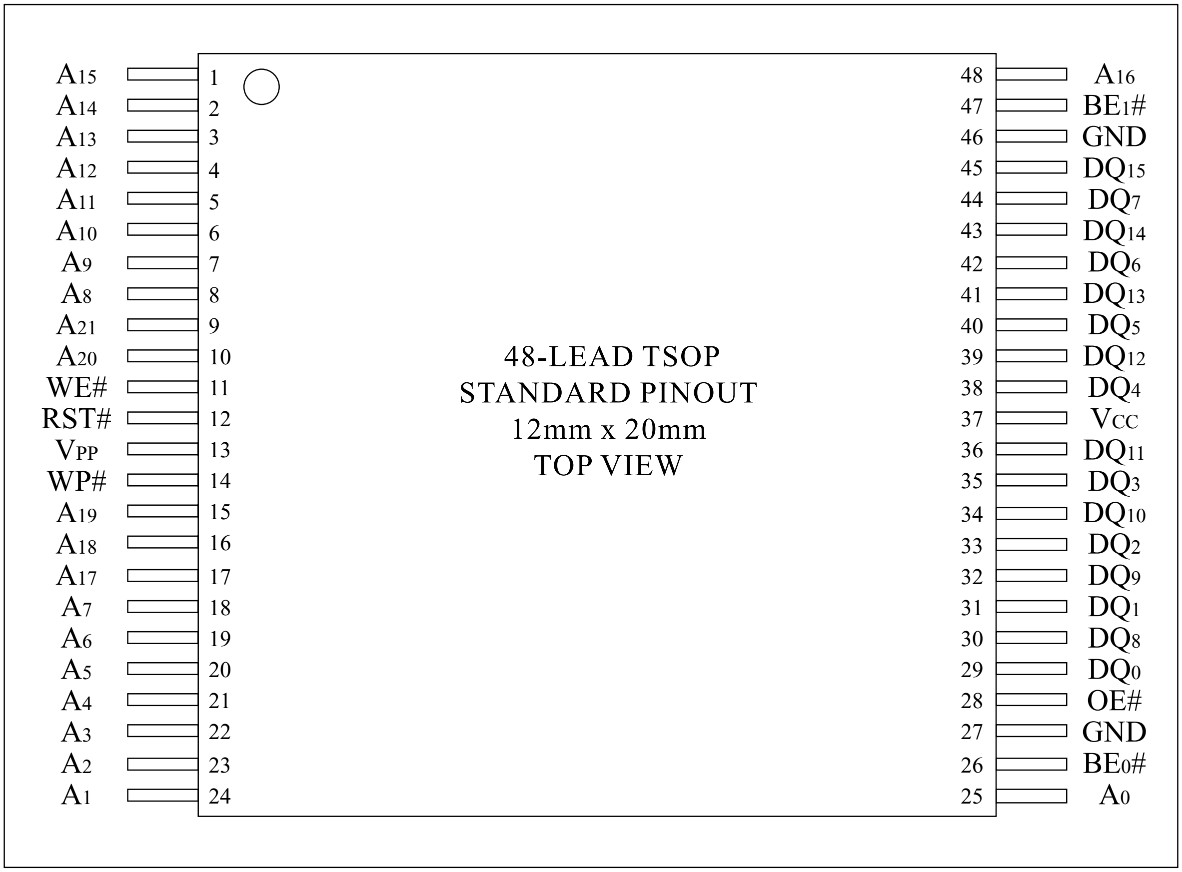


Figure 1. 48-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{21}	INPUT	ADDRESS INPUTS: Inputs for addresses. A_0-A_{21}
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code and partition configuration register code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
BE_0#, BE_1#	INPUT	BANK ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. BE_0#-high (V_{IH}) and BE_1#-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
RST#	INPUT	RESET: When low (V_{IL}), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of BE_0# or BE_1# or WE# (whichever goes high first).
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When WP# is V_{IH}, lock-down is disabled.
V_{PP}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, bank erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin. Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum. Use of this pin at 12V beyond these limits may reduce block cycling capability or cause permanent damage.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.

Table 2. Simultaneous Operation Modes Allowed with Eight Planes$^{(1, 2)}$

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Bank Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Bank Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

NOTES:

1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition. Only one partition can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.

Selected by BE$_0$#=V$_{IL}$ (Bank 0)

PLANE3 (PARAMETER PLANE)

BLOCK NUMBER		ADDRESS RANGE
134	4K-WORD	3FF000H - 3FFFFFH
133	4K-WORD	3FE000H - 3FEFFFH
132	4K-WORD	3FD000H - 3FDFFFH
131	4K-WORD	3FC000H - 3FCFFFH
130	4K-WORD	3FB000H - 3FBFFFH
129	4K-WORD	3FA000H - 3FAFFFH
128	4K-WORD	3F9000H - 3F9FFFH
127	4K-WORD	3F8000H - 3F8FFFH
126	32K-WORD	3F0000H - 3F7FFFH
125	32K-WORD	3E8000H - 3EFFFFH
124	32K-WORD	3E0000H - 3E7FFFH
123	32K-WORD	3D8000H - 3DFFFFH
122	32K-WORD	3D0000H - 3D7FFFH
121	32K-WORD	3C8000H - 3CFFFFH
120	32K-WORD	3C0000H - 3C7FFFH
119	32K-WORD	3B8000H - 3BFFFFH
118	32K-WORD	3B0000H - 3B7FFFH
117	32K-WORD	3A8000H - 3AFFFFH
116	32K-WORD	3A0000H - 3A7FFFH
115	32K-WORD	398000H - 39FFFFH
114	32K-WORD	390000H - 397FFFH
113	32K-WORD	388000H - 38FFFFH
112	32K-WORD	380000H - 387FFFH
111	32K-WORD	378000H - 37FFFFH
110	32K-WORD	370000H - 377FFFH
109	32K-WORD	368000H - 36FFFFH
108	32K-WORD	360000H - 367FFFH
107	32K-WORD	358000H - 35FFFFH
106	32K-WORD	350000H - 357FFFH
105	32K-WORD	348000H - 34FFFFH
104	32K-WORD	340000H - 347FFFH
103	32K-WORD	338000H - 33FFFFH
102	32K-WORD	330000H - 337FFFH
101	32K-WORD	328000H - 32FFFFH
100	32K-WORD	320000H - 327FFFH
99	32K-WORD	318000H - 31FFFFH
98	32K-WORD	310000H - 317FFFH
97	32K-WORD	308000H - 30FFFFH
96	32K-WORD	300000H - 307FFFH

PLANE2 (UNIFORM PLANE)

95	32K-WORD	2F8000H - 2FFFFFH
94	32K-WORD	2F0000H - 2F7FFFH
93	32K-WORD	2E8000H - 2EFFFFH
92	32K-WORD	2E0000H - 2E7FFFH
91	32K-WORD	2D8000H - 2DFFFFH
90	32K-WORD	2D0000H - 2D7FFFH
89	32K-WORD	2C8000H - 2CFFFFH
88	32K-WORD	2C0000H - 2C7FFFH
87	32K-WORD	2B8000H - 2BFFFFH
86	32K-WORD	2B0000H - 2B7FFFH
85	32K-WORD	2A8000H - 2AFFFFH
84	32K-WORD	2A0000H - 2A7FFFH
83	32K-WORD	298000H - 29FFFFH
82	32K-WORD	290000H - 297FFFH
81	32K-WORD	288000H - 28FFFFH
80	32K-WORD	280000H - 287FFFH
79	32K-WORD	278000H - 27FFFFH
78	32K-WORD	270000H - 277FFFH
77	32K-WORD	268000H - 26FFFFH
76	32K-WORD	260000H - 267FFFH
75	32K-WORD	258000H - 25FFFFH
74	32K-WORD	250000H - 257FFFH
73	32K-WORD	248000H - 24FFFFH
72	32K-WORD	240000H - 247FFFH
71	32K-WORD	238000H - 23FFFFH
70	32K-WORD	230000H - 237FFFH
69	32K-WORD	228000H - 22FFFFH
68	32K-WORD	220000H - 227FFFH
67	32K-WORD	218000H - 21FFFFH
66	32K-WORD	210000H - 217FFFH
65	32K-WORD	208000H - 20FFFFH
64	32K-WORD	200000H - 207FFFH

PLANE1 (UNIFORM PLANE)

BLOCK NUMBER		ADDRESS RANGE
63	32K-WORD	1F8000H - 1FFFFFH
62	32K-WORD	1F0000H - 1F7FFFH
61	32K-WORD	1E8000H - 1EFFFFH
60	32K-WORD	1E0000H - 1E7FFFH
59	32K-WORD	1D8000H - 1DFFFFH
58	32K-WORD	1D0000H - 1D7FFFH
57	32K-WORD	1C8000H - 1CFFFFH
56	32K-WORD	1C0000H - 1C7FFFH
55	32K-WORD	1B8000H - 1BFFFFH
54	32K-WORD	1B0000H - 1B7FFFH
53	32K-WORD	1A8000H - 1AFFFFH
52	32K-WORD	1A0000H - 1A7FFFH
51	32K-WORD	198000H - 19FFFFH
50	32K-WORD	190000H - 197FFFH
49	32K-WORD	188000H - 18FFFFH
48	32K-WORD	180000H - 187FFFH
47	32K-WORD	178000H - 17FFFFH
46	32K-WORD	170000H - 177FFFH
45	32K-WORD	168000H - 16FFFFH
44	32K-WORD	160000H - 167FFFH
43	32K-WORD	158000H - 15FFFFH
42	32K-WORD	150000H - 157FFFH
41	32K-WORD	148000H - 14FFFFH
40	32K-WORD	140000H - 147FFFH
39	32K-WORD	138000H - 13FFFFH
38	32K-WORD	130000H - 137FFFH
37	32K-WORD	128000H - 12FFFFH
36	32K-WORD	120000H - 127FFFH
35	32K-WORD	118000H - 11FFFFH
34	32K-WORD	110000H - 117FFFH
33	32K-WORD	108000H - 10FFFFH
32	32K-WORD	100000H - 107FFFH

PLANE0 (UNIFORM PLANE)

31	32K-WORD	0F8000H - 0FFFFFH
30	32K-WORD	0F0000H - 0F7FFFH
29	32K-WORD	0E8000H - 0EFFFFH
28	32K-WORD	0E0000H - 0E7FFFH
27	32K-WORD	0D8000H - 0DFFFFH
26	32K-WORD	0D0000H - 0D7FFFH
25	32K-WORD	0C8000H - 0CFFFFH
24	32K-WORD	0C0000H - 0C7FFFH
23	32K-WORD	0B8000H - 0BFFFFH
22	32K-WORD	0B0000H - 0B7FFFH
21	32K-WORD	0A8000H - 0AFFFFH
20	32K-WORD	0A0000H - 0A7FFFH
19	32K-WORD	098000H - 09FFFFH
18	32K-WORD	090000H - 097FFFH
17	32K-WORD	088000H - 08FFFFH
16	32K-WORD	080000H - 087FFFH
15	32K-WORD	078000H - 07FFFFH
14	32K-WORD	070000H - 077FFFH
13	32K-WORD	068000H - 06FFFFH
12	32K-WORD	060000H - 067FFFH
11	32K-WORD	058000H - 05FFFFH
10	32K-WORD	050000H - 057FFFH
9	32K-WORD	048000H - 04FFFFH
8	32K-WORD	040000H - 047FFFH
7	32K-WORD	038000H - 03FFFFH
6	32K-WORD	030000H - 037FFFH
5	32K-WORD	028000H - 02FFFFH
4	32K-WORD	020000H - 027FFFH
3	32K-WORD	018000H - 01FFFFH
2	32K-WORD	010000H - 017FFFH
1	32K-WORD	008000H - 00FFFFH
0	32K-WORD	000000H - 007FFFH

Figure 2.1. Memory Map (Top Parameter)

Selected by $BE_1\#=V_{IL}$ (Bank 1)

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (UNIFORM PLANE)	134	32K-WORD	3F8000H - 3FFFFFH
	133	32K-WORD	3F0000H - 3F7FFFH
	132	32K-WORD	3E8000H - 3EFFFFH
	131	32K-WORD	3E0000H - 3E7FFFH
	130	32K-WORD	3D8000H - 3DFFFFH
	129	32K-WORD	3D0000H - 3D7FFFH
	128	32K-WORD	3C8000H - 3CFFFFH
	127	32K-WORD	3C0000H - 3C7FFFH
	126	32K-WORD	3B8000H - 3BFFFFH
	125	32K-WORD	3B0000H - 3B7FFFH
	124	32K-WORD	3A8000H - 3AFFFFH
	123	32K-WORD	3A0000H - 3A7FFFH
	122	32K-WORD	398000H - 39FFFFH
	121	32K-WORD	390000H - 397FFFH
	120	32K-WORD	388000H - 38FFFFH
	119	32K-WORD	380000H - 387FFFH
	118	32K-WORD	378000H - 37FFFFH
	117	32K-WORD	370000H - 377FFFH
	116	32K-WORD	368000H - 36FFFFH
	115	32K-WORD	360000H - 367FFFH
	114	32K-WORD	358000H - 35FFFFH
	113	32K-WORD	350000H - 357FFFH
	112	32K-WORD	348000H - 34FFFFH
	111	32K-WORD	340000H - 347FFFH
	110	32K-WORD	338000H - 33FFFFH
	109	32K-WORD	330000H - 337FFFH
	108	32K-WORD	328000H - 32FFFFH
	107	32K-WORD	320000H - 327FFFH
	106	32K-WORD	318000H - 31FFFFH
	105	32K-WORD	310000H - 317FFFH
	104	32K-WORD	308000H - 30FFFFH
	103	32K-WORD	300000H - 307FFFH

PLANE2 (UNIFORM PLANE)	102	32K-WORD	2F8000H - 2FFFFFH
	101	32K-WORD	2F0000H - 2F7FFFH
	100	32K-WORD	2E8000H - 2EFFFFH
	99	32K-WORD	2E0000H - 2E7FFFH
	98	32K-WORD	2D8000H - 2DFFFFH
	97	32K-WORD	2D0000H - 2D7FFFH
	96	32K-WORD	2C8000H - 2CFFFFH
	95	32K-WORD	2C0000H - 2C7FFFH
	94	32K-WORD	2B8000H - 2BFFFFH
	93	32K-WORD	2B0000H - 2B7FFFH
	92	32K-WORD	2A8000H - 2AFFFFH
	91	32K-WORD	2A0000H - 2A7FFFH
	90	32K-WORD	298000H - 29FFFFH
	89	32K-WORD	290000H - 297FFFH
	88	32K-WORD	288000H - 28FFFFH
	87	32K-WORD	280000H - 287FFFH
	86	32K-WORD	278000H - 27FFFFH
	85	32K-WORD	270000H - 277FFFH
	84	32K-WORD	268000H - 26FFFFH
	83	32K-WORD	260000H - 267FFFH
	82	32K-WORD	258000H - 25FFFFH
	81	32K-WORD	250000H - 257FFFH
	80	32K-WORD	248000H - 24FFFFH
	79	32K-WORD	240000H - 247FFFH
	78	32K-WORD	238000H - 23FFFFH
	77	32K-WORD	230000H - 237FFFH
	76	32K-WORD	228000H - 22FFFFH
	75	32K-WORD	220000H - 227FFFH
	74	32K-WORD	218000H - 21FFFFH
	73	32K-WORD	210000H - 217FFFH
	72	32K-WORD	208000H - 20FFFFH
	71	32K-WORD	200000H - 207FFFH

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH
	58	32K-WORD	198000H - 19FFFFH
	57	32K-WORD	190000H - 197FFFH
	56	32K-WORD	188000H - 18FFFFH
	55	32K-WORD	180000H - 187FFFH
	54	32K-WORD	178000H - 17FFFFH
	53	32K-WORD	170000H - 177FFFH
	52	32K-WORD	168000H - 16FFFFH
	51	32K-WORD	160000H - 167FFFH
	50	32K-WORD	158000H - 15FFFFH
	49	32K-WORD	150000H - 157FFFH
	48	32K-WORD	148000H - 14FFFFH
	47	32K-WORD	140000H - 147FFFH
	46	32K-WORD	138000H - 13FFFFH
	45	32K-WORD	130000H - 137FFFH
	44	32K-WORD	128000H - 12FFFFH
	43	32K-WORD	120000H - 127FFFH
	42	32K-WORD	118000H - 11FFFFH
	41	32K-WORD	110000H - 117FFFH
	40	32K-WORD	108000H - 10FFFFH
	39	32K-WORD	100000H - 107FFFH

PLANE0 (PARAMETER PLANE)	38	32K-WORD	0F8000H - 0FFFFFH
	37	32K-WORD	0F0000H - 0F7FFFH
	36	32K-WORD	0E8000H - 0EFFFFH
	35	32K-WORD	0E0000H - 0E7FFFH
	34	32K-WORD	0D8000H - 0DFFFFH
	33	32K-WORD	0D0000H - 0D7FFFH
	32	32K-WORD	0C8000H - 0CFFFFH
	31	32K-WORD	0C0000H - 0C7FFFH
	30	32K-WORD	0B8000H - 0BFFFFH
	29	32K-WORD	0B0000H - 0B7FFFH
	28	32K-WORD	0A8000H - 0AFFFFH
	27	32K-WORD	0A0000H - 0A7FFFH
	26	32K-WORD	098000H - 09FFFFH
	25	32K-WORD	090000H - 097FFFH
	24	32K-WORD	088000H - 08FFFFH
	23	32K-WORD	080000H - 087FFFH
	22	32K-WORD	078000H - 07FFFFH
	21	32K-WORD	070000H - 077FFFH
	20	32K-WORD	068000H - 06FFFFH
	19	32K-WORD	060000H - 067FFFH
	18	32K-WORD	058000H - 05FFFFH
	17	32K-WORD	050000H - 057FFFH
	16	32K-WORD	048000H - 04FFFFH
	15	32K-WORD	040000H - 047FFFH
	14	32K-WORD	038000H - 03FFFFH
	13	32K-WORD	030000H - 037FFFH
	12	32K-WORD	028000H - 02FFFFH
	11	32K-WORD	020000H - 027FFFH
	10	32K-WORD	018000H - 01FFFFH
	9	32K-WORD	010000H - 017FFFH
	8	32K-WORD	008000H - 00FFFFH
	7	4K-WORD	007000H - 007FFFH
	6	4K-WORD	006000H - 006FFFH
	5	4K-WORD	005000H - 005FFFH
	4	4K-WORD	004000H - 004FFFH
	3	4K-WORD	003000H - 003FFFH
	2	4K-WORD	002000H - 002FFFH
	1	4K-WORD	001000H - 001FFFH
	0	4K-WORD	000000H - 000FFFH

Figure 2.2. Memory Map (Bottom Parameter)

Table 3. Identifier Codes and OTP Address for Read Operation

	Code	Address $[A_{15}\text{-}A_0]^{(1)}$	Data $[DQ_{15}\text{-}DQ_0]$	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	
Device Code	Device Code	0001H	00B0H (BE_0#=V_{IL})	2
			00B1H (BE_1#=V_{IL})	
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	$DQ_0 = 0$	3
	Block is Locked		$DQ_0 = 1$	3
	Block is not Locked-Down		$DQ_1 = 0$	3
	Block is Locked-Down		$DQ_1 = 1$	3
Device Configuration Code	Partition Configuration Register	0006H	PCRC	4
OTP	OTP Lock	0080H	OTP-LK	5, 7
	OTP	0081-0088H	OTP	6, 7

NOTES:
1. The address A_{21}-A_{16} are shown in below table for reading the manufacturer, device, lock configuration, device configuration code and OTP data.
2. Bank 0 (selected by BE_0#=V_{IL}) has its parameter blocks in the plane3 (The highest address within the bank). Bank 1 (selected by BE_1#=V_{IL}) has its parameter blocks in the plane0 (The lowest address within the bank).
3. DQ_{15}-DQ_2 are reserved for future implementation.
4. PCRC=Partition Configuration Register Code.
5. OTP-LK=OTP Block Lock configuration.
6. OTP=OTP Block data.
7. When the data within OTP block is read, BE_0# must be V_{IL}.
   OTP block in Bank 1 (selected by BE_1#=V_{IL}) should not be used.

Table 4. Identifier Codes and OTP Address for Read Operation on Partition Configuration$^{(1)}$

Partition Configuration Register $^{(2)}$			Address$^{(3)}$
PCR.10	PCR.9	PCR.8	$[A_{21}\text{-}A_{16}]$
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

NOTES:
1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
2. Refer to Table 12 for the partition configuration register.
3. When the data within OTP block is read, BE_0# must be V_{IL}.
   OTP block in Bank 1 (selected by BE_1#=V_{IL}) should not be used.

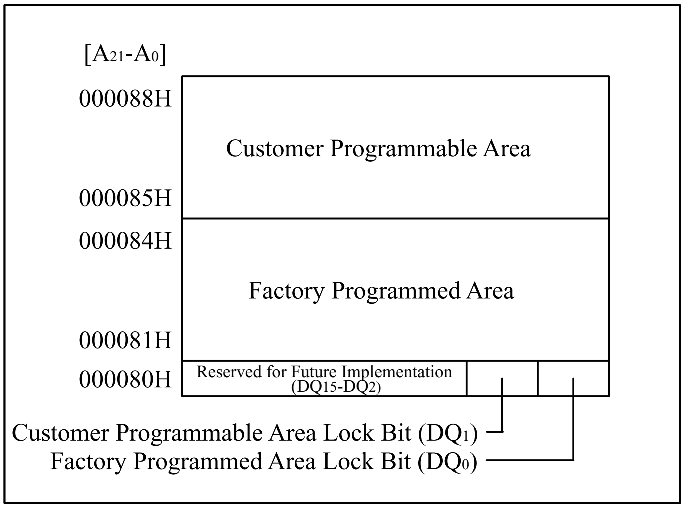


Figure 3. OTP Block Address Map for OTP Program(1)
(The area outside 80H~88H cannot be used.)

NOTE:

1. When the OTP program operation is executed, write the OTP Program command with BE_0# at V_{IL}. OTP block in Bank 1 (selected by BE_1#=V_{IL}) should not be used.

Table 5. Bus Operation(1, 2)

Mode		Notes	RST#	BE_0#	BE_1#	OE#	WE#	Address	V_{PP}	DQ_{0-15}
Read Array	Bank 0	6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	D_{OUT}
	Bank 1			V_{IH}	V_{IL}					
	Inhibited			V_{IL}	V_{IL}					N/A
Output Disable			V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z
Standby	Bank 0		V_{IH}	V_{IH}	V_{IL}	X	X	X	X	High Z
	Bank 1			V_{IL}	V_{IH}					
	Bank 0, 1			V_{IH}	V_{IH}					
Reset		3	V_{IL}	X	X	X	X	X	X	High Z
Read Identifier Codes/OTP	Bank 0	6,9	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	See Table 3 and Table 4	X	See Table 3 and Table 4
	Bank 1			V_{IH}	V_{IL}					
	Inhibited			V_{IL}	V_{IL}					N/A
Read Query	Bank 0	6,7	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	See Appendix	X	See Appendix
	Bank 1			V_{IH}	V_{IL}					
	Inhibited			V_{IL}	V_{IL}					N/A
Write	Bank 0	4,5, 6,8	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	D_{IN}
	Bank 1			V_{IH}	V_{IL}					
	Inhibited			V_{IL}	V_{IL}					N/A

NOTES:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, (page buffer) program or OTP program are reliably executed when $V_{PP}=V_{PPH1/2}$ and V_{CC}=2.7V-3.6V.
   Command writes involving bank erase are reliably executed when $V_{PP}=V_{PPH1}$ and V_{CC}=2.7V-3.6V.
5. Refer to Table 6 for valid D_{IN} during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Appendix of LH28F128BF series for more information about query code.
8. While the erase or program operation is executed in one bank, it is inhibited to execute the erase or program operation in another bank.
9. When the data within OTP block is read, BE_0# must be V_{IL}.
   OTP block in Bank 1 (selected by BE_1#=V_{IL}) should not be used.

Table 6. Command Definitions[12]

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[1]	Addr[2]	Data[3]	Oper[1]	Addr[2]	Data[3]
Read Array	1	2	Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	2,3,4,11	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	2,3,4	Write	PA	98H	Read	QA	QD
Read Status Register	2	2,3	Write	PA	70H	Read	PA	SRD
Clear Status Register	1	2	Write	PA	50H			
Block Erase	2	2,3,5	Write	BA	20H	Write	BA	D0H
Bank Erase	2	2,5,9	Write	X	30H	Write	X	D0H
Program	2	2,3,5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	2,3,5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	2,8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	2,8,9	Write	PA	D0H			
Set Block Lock Bit	2	2	Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	2,10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2	2	Write	BA	60H	Write	BA	2FH
OTP Program	2	2,3,9,11	Write	OA	C0H	Write	OA	OD
Set Partition Configuration Register	2	2,3	Write	PCRC	60H	Write	PCRC	04H

NOTES:

1. Bus operations are defined in Table 5.
2. The address which is written at the first bus cycle should be the same as the address which is written at the second bus cycle.
   X=Any valid address. Bank erase is executed to the bank selected by BE_0# or BE_1#.
   PA=Address within the selected partition.
   IA=Identifier codes address (See Table 3 and Table 4).
   QA=Query codes address. Refer to Appendix of LH28F128BF series for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See Figure 3).
   PCRC=Partition configuration register code presented on the address A_0-A_{15}.
3. ID=Data read from identifier codes. (See Table 3 and Table 4).
   QD=Data read from query database. Refer to Appendix of LH28F128BF series for details.
   SRD=Data read from status register. See Table 10 and Table 11 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or BE_0# or BE_1# (whichever goes high first).
   OD=Data to be programmed at location OA. Data is latched on the rising edge of WE# or BE_0# or BE_1# (whichever goes high first).
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 3 and Table 4).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, bank erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target partition to be programmed and the confirm command (D0H). Refer to Appendix of

LH28F128BF series for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Bank erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is V_{IL}. When WP# is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. When the data within OTP block is read, BE_0# must be V_{IL}. When the OTP program operation is executed, write the OTP Program command with BE_0# at V_{IL}. OTP block in Bank 1 (selected by BE_1#=V_{IL}) should not be used.
12. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 7. Functions of Block Lock(5) and Block Lock-Down

Current State					Erase/Program Allowed (2)
State	WP#	DQ_1(1)	DQ_0(1)	State Name	
[000]	0	0	0	Unlocked	Yes
[001](3)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101](3)	1	0	1	Locked	No
[110](4)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

NOTES:

1. DQ_0=1: a block is locked; DQ_0=0: a block is unlocked.
   DQ_1=1: a block is locked-down; DQ_1=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, bank erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation.
4. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function which is different from those described above.

Table 8. Block Locking State Transitions upon Command Write(4)

Current State				Result after Lock Command Written (Next State)		
State	WP#	DQ_1	DQ_0	Set Lock(1)	Clear Lock(1)	Set Lock-down(1)
[000]	0	0	0	[001]	No Change	[011](2)
[001]	0	0	1	No Change(3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111](2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111](2)
[111]	1	1	1	No Change	[110]	No Change

NOTES:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that WP# is not changed and fixed V_{IL} or V_{IH}.

Table 9. Block Locking State Transitions upon WP# Transition(4)

Previous State	Current State				Result after WP# Transition (Next State)	
	State	WP#	DQ_1	DQ_0	WP#=0→1(1)	WP#=1→0(1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110](2)	[011]	0	1	1	[110]	-
Other than [110](2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011](3)
-	[111]	1	1	1	-	[011]

NOTES:

1. "WP#=0→1" means that WP# is driven to V_{IH} and "WP#=1→0" means that WP# is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

Table 10. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	Check SR.7 to determine block erase, bank erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".
SR.5 = BLOCK ERASE AND BANK ERASE STATUS (BEFCES) 1 = Error in Block Erase or Bank Erase 0 = Successful Block Erase or Bank Erase	If both SR.5 and SR.4 are "1"s after a block erase, bank erase, page buffer program, set/clear block lock bit, set block lock-down bit, set partition configuration register attempt, an improper command sequence was entered.
SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS) 1 = Error in (Page Buffer) Program or OTP Program 0 = Successful (Page Buffer) Program or OTP Program	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Bank Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1}$, V_{PPH2} or V_{PPLK}.
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} LOW Detect, Operation Abort 0 = V_{PP} OK	SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Bank Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.
SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed	SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked	
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	

Table 11. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R) XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not. XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Table 12. Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)
- 000 = No partitioning. Dual Work is not allowed.
- 001 = Plane1-3 are merged into one partition. (default in Bank 1 selected by BE$_1$#=V$_{IL}$)
- 010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.
- 100 = Plane 0-2 are merged into one partition. (default in Bank 0 selected by BE$_0$#=V$_{IL}$)
- 011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in Bank 1 and "100" in Bank 0.

See Figure 4 for the detail on partition configuration.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when polling the partition configuration register.

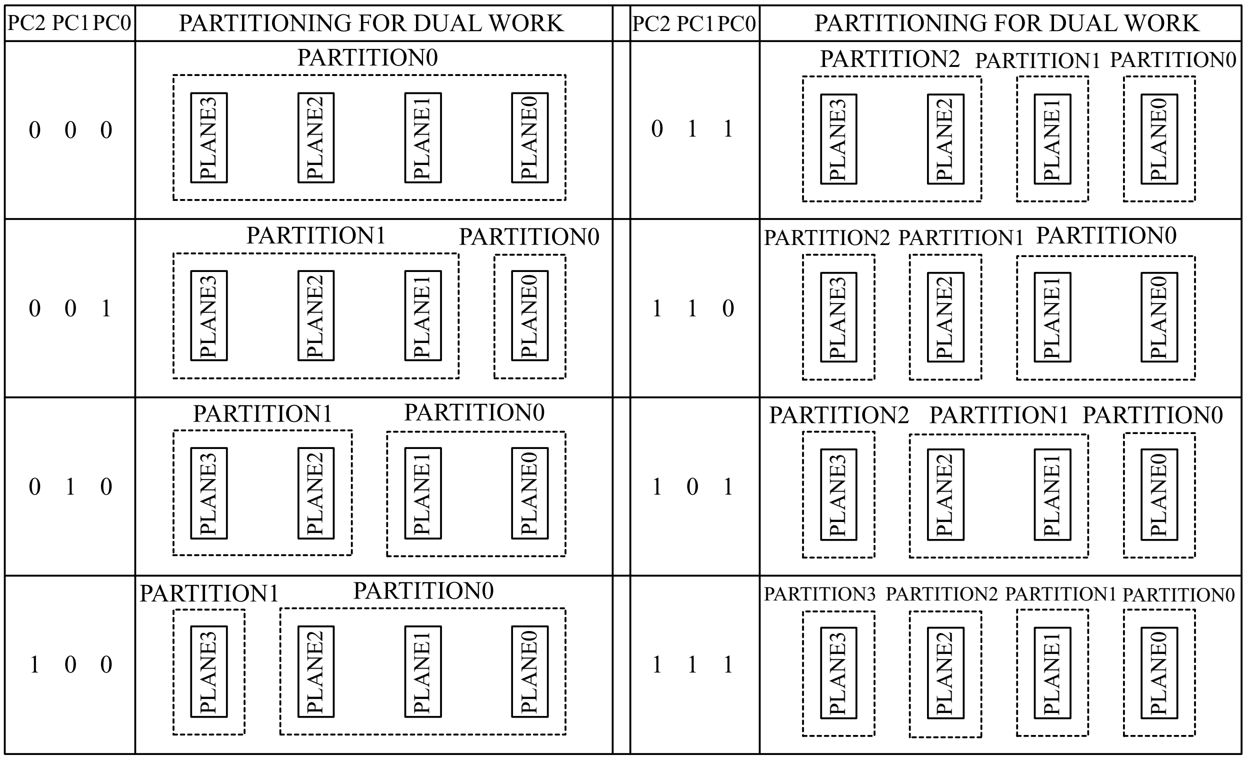


Figure 4. Partition Configuration

1 Electrical Specifications

1.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ...-40°C to +85°C (1)

Storage Temperature

During under Bias............................... -40°C to +85°C

During non Bias................................ -65°C to +125°C

Voltage On Any Pin

(except V_{CC} and V_{PP})............. -0.5V to V_{CC}+0.5V (2)

V_{CC} Supply Voltage .... -0.2V to +3.9V (2)

V_{PP} Supply Voltage .... -0.2V to 12.6V (2, 3, 4)

Output Short Circuit Current...........................100mA (5)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20ns.
3. Maximum DC voltage on V_{PP} may overshoot to +13.0V for periods <20ns.
4. V_{PP} erase/program voltage is normally 2.7V-3.6V. Applying 11.7V-12.3V to V_{PP} during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. V_{PP} may be connected to 11.7V-12.3V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	-40	+25	+85	°C	
V_{CC} Supply Voltage	V_{CC}	2.7	3.0	3.6	V	1
V_{PP} Voltage when Used as a Logic Control	V_{PPH1}	1.65	3.0	3.6	V	1
V_{PP} Supply Voltage	V_{PPH2}	11.7	12	12.3	V	1, 2
Main Block Erase Cycling: V_{PP}=3.0V		100,000			Cycles	
Parameter Block Erase Cycling: V_{PP}=3.0V		100,000			Cycles	
Main Block Erase Cycling: V_{PP}=12V, 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: V_{PP}=12V, 80 hrs.				1,000	Cycles	
Maximum V_{PP} hours at 12V				80	Hours	

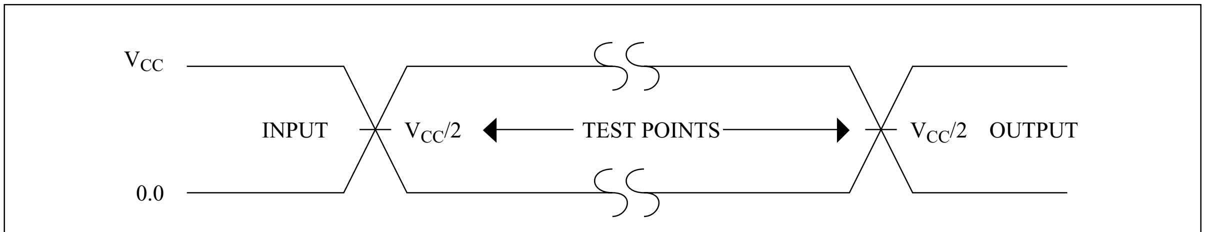
NOTES:
1. See DC Characteristics tables for voltage range-specific specification.
2. Applying V_{PP}=11.7V-12.3V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to V_{PP}=11.7V-12.3V is not allowed and can cause damage to the device.

1.2.1 Capacitance[1] (T_A=+25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0.0V		12	16	pF
Output Capacitance	C_{OUT}	V_{OUT}=0.0V		20	24	pF

NOTE:
1. Sampled, not 100% tested.

1.2.2 AC Input/Output Test Conditions



AC test inputs are driven at V_{CC}(min) for a Logic "1" and 0.0V for a Logic "0".
Input timing begins, and output timing ends at $V_{CC}/2$. Input rise and fall times (10% to 90%) < 5ns.
Worst case speed conditions are when $V_{CC}=V_{CC}$(min).

Figure 5. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

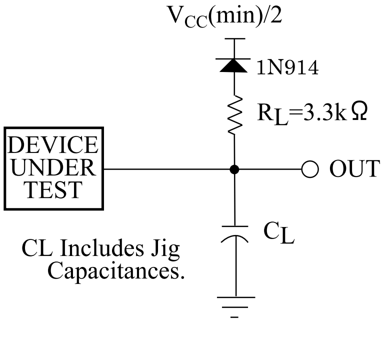


Figure 6. Transient Equivalent Testing Load Circuit

Table 13. Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=2.7V-3.6V	50

1.2.3 DC Characteristics

V_{CC}=2.7V-3.6V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current	1	-2.0		+2.0	µA	V_{CC}=V_{CC}Max., V_{IN}/V_{OUT}=V_{CC} or GND
I_{LO}	Output Leakage Current	1	-2.0		+2.0	µA	
I_{CCS}	V_{CC} Standby Current	1		8	40	µA	V_{CC}=V_{CC}Max., BE_0#=BE_1#=RST#= V_{CC}±0.2V, WP#=V_{CC} or GND
I_{CCAS}	V_{CC} Automatic Power Savings Current	1,4		8	40	µA	V_{CC}=V_{CC}Max., BE_0# or BE_1#= GND±0.2V, WP#=V_{CC} or GND
I_{CCD}	V_{CC} Reset Power-Down Current	1		8	40	µA	RST#=GND±0.2V
I_{CCR}	Average V_{CC} Read Current Normal Mode	1,7		15	25	mA	V_{CC}=V_{CC}Max., BE_0# or BE_1#=V_{IL}, OE#=V_{IH}, f=5MHz
	Average V_{CC} Read Current Page Mode 8 Word Read	1,7		5	10	mA	
I_{CCW}	V_{CC} (Page Buffer) Program Current	1,5,7		20	60	mA	V_{PP}=V_{PPH1}
		1,5,7		10	20	mA	V_{PP}=V_{PPH2}
I_{CCE}	V_{CC} Block Erase, Bank Erase Current	1,5,7		10	30	mA	V_{PP}=V_{PPH1}
		1,5,7		10	30	mA	V_{PP}=V_{PPH2}
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current	1,2,7		10	200	µA	BE_0#=BE_1#=V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	1,6,7		4	10	µA	V_{PP}≤V_{CC}
I_{PPW}	V_{PP} (Page Buffer) Program Current	1,5,6,7		2	5	µA	V_{PP}=V_{PPH1}
		1,5,6,7		10	30	mA	V_{PP}=V_{PPH2}
I_{PPE}	V_{PP} Block Erase, Bank Erase Current	1,5,6,7		2	5	µA	V_{PP}=V_{PPH1}
		1,5,6,7		5	15	mA	V_{PP}=V_{PPH2}
I_{PPWS}	V_{PP} (Page Buffer) Program Suspend Current	1,6,7		2	5	µA	V_{PP}=V_{PPH1}
		1,6,7		10	200	µA	V_{PP}=V_{PPH2}
I_{PPES}	V_{PP} Block Erase Suspend Current	1,6,7		2	5	µA	V_{PP}=V_{PPH1}
		1,6,7		10	200	µA	V_{PP}=V_{PPH2}

DC Characteristics (Continued)

V_{CC}=2.7V-3.6V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	5	-0.4		0.4	V	
V_{IH}	Input High Voltage	5	V_{CC} -0.4		V_{CC} + 0.4	V	
V_{OL}	Output Low Voltage	5			0.2	V	V_{CC}=V_{CC}Min., I_{OL}=100µA
V_{OH}	Output High Voltage	5	V_{CC} -0.2			V	V_{CC}=V_{CC}Min., I_{OH}=-100µA
V_{PPLK}	V_{PP} Lockout during Normal Operations	3,5,6			0.4	V	
V_{PPH1}	V_{PP} during Block Erase, Bank Erase, (Page Buffer) Program or OTP Program Operations	6	1.65	3.0	3.6	V	
V_{PPH2}	V_{PP} during Block Erase, (Page Buffer) Program or OTP Program Operations	6	11.7	12	12.3	V	
V_{LKO}	V_{CC} Lockout Voltage		1.5			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC}=3.0V and T_A=+25°C unless V_{CC} is specified.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program while in block erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Block erase, bank erase, (page buffer) program and OTP program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max.) and V_{PPH1}(min.), between V_{PPH1}(max.) and V_{PPH2}(min.) and above V_{PPH2}(max.).
4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
5. Sampled, not 100% tested.
6. V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, bank erase, (page buffer) program and OTP program cannot be executed and should not be attempted.
   Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{CC} power bus.
   Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum.
7. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.

1.2.4 AC Characteristics - Read-Only Operations(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		90		ns
t_{AVQV}	Address to Output Delay			90	ns
t_{ELQV}	BE_0# or BE_1# to Output Delay	3		90	ns
t_{APA}	Page Address Access Time			35	ns
t_{GLQV}	OE# to Output Delay	3		20	ns
t_{PHQV}	RST# High to Output Delay			150	ns
t_{EHQZ}, t_{GHQZ}	BE_0# or BE_1# or OE# to Output in High Z, Whichever Occurs First	2		20	ns
t_{ELQX}	BE_0# or BE_1# to Output in Low Z	2	0		ns
t_{GLQX}	OE# to Output in Low Z	2	0		ns
t_{OH}	Output Hold from First Occurring Address, BE_0# or BE_1# or OE# change	2	0		ns

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to t_{ELQV} — t_{GLQV} after the falling edge of BE_0# or BE_1# without impact to t_{ELQV}.

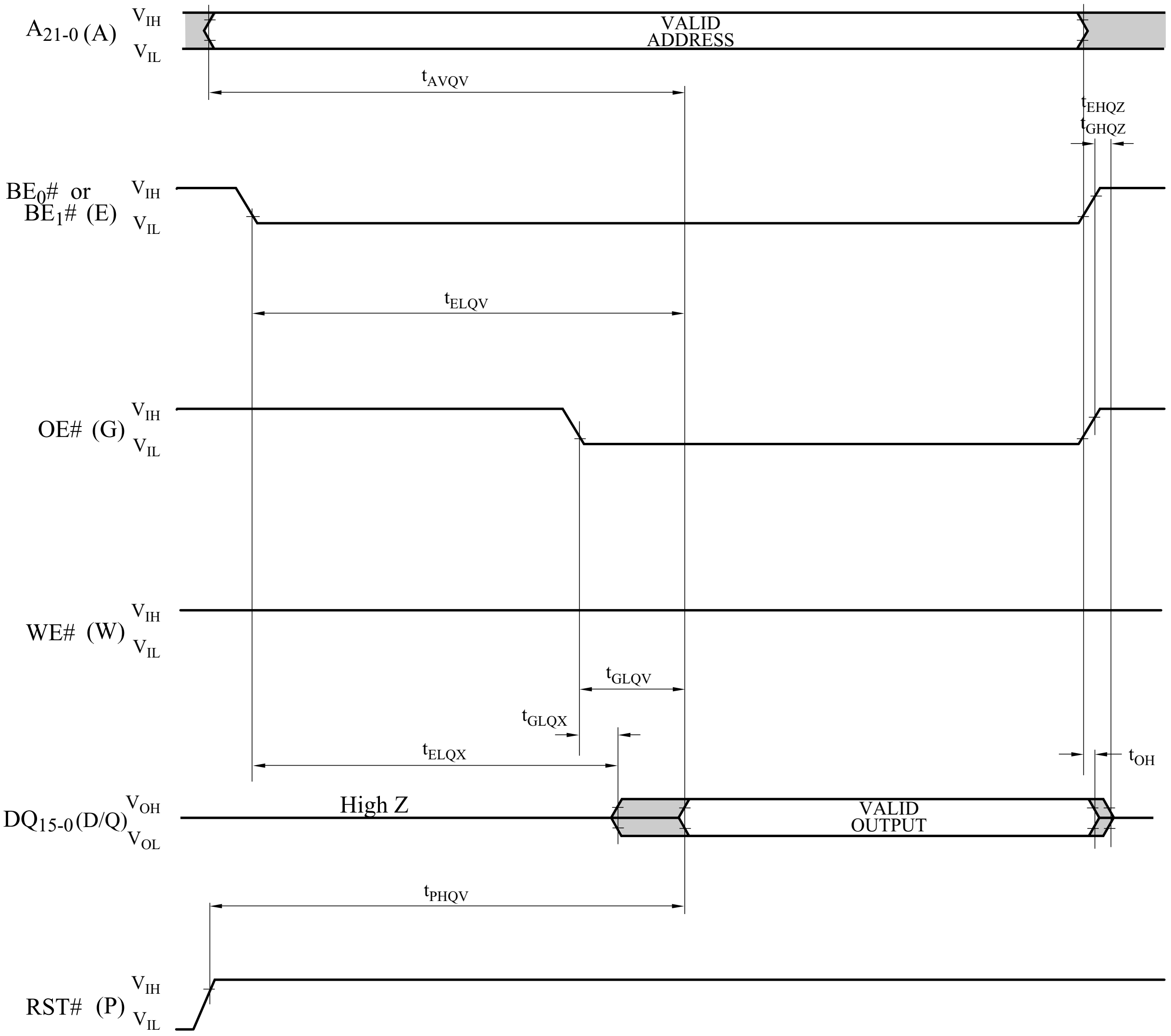


Figure 7. AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code

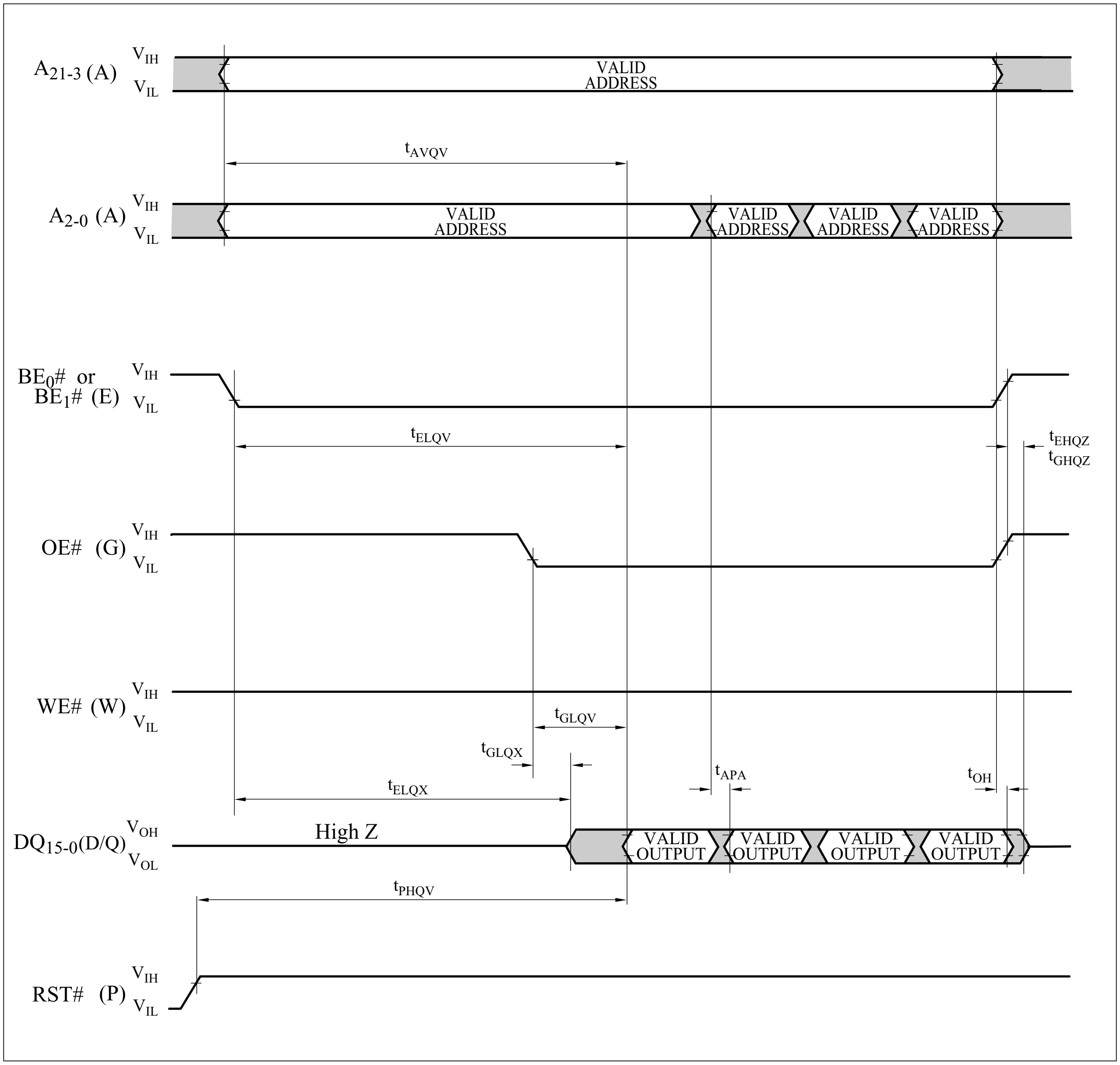


Figure 8. AC Waveform for Asynchronous Page Mode Read Operations from Main Blocks or Parameter Blocks

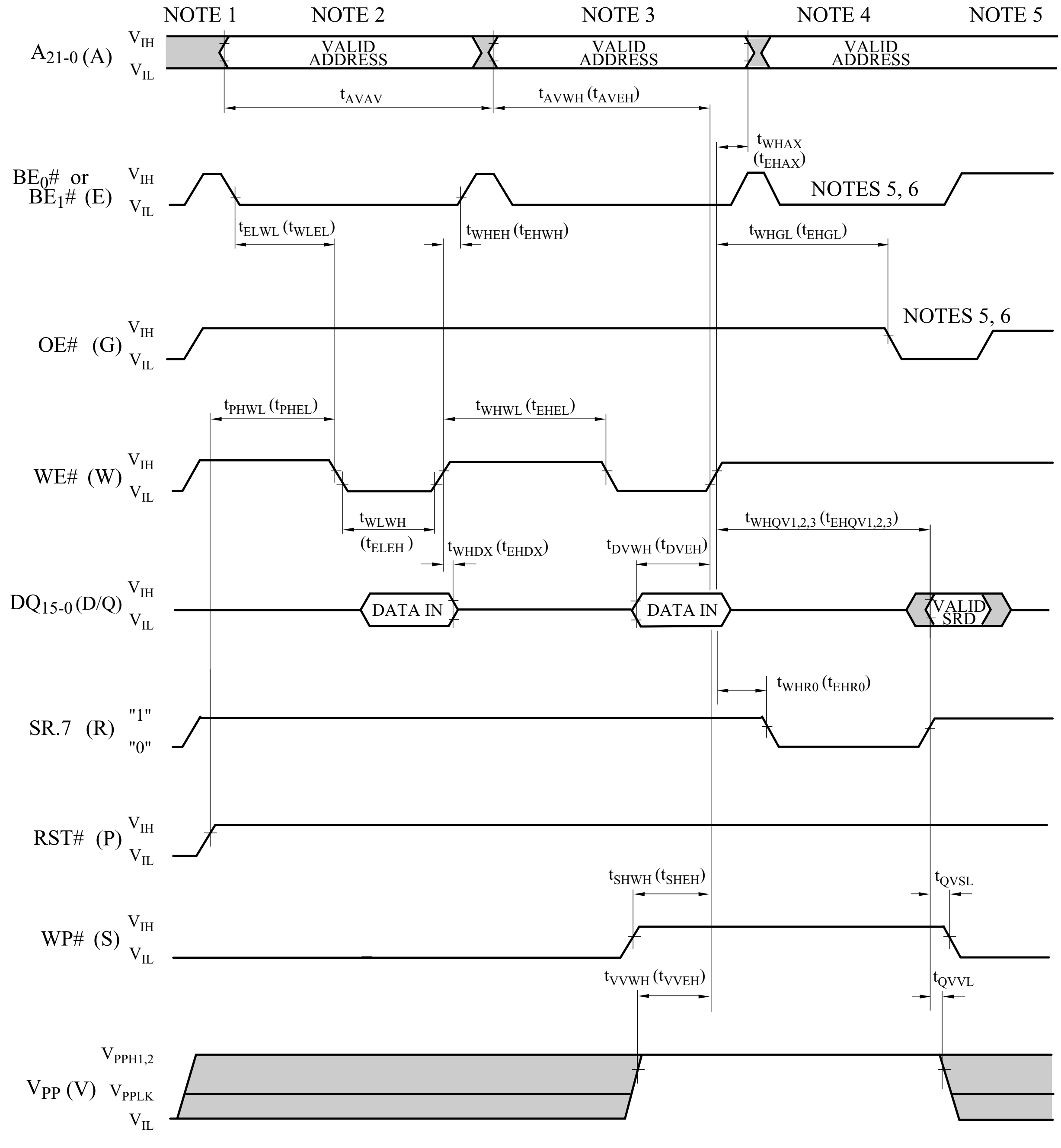
1.2.5 AC Characteristics - Write Operations(1), (2)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (BE_0# or BE_1#) Going Low	3	150		ns
t_{ELWL} (t_{WLEL})	BE_0# or BE_1# (WE#) Setup to WE# (BE_0# or BE_1#) Going Low	4	0		ns
t_{WLWH} (t_{ELEH})	WE# (BE_0# or BE_1#) Pulse Width	4	60		ns
t_{DVWH} (t_{DVEH})	Data Setup to WE# (BE_0# or BE_1#) Going High	8	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to WE# (BE_0# or BE_1#) Going High	8	50		ns
t_{WHEH} (t_{EHWH})	BE_0# or BE_1# (WE#) Hold from WE# (BE_0# or BE_1#) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from WE# (BE_0# or BE_1#) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from WE# (BE_0# or BE_1#) High		0		ns
t_{WHWL} (t_{EHEL})	WE# (BE_0# or BE_1#) Pulse Width High	5	30		ns
t_{SHWH} (t_{SHEH})	WP# High Setup to WE# (BE_0# or BE_1#) Going High	3	0		ns
t_{VVWH} (t_{VVEH})	V_{PP} Setup to WE# (BE_0# or BE_1#) Going High	3	200		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		30		ns
t_{QVSL}	WP# High Hold from Valid SRD	3, 6	0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD	3, 6	0		ns
t_{WHR0} (t_{EHR0})	WE# (BE_0# or BE_1#) High to SR.7 Going "0"	3, 7		t_{AVQV}+ 50	ns

NOTES:

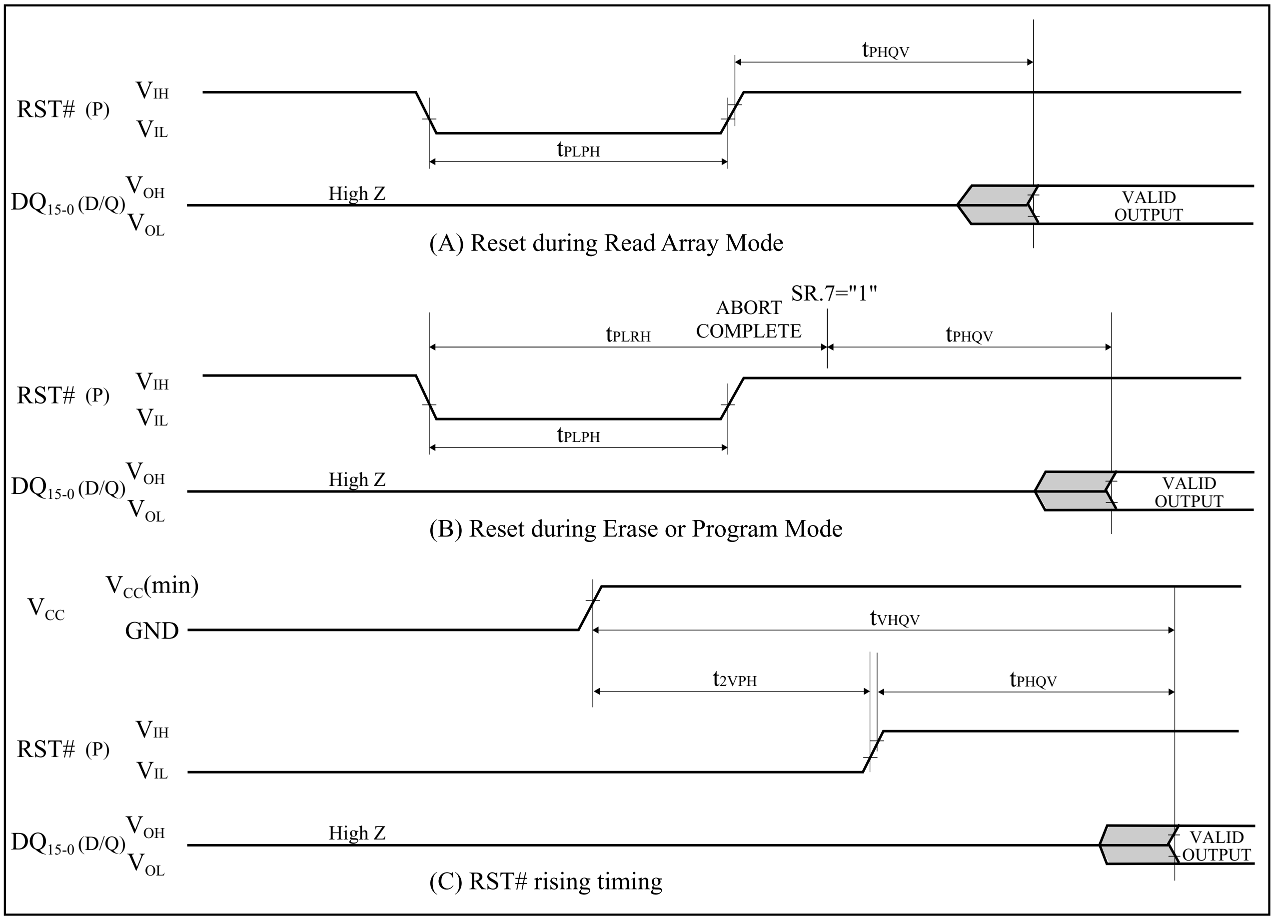
1. The timing characteristics for reading the status register during block erase, bank erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either BE_0# or BE_1# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of BE_0# or BE_1# or WE# (whichever goes low last) to the rising edge of BE_0# or BE_1# or WE# (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of BE_0# or BE_1# or WE# (whichever goes high first) to the falling edge of BE_0# or BE_1# or WE# (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. V_{PP} should be held at $V_{PP}=V_{PPH1/2}$ until determination of block erase, (page buffer) program or OTP program success (SR.1/3/4/5=0) and held at $V_{PP}=V_{PPH1}$ until determination of bank erase success (SR.1/3/5=0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command=t_{AVQV}+100ns.
8. Refer to Table 6 for valid address and data for block erase, bank erase, (page buffer) program, OTP program or lock bit configuration.



NOTES:
1. V_{CC} power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, OE# and BE_0# or BE_1# must be driven active, and WE# de-asserted.

Figure 9. AC Waveform for Write Operations

1.2.6 Reset Operations



(A) Reset during Read Array Mode

(B) Reset during Erase or Program Mode

(C) RST# rising timing

Figure 10. AC Waveform for Reset Operations

Reset AC Specifications (V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RST# Low to Reset during Read (RST# should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	RST# Low to Reset during Erase or Program	1, 3, 4		22	µs
t_{2VPH}	V_{CC} 2.7V to RST# High	1, 3, 5	100		ns
t_{VHQV}	V_{CC} 2.7V to Output Delay	3		1	ms

NOTES:

1. A reset time, t_{PHQV}, is required from the later of SR.7 going "1" or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RST# asserted while a block erase, bank erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RST# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

1.2.7 Block Erase, Bank Erase, (Page Buffer) Program and OTP Program Performance(3)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	$V_{PP}=V_{PPH1}$ (In System)			$V_{PP}=V_{PPH2}$ (In Manufacturing)			Unit
				Min.	Typ.(1)	Max.(2)	Min.	Typ.(1)	Max.(2)	
t_{WPB}	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3		0.04	0.12	s
		2	Used		0.03	0.12		0.02	0.06	s
t_{WMB}	32K-Word Main Block Program Time	2	Not Used		0.38	2.4		0.31	1.0	s
		2	Used		0.24	1.0		0.17	0.5	s
t_{WHQV1}/ t_{EHQV1}	Word Program Time	2	Not Used		11	200		9	185	µs
		2	Used		7	100		5	90	µs
t_{WHOV1}/ t_{EHOV1}	OTP Program Time	2, 6	Not Used		36	400		27	185	µs
t_{WHQV2}/ t_{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4		0.2	4	s
t_{WHQV3}/ t_{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5		0.5	5	s
	Bank Erase Time	2			80	700				s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10		5	10	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20		5	20	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			µs

NOTES:
1. Typical values measured at V_{CC}=3.0V, V_{PP}=3.0V or 12V, and T_A=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (WE# or BE_0# or BE_1# going high) until SR.7 going "1".
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.
6. When the OTP program operation is executed, write the OTP Program command with BE_0# at V_{IL}. OTP block in Bank 1 (selected by BE_1#=V_{IL}) should not be used.

2 Related Document Information[1]

Document No.	Document Name
FUM00701	LH28F128BF series Appendix

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.

3 Package and packing specification

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80% R.H. max.

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1, or Manual soldering.)

- Temperature : 5～25℃
- Humidity : 60% R.H. max.
- Period : 96 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃。
- Humidity : 60% R.H. max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃。
- Humidity : 60% R.H. max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

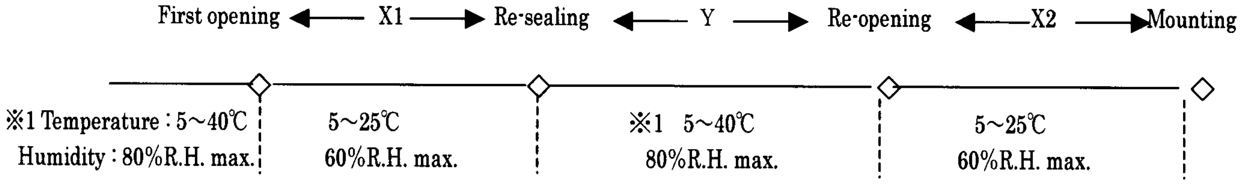
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1+X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened. (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period :
  120℃ for 16~24 hours.
- The above baking conditions apply since the trays are heat-resistant.

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

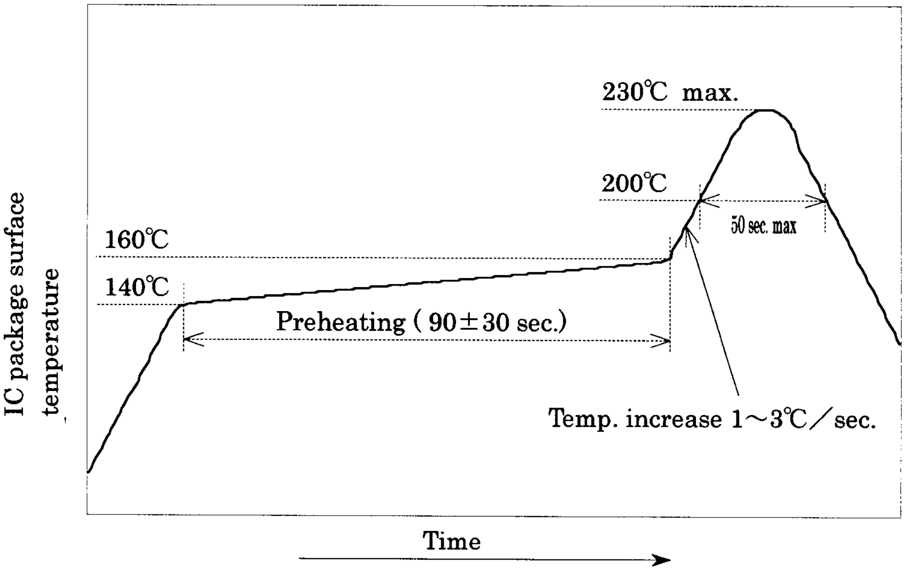
3.Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1.Soldering.

(1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
  Peak temperature of 230℃ max.
  Above 200℃ for 50 sec. max.
  Preheat temperature of 140~160℃ for 90±30 sec.
  Temperature increase rate of 1~3℃/sec.
- Measuring point : IC package surface.
- Temperature profile :



(2) Manual soldering (soldering iron) (one-time soldering only)

Soldering iron should only touch the IC's outer leads.

- Temperature and period :
  350℃ max. for 3 sec. / pin max., or 260℃ max. for 10 sec. / pin max.
  (Soldering iron should only touch the IC's outer leads.)
- Measuring point : Soldering iron tip.

4. Condition for removal of residual flax.

(1) Ultrasonic washing power : 25 watts / liter max.
(2) Washing time : Total 1 minute max.
(3) Solvent temperature : 15～40℃

5. Package outline specification.
Refer to the attached drawing.

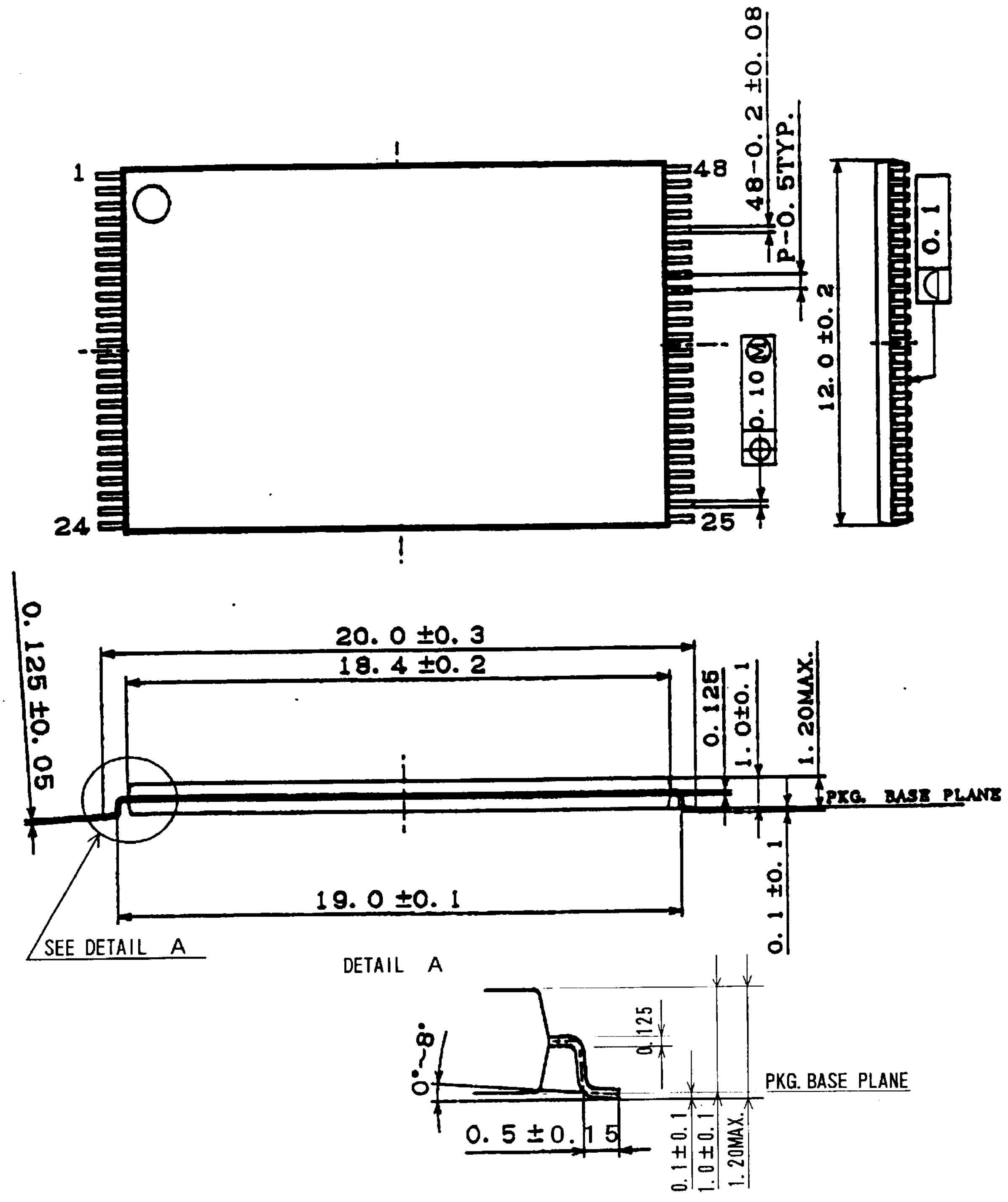
6. Markings.

6-1.Marking details. (The information on the package should be given as follows.)

(1) Product name : LH28F128BFHED-PWTL90
(2) Company name : SHARP
(3) Date code
(Example) YY WW XXX
▶Denotes the production ref. code (1~3 digits).
▶Denotes the production week. (01・02・~・52・53)
▶ Denotes the production year. (Last two digits of the year.)
(4) "JAPAN" indicates the country of origin.

6-2.Marking layout.

The layout is shown in the attached drawing.
(However, this layout does not specify the size of the marking character and marking position.)

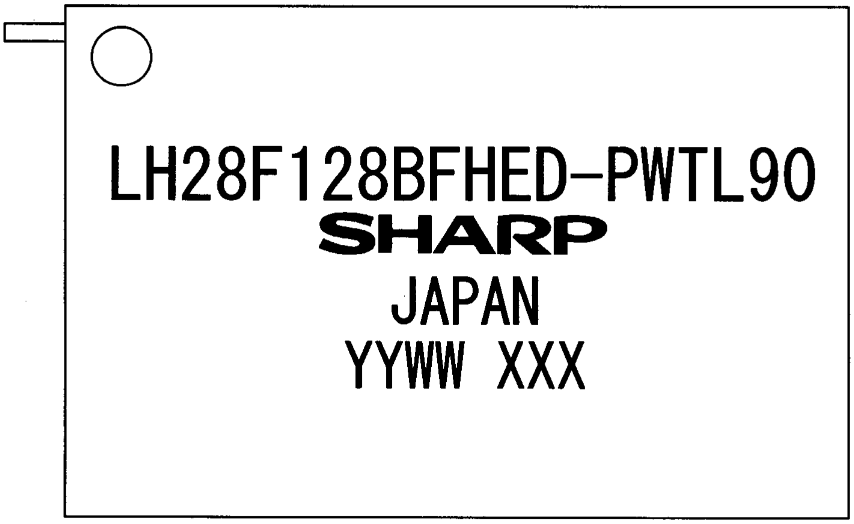


LEAD TYPE	LEAD FINISH	LEAD MATERIAL
	~~Sn/Bi/ PLATING~~	~~42ALLOY~~
	TIN-LEAD PLATING	42ALLOY

NAME	TSOP048-P-1220			備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。
DRAWING NO.	AA1142	UNIT	mm	NOTE Plastic body dimensions do not include burr of resin.

20020219

マークレイアウト図
Marking layout



7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (500 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (50 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (2000 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2.Outline dimension of tray.

Refer to the attached drawing.

7-3.Outline dimension of carton.

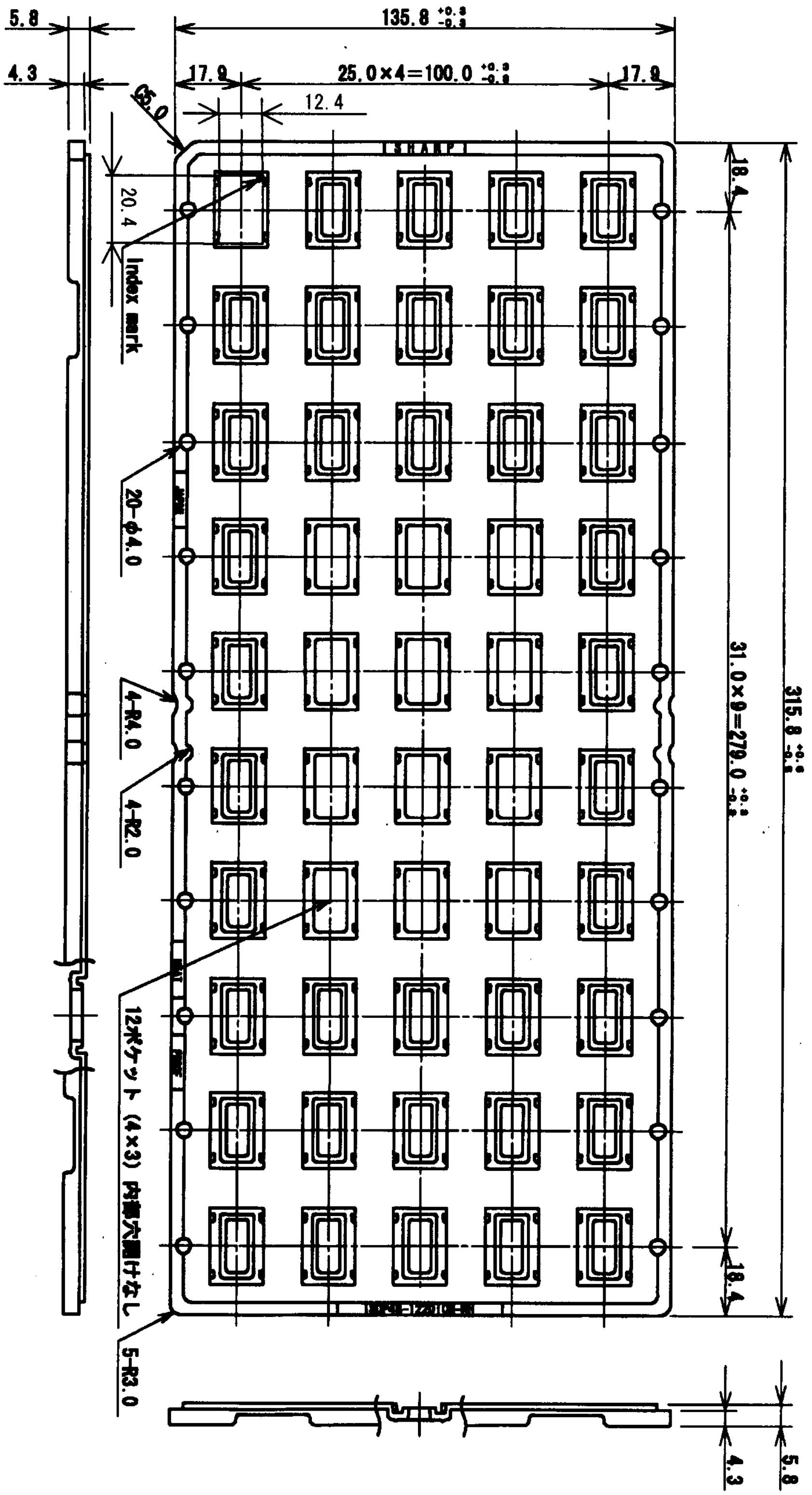
Refer to the attached drawing.

8. Precautions for use.

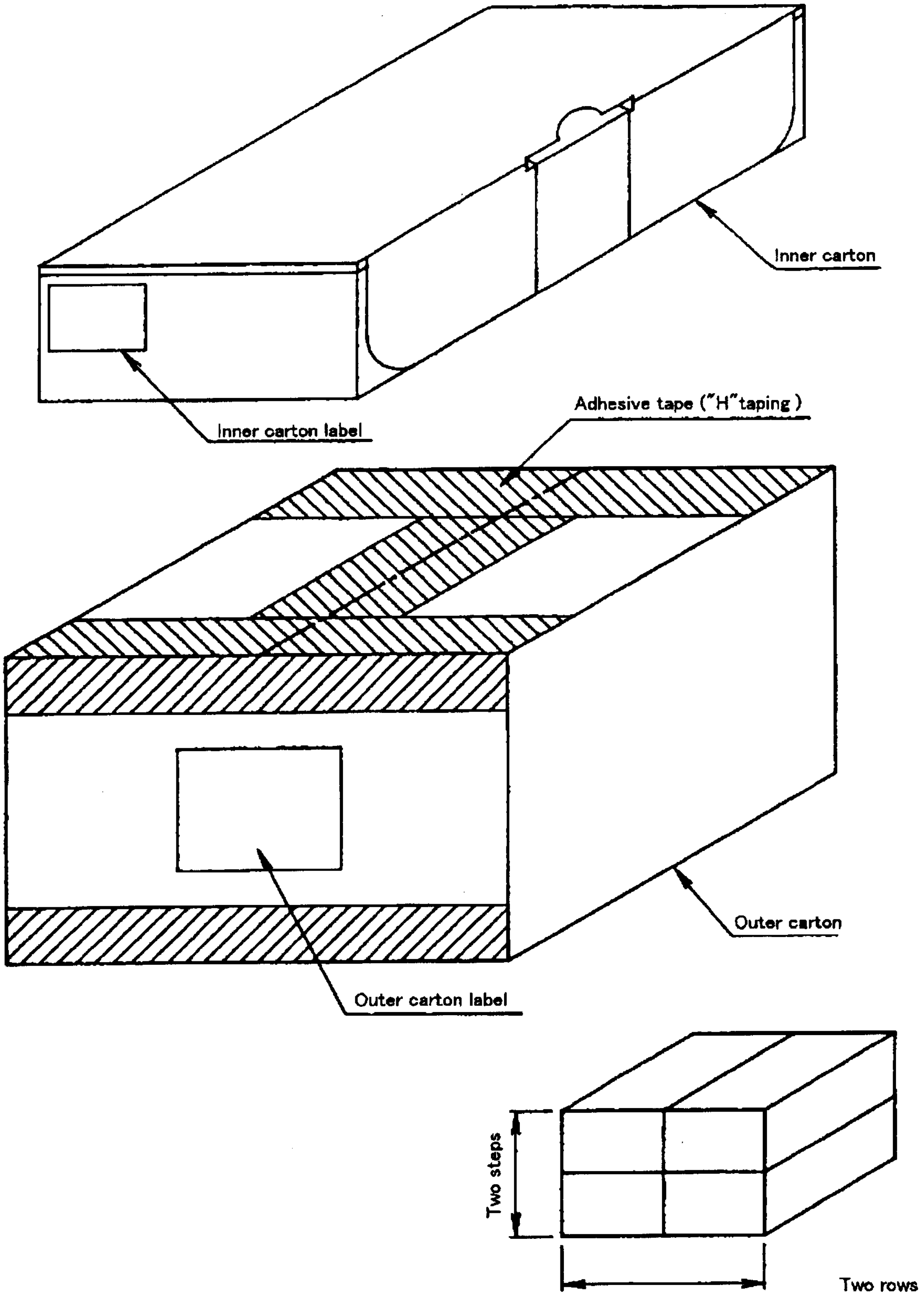
(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.

(3) The devices should be mounted the devices within one year of the date of delivery.



名称 NAME	TSOP48-1220TCM-RH		備考 NOTE
DRAWING NO.	CV756	単位 UNIT	mm

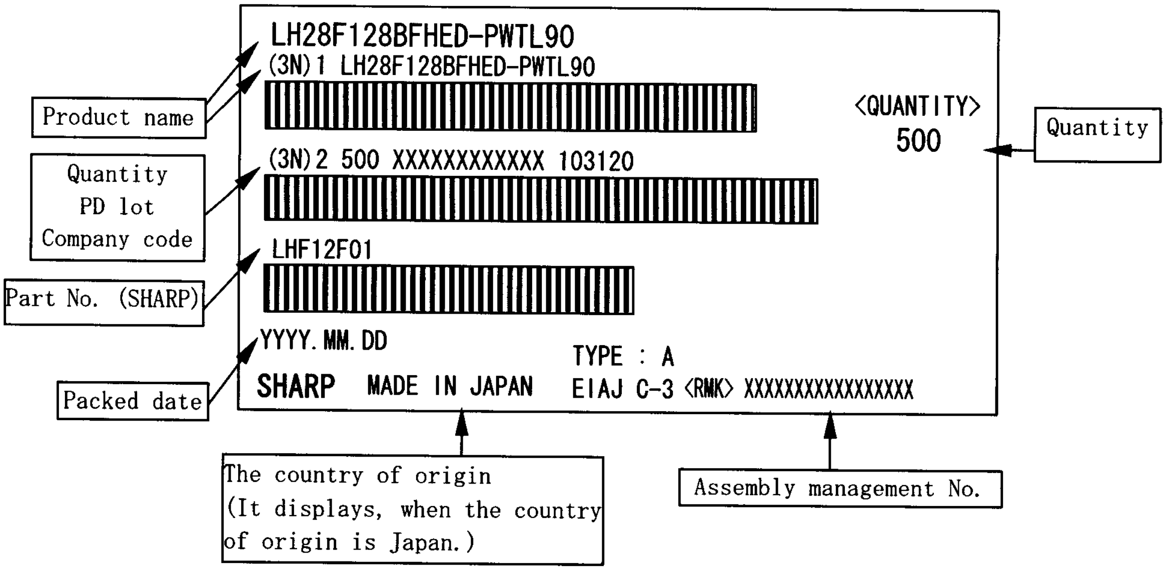


L × W× H
Inner carton - Outer dimensions : 335×150×80
Outer carton - Outer dimensions : 340×310×175

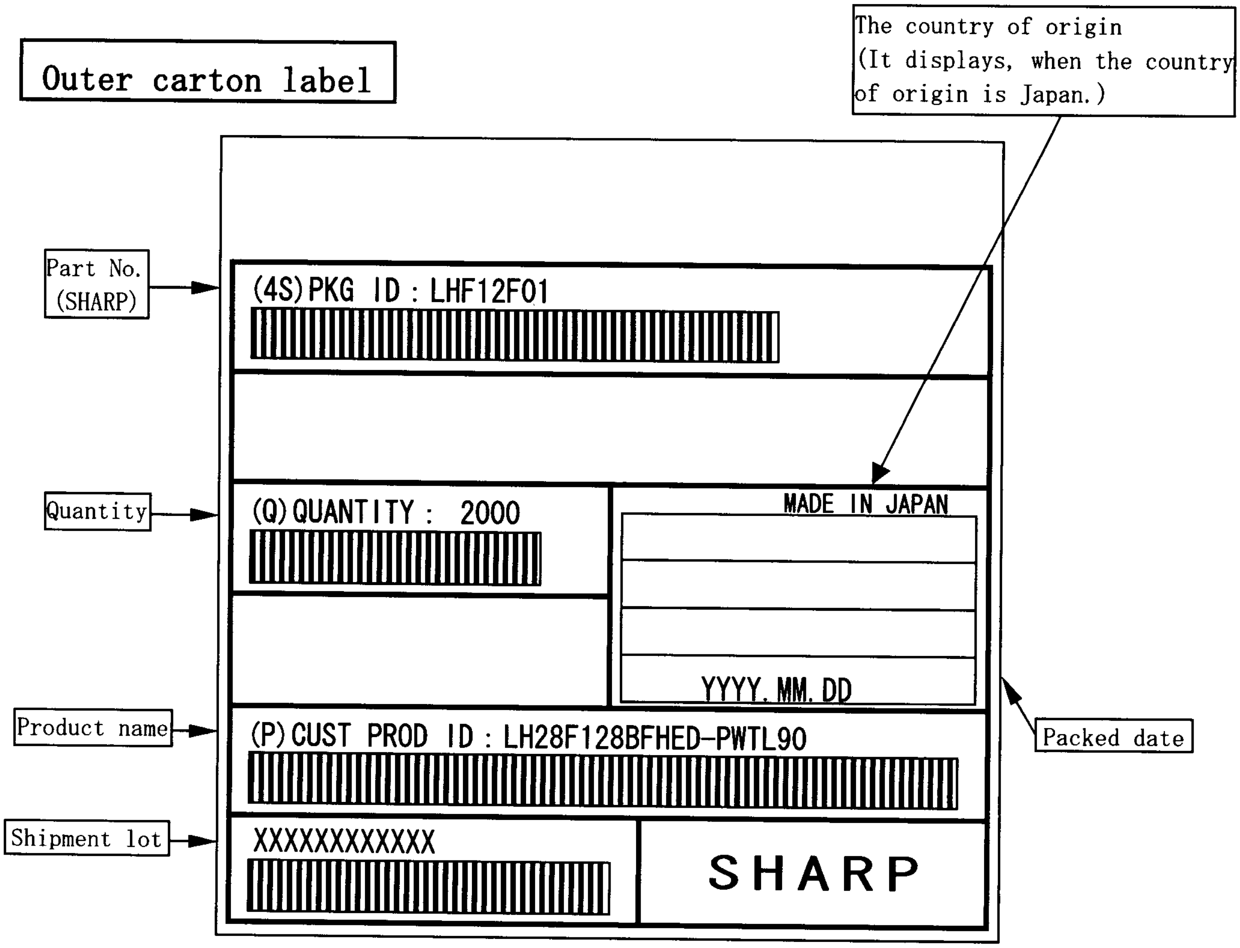
名称 NAME	トレイ品 包装仕様 Packing specifications		
DRAWING NO.	BJ433	単位 UNIT	mm

備考 出荷数量が端数の場合、本仕様と異なることがあります。
NOTE There is a possibility different from this specification when the number of shipments is fractions.

Inner carton label



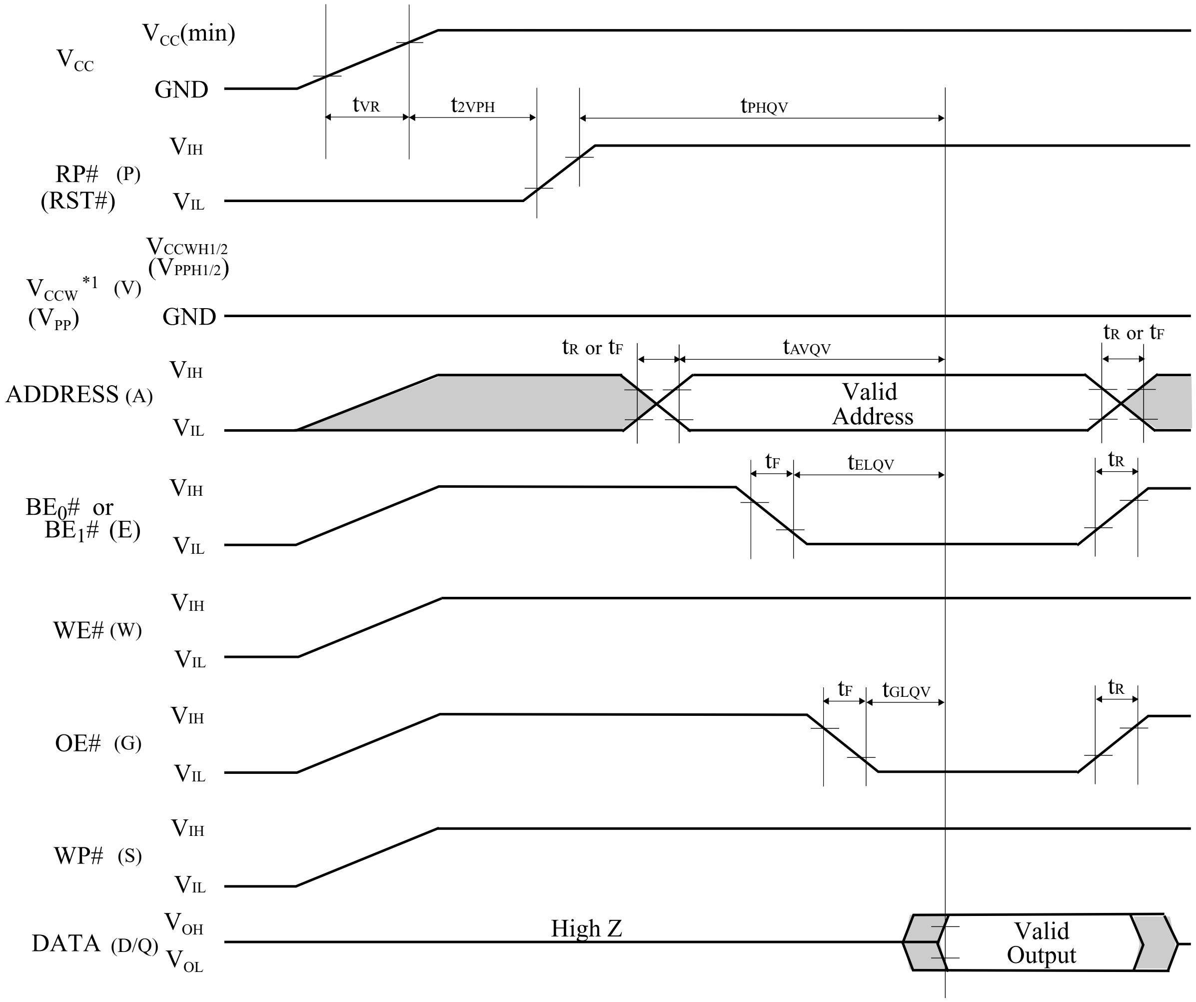
Outer carton label



A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the design, which applies V_{CCW} (V_{PP}) to 0V during read operations and $V_{CCWH1/2}$ ($V_{PPH1/2}$) during write or erase operations. See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

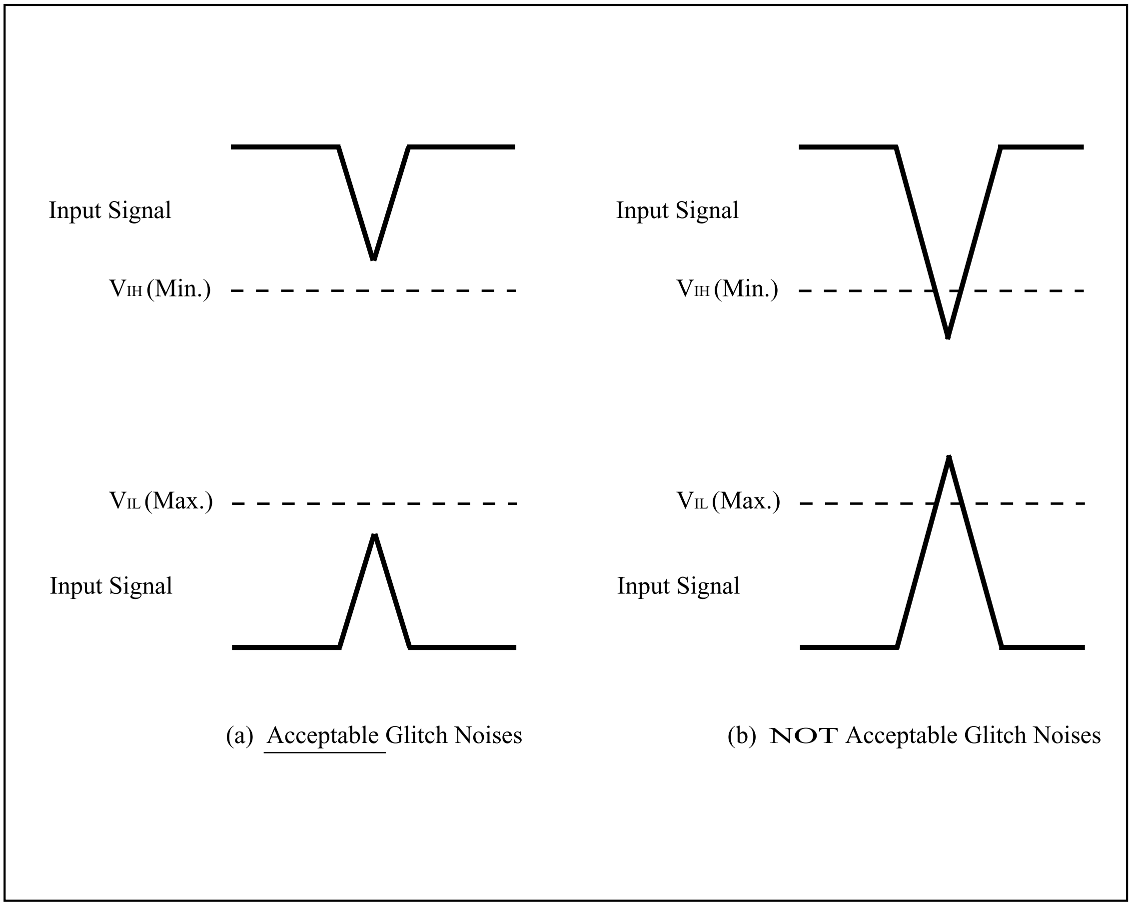
A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).



(a) Acceptable Glitch Noises (b) NOT Acceptable Glitch Noises

Figure A-2. Waveform for Glitch Noises

See the “DC CHARACTERISTICS“ described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION[1]

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

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