



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LA4425PV

Monolithic Linear IC
For Car Radio and Car Stereo
5W Power Amplifier
with Very Few External Parts

Overview

The LA4425PV is a 5W power amplifier with very few external parts. Encapsulated in a surface mount package [SSOP44K (275 mil)], it is designed for operation without a heat sink. Only two external parts (Only IN/OUT coupling capacitors). Almost no evaluation, adjustment and check of its functions as a power IC required, enabling control to be simplified and set patterns to be further miniaturized.

Functions

- Wide operation supply range → 5 to 16V
- On-chip protection:
 - Over-voltage protection
 - Thermal protection
 - Output D.C. short protection .
- On-chip pop noise reducing circuit

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	Rg = 0Ω	18	V
Surge maximum supply voltage	V _{CC} surge	Giant pulse 200ms Rise time 1ms	50	V
Maximum output current	I _O peak		3.3	A
Allowable power dissipation	Pd max	When mounted on the specified PCB	5.15	W
Operating temperature	T _{opr}		-40 to +85	°C
Storage temperature	T _{stg}		-40 to +150	°C

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LA4425PV

Operating Conditions at $T_a = 25^\circ\text{C}$,

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		13.2	V
Recommended load resistance	R_L		4	Ω
Operating voltage range	$V_{CC\text{ op}}$		5 to 16	V
Operating load resistance range	$R_L\text{ op}$	Under conditions where maximum ratings are not exceeded	2 to 8	Ω

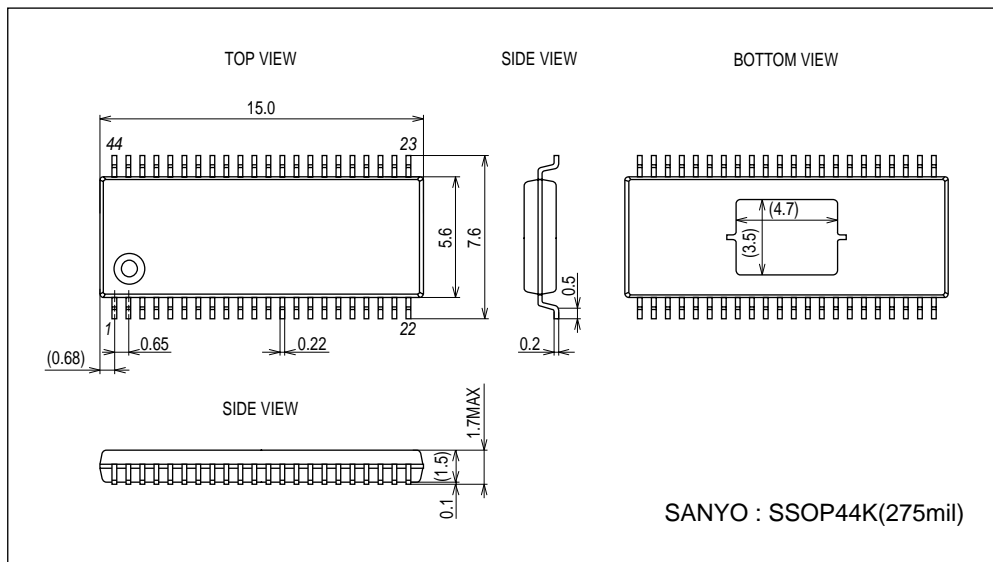
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 13.2\text{V}$, $R_L = 4\Omega$, $f = 1\text{ kHz}$, $R_g = 600\Omega$, Specified board/specified circuit

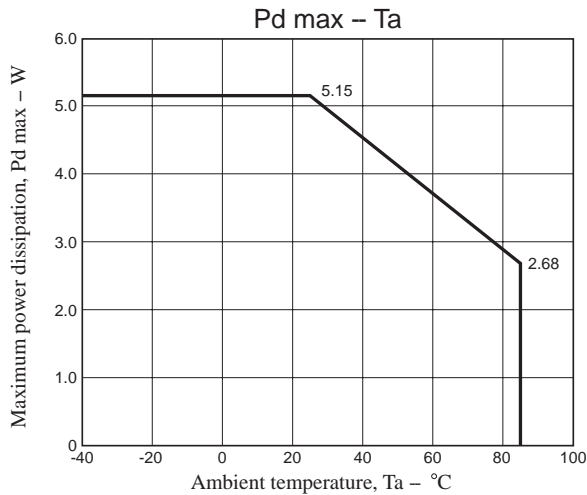
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}			65	130	mA
Voltage gain	V_G	$V_O = 0\text{dBm}$	43	45	47	dB
Output power	P_{O1}	$13.2\text{ V} / 4\Omega$, THD = 10%	4	5		W
	P_{O2}	$14.4\text{ V} / 4\Omega$, THD = 10%	5	6		W
Total harmonic distortion	THD	$V_O = 2\text{Vrms}$		0.1	1.0	%
Output noise voltage	V_{NO}	$R_g = 0\Omega$, BPF = 20 Hz to 20 kHz		0.15	0.5	mV
Ripple rejection ratio	SVRR1	$R_g = 0\Omega$, BPF = 20 Hz to 20 kHz $V_R = 0\text{dBm}$, $f_R = 100\text{Hz}$	30	40		dB
	SVRR2	$R_g = 0\Omega$, BPF = 20 Hz to 20 kHz $V_R = 0\text{dBm}$, $f_R = 1\text{kHz}$		47		dB
Over-voltage attack	V_{CCX}	$R_g = 0\Omega$		21.5		V
Starting time	t_S			0.35		s
Input resistance	R_{IN}			50		$k\Omega$
Roll-off frequency	f_L			40		Hz
	f_H			90		kHz

Package Dimensions

unit : mm (typ)

3333



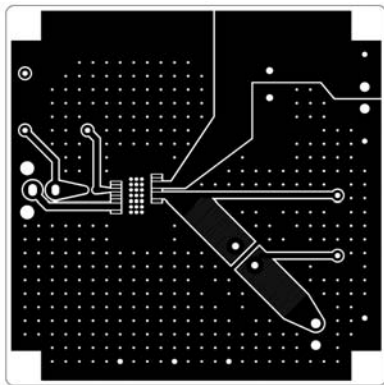


Board specifications of the Pdmax - Ta measurement (LA4425PV specified PCB)

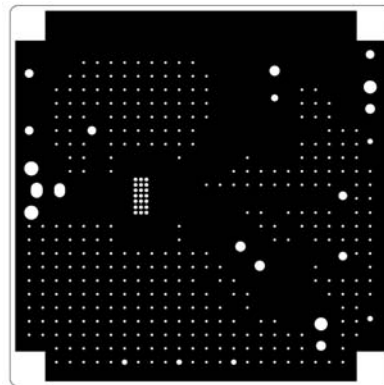
Size: 70mm × 70mm × 1.6mm³ (Four layer boards)

Copper foil thickness: L1/L4=18μm, L2/L3=35μm

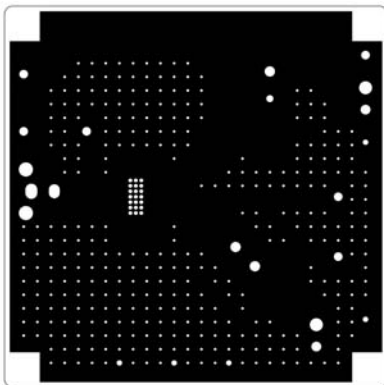
Materials: FR-4 (Glass cloth matrix epoxy resin)



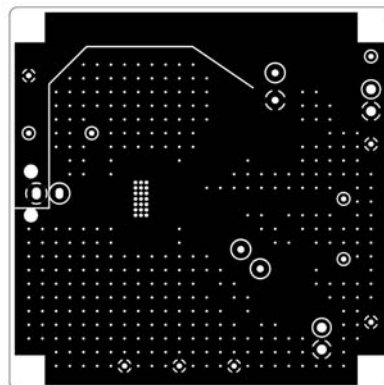
L1: Figure of copper wiring pattern



L2: Figure of copper wiring pattern



L3: Figure of copper wiring pattern



L4: Figure of copper wiring pattern

Notes:

The data for the case with the exposed die-pad substrate mounted shows the values when 95% or more of the Exposed Die-Pad is wet.

1. For the set design, employ the derating design with sufficient margin.
2. Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.

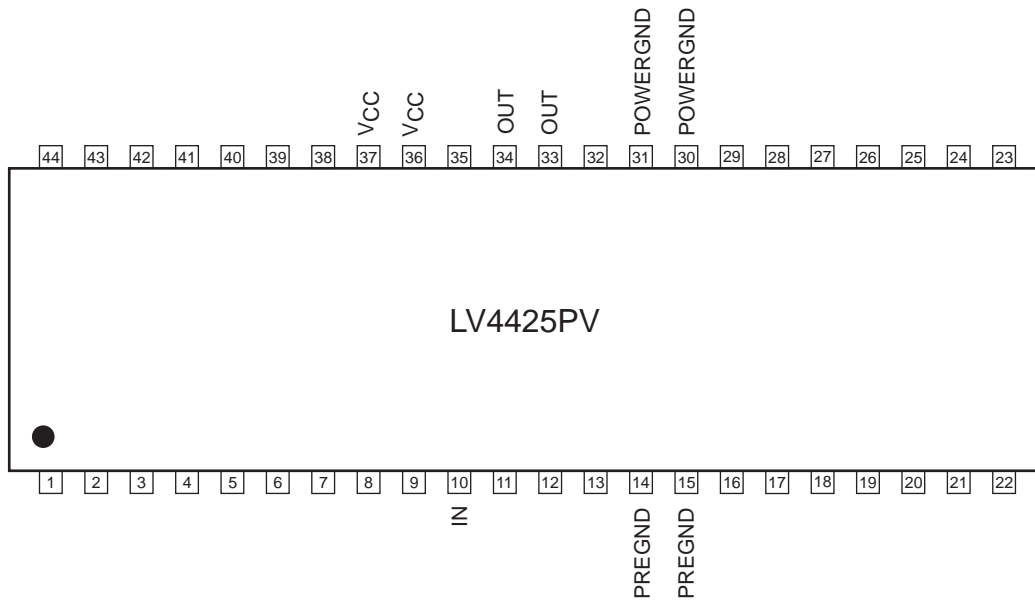
Accordingly, the design must ensure these stresses to be as low or small as possible.

The guideline for ordinary derating is shown below:

- (1) Maximum value 80% or less for the voltage ratings
 - (2) Maximum value 80% or less for the current ratings
 - (3) Maximum value 80% or less for the temperature ratings
3. After the set has been designed, be sure to verify the design with the actual product. Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc. Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

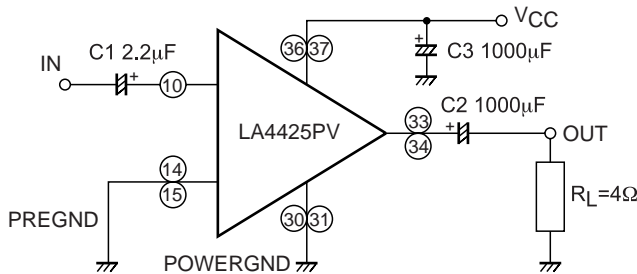
LA4425PV

Pin Assignment



- Connect exposed die pad on the back side to GND with a large pattern.
- Pins whose names are not given next to the pin numbers are all “NC pins” that are not connected to the chip inside the package, and they must not be used as relay pins.

Application Circuit Example



- On-chip overvoltage protection
- On-chip thermal protection
- On-chip pop noise reducing circuit
- On-chip output D.C. short protection

Pin Voltage at $V_{CC} = 13.2V$

Characteristics	Input	Pre GND	Power GND	Output	V_{CC}
Pin No.	10	14, 15	30, 31	33, 34	36, 37
Pin voltage (reference value)	($\approx 2V_{BE}$) 1.4V	0V	0V	($\approx 1/2V_{CC}$) 6.5V	(V_{CC}) 13.2V

IC Usage Notes

- Maximum ratings

If the IC is used in the vicinity of the maximum ratings, even a slight variation in conditions may cause the maximum ratings to be exceeded, thereby leading to a breakdown.

- Printed circuit board

When drawing the printed circuit pattern, refer to the sample printed circuit pattern. Be careful not to form a feedback loop between input and output.

Always use both pins of the Pre GND, Power GND, OUT and V_{CC} when designing the layout.

- Exposed Die-Pad

The exposed die pad on the back side of the IC must be connected to GND with a large pattern surface area.

- Load Resistance and Misoperation

It should be noted that when $R_L < 2\Omega$ and V_{CC} is high, and the switch is turned “ON” when setting is for a signal (THD = 10%), the ground detector (current × voltage Schmitt circuit) operates momentarily.

- Starting Time (t_s)

This is set at 0.35sec/typ, but it can be made shorter by making input capacitor C_i smaller, or longer by making it larger.

- Pop noise

The pop noise prevention circuit operates to reduce pop until R_g reaches 50kΩ. However, if R_g is left open, the charging route of input capacitor C_i is lost, so the pop noise reduction circuit stops operating and click noises become louder.

- VG/OSC

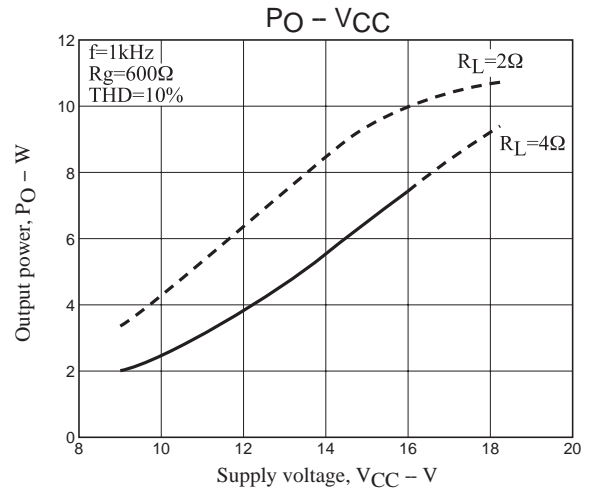
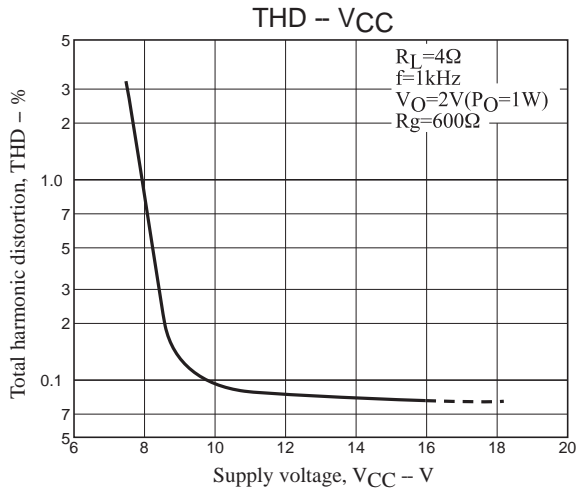
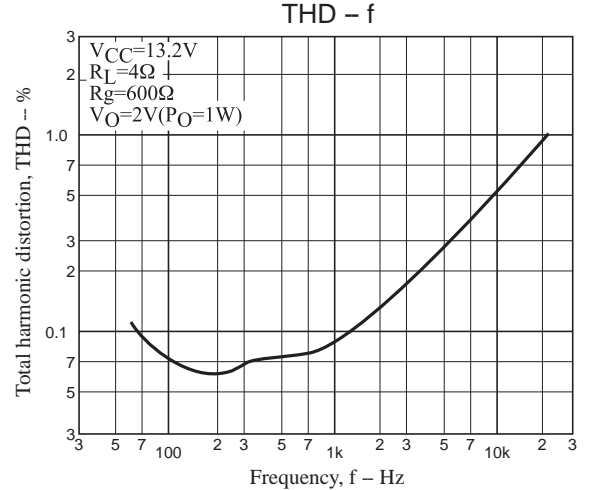
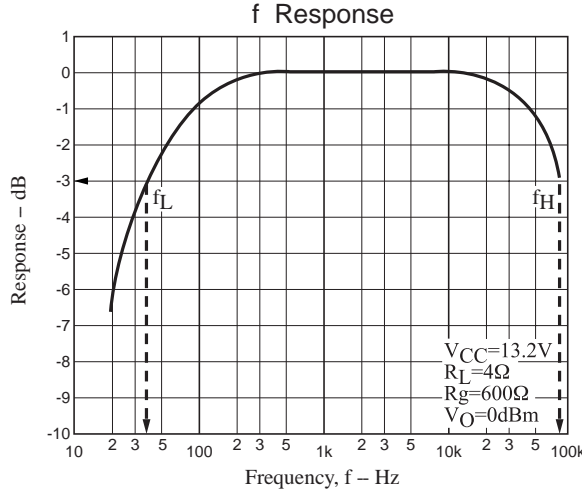
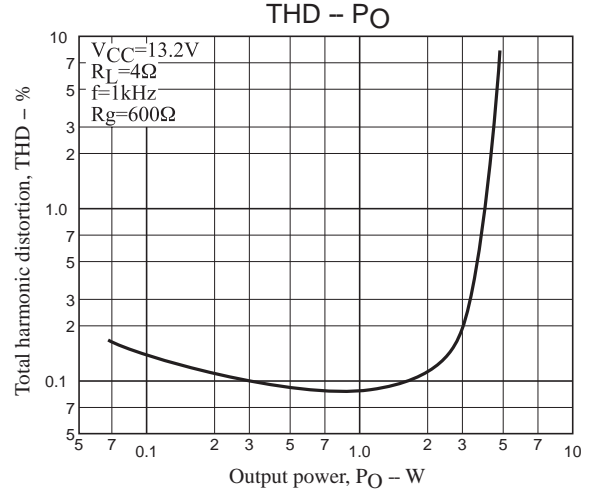
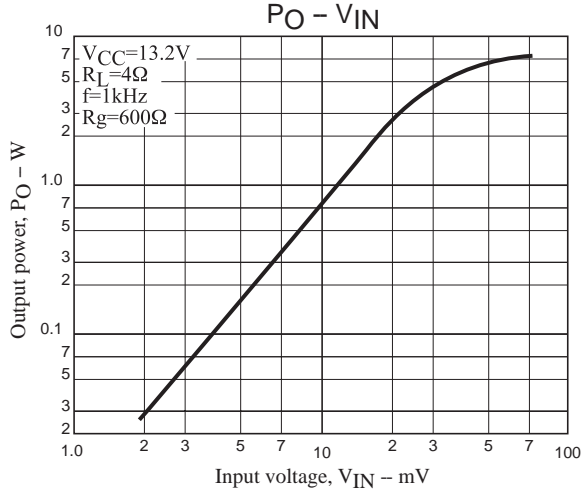
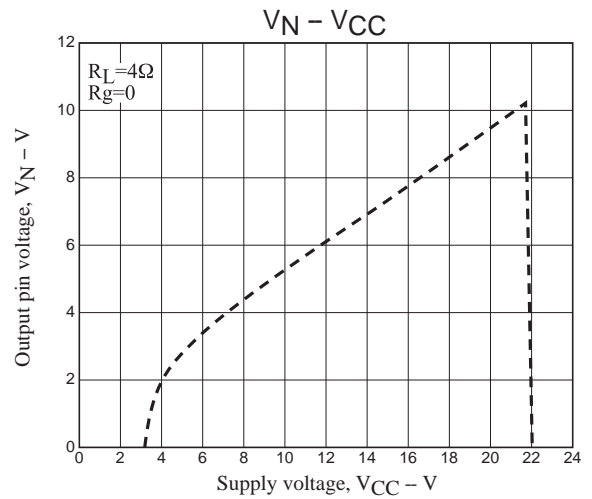
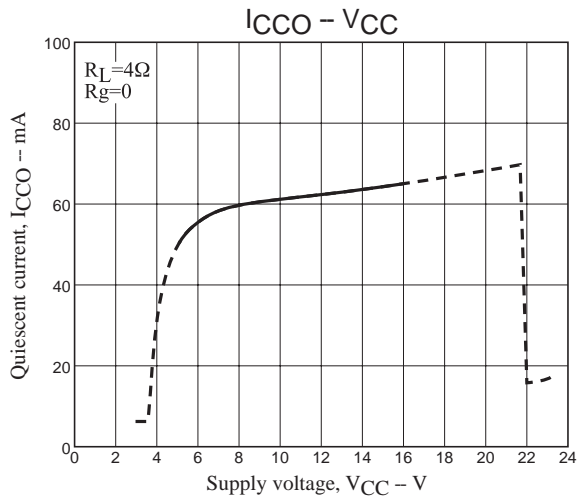
The voltage gain is fixed at 45dB inside the IC. It is impossible to change it externally.

Phase compensation capacitors (350pF/total) are connected between individual stages inside the IC, and the open loop gain is low. In addition, the upper and lower drives are made equivalent so that final stage current gain is adjusted, providing a measure against unwanted high-frequency parasitic oscillation peculiar to power IC's.

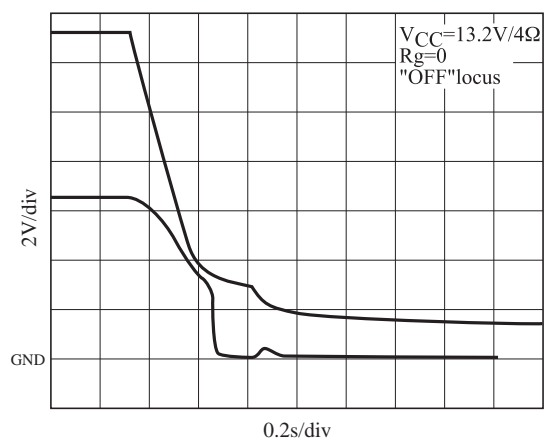
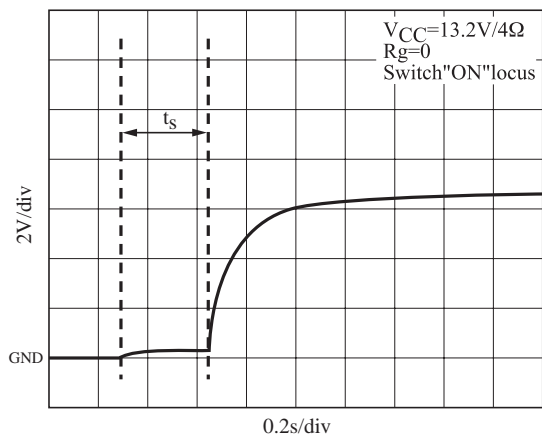
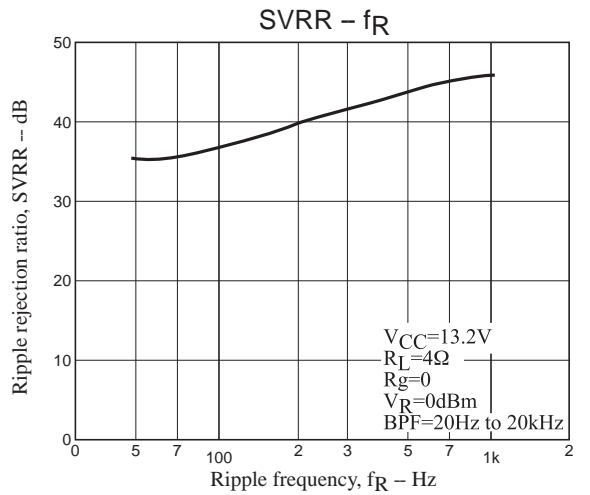
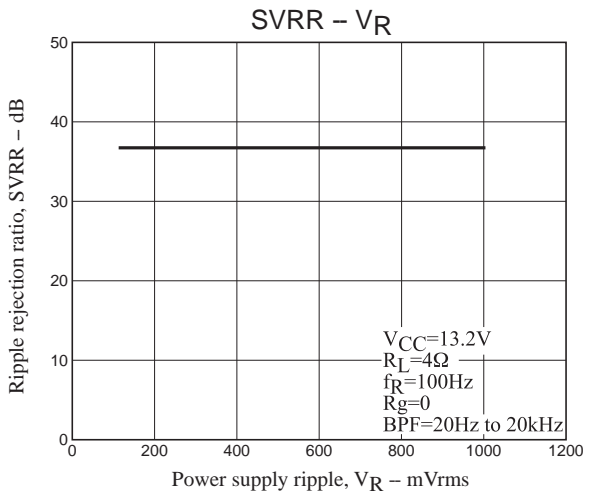
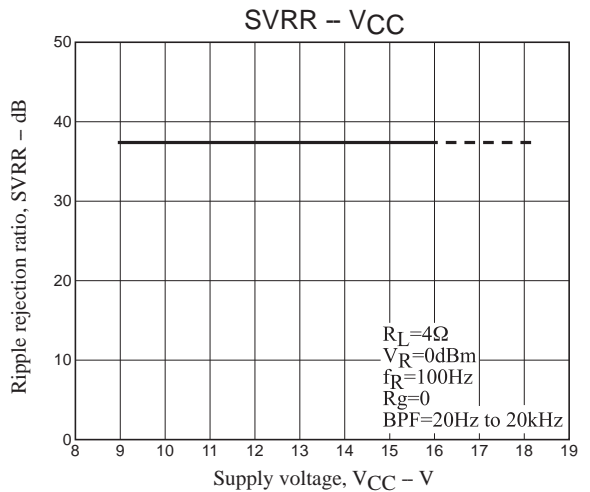
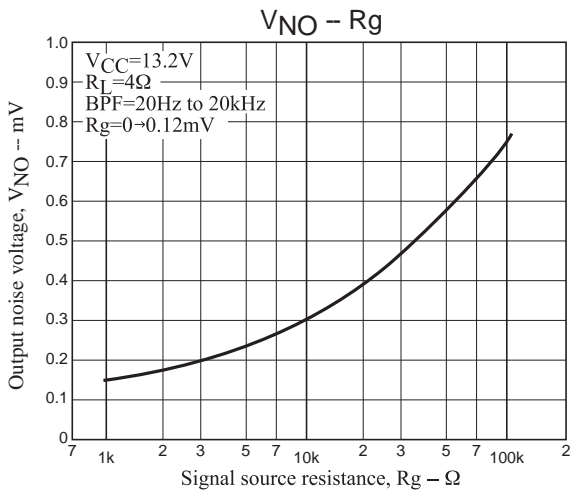
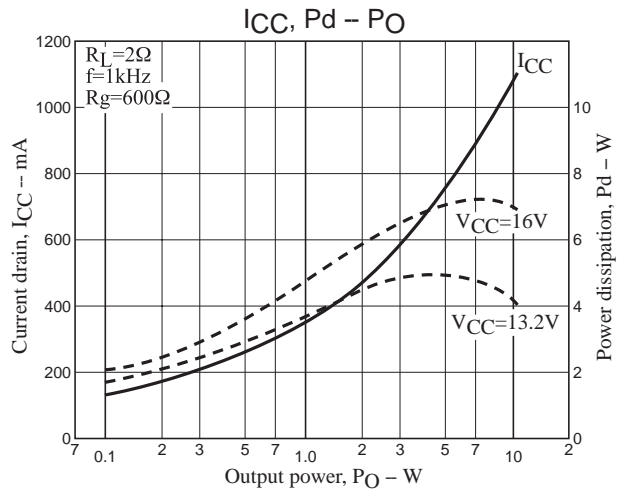
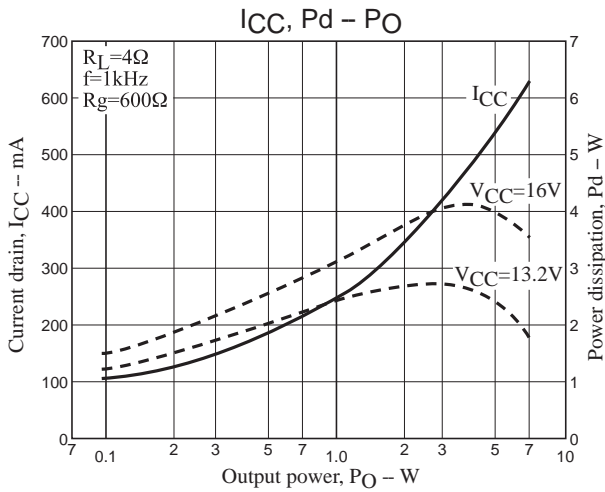
- BTL Connection

Connection is impossible with IC alone.

LA4425PV



LA4425PV



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