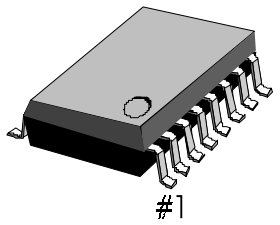
KS8808A PLL Frequency Synthesizer for Pager

INTRODUCTION

KS8808A is a superior low-power-programmable PLL frequency synthesizer which can be used in a high performance Wide Area Pager system.

KS8808A consists of 2 kinds of divider block including a 17bit Shift register, 16-bit Latch, 14/16-bit Counter, Prescaler, and a phase detector block including a Phase detector, Lock detector and a Charge pump.

16 - SSOP- 0044



(Magnification = 1 : 4)

ORDERING INFORMATION

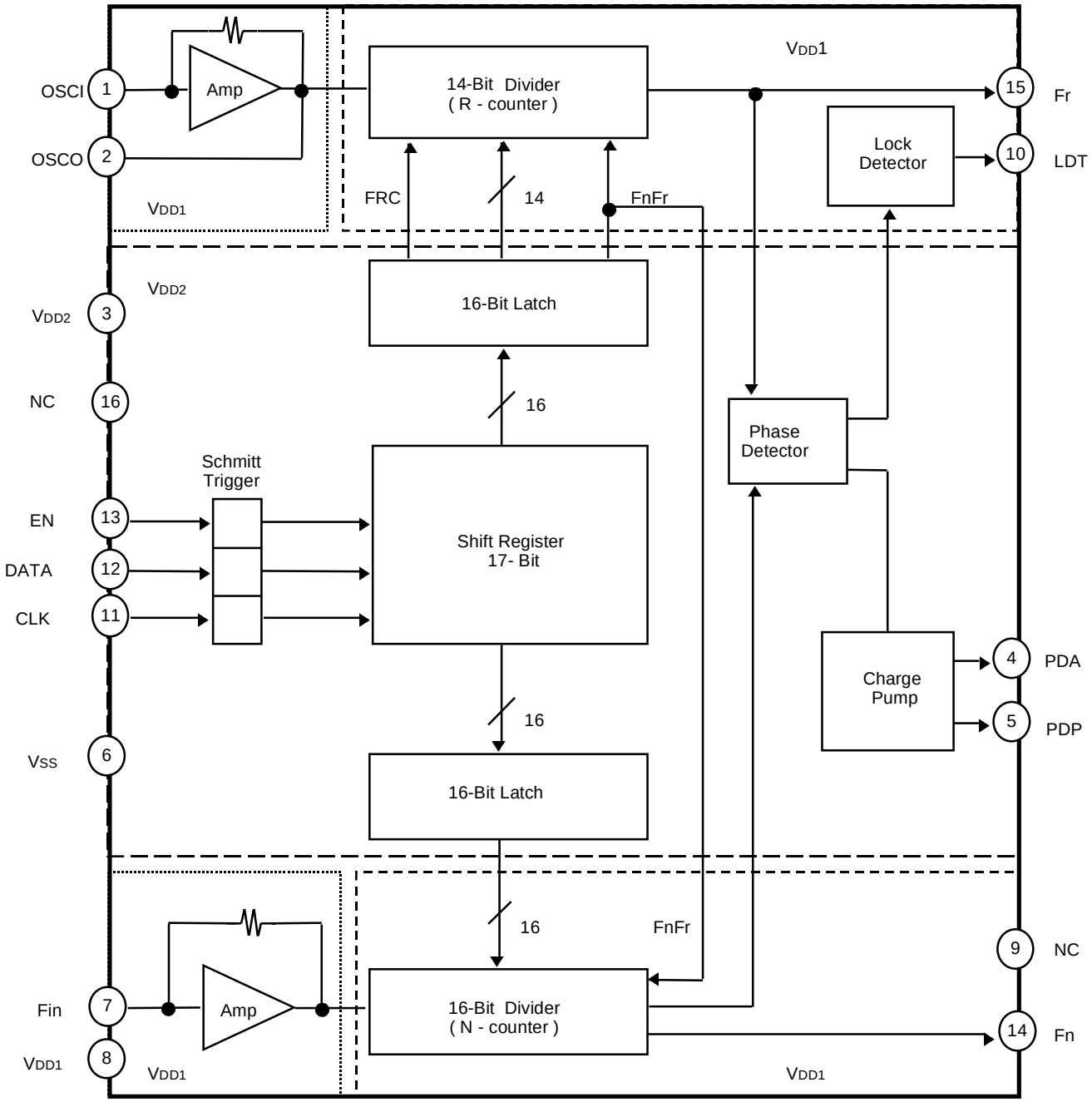
Device	Package	Operating Temperature
+ KS8808D	16 - TSSOP	- 25 ℃ ~ + 75℃

+ : New Product

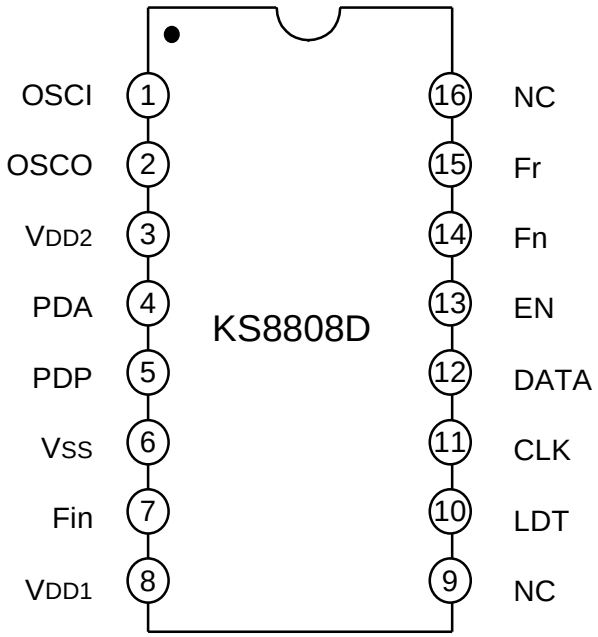
FEATURES

- Maximum operating frequency : 120 MHz @ 500mVp-p, V_{DD1}=0.95 V
  165 MHz @ 500mVp-p, V_{DD1}=1.0 V
- On-chip reference oscillator supports an external crystal which oscillates up to 18 MHz.
- Superior supply current :
  F_{IN} = 90 MHz , I_{DD1} = 0.6 mA (Typ.) @ V_{DD1}=1.0 V, V_{DD2}=3.0 V.
  F_{IN} =150 MHz , I_{DD2} = 0.9 mA (Typ.) @ V_{DD1}=1.0 V, V_{DD2}=3.0 V.
  Operating voltage : V_{DD1} = 0.95 V ~ 2.0 V, V_{DD2} = 2.0 V ~ 3.3 V.
- Reference frequency counter divider range : 1 / 28 ~ 1 / 65532 (Multiple 4)
  But, the Divider range with FRC_High state : 1 / 7 ~ 1 / 16383
- RX frequency counter divider range : 1 / 28 ~ 1 / 65535
- Package type : 16 - TSSOP (0.65 mm)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	OSCI	I	These input / output pins generate the reference frequency. In case of OSCI Pin, external reference frequency can be input through an AC coupling.
2	OSCO	O	
3	V_{DD2}	-	The highest potential supply terminal that can be supplied up to 2.0 V ~ 3.3 V, except for V_{DD1}.
4	PDA	O	The Output of RX Phase detector terminal for active loop filter. There are 3 - kinds of output signal states according to Rx Loop Error; - If Fr > Fn (Fr is leading), the output is negative pulse state, - If Fr < Fn (Fr is lagging), the output is positive pulse state, - If Fr = Fn (the same phase), the output is high impedance state.
5	PDP	O	The Output of RX Phase detector terminal for passive loop filter . There are 3 - kinds of output signal states according to Rx Loop Error: - If Fr < Fn (Fr is lagging), the output is negative pulse state, - If Fr > Fn (Fr is leading), the output is positive pulse state, - If Fr = Fn (the same phase), the output is high impedance state.

PIN DESCRIPTION (*Continued*)

Pin No.	Symbol	I/O	Description
6	Vss	-	Ground terminal
7	Fin	I	Input terminal for 16 bit Divider from VCO. Mostly, VCO output should be input through the AC coupling and the minimum input level is 500 mV_{P-P} (in case of 90 MHz).
8	V_{DD1}	-	Voltage supply terminal for Oscillator and Fin block. This pin can be supplied up to 0.95 ~ 2.0 V from Vss.
9	NC	-	No Connection
10	LDT	O	Lock detector is also an output of the Phase Detector . The Low state of this output shows unlock status, which is the error width between the Ref. signal and the VCO output signal.
11	CLK	I	These pins are controlled by μ-controller and it also has Schmitt Trigger architecture . The features of these pins are as follows ; Clock input for 17 - bit Shift Register, Serial data input (it includes FnFr - on / off and FRC), and Latch enable input (User selectable EN1 or EN2).
12	DATA	I	
13	EN	I	
14	Fn	O	Output terminal for divider value of N -counter. To control the output On/Off, the FnFr bit of the Reference register can be programmed. When FnFr bit is set to High , this output shows low level .
15	Fr	O	Output terminal for divider value of R -Counter. To control the output On/Off, the FnFr bit of the Reference register can be programmed. When FnFr bit is set to High , this output shows low level .
16	NC		No Connection. (pull-up)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply voltage	V_{DD1}~V_{DD2}	- 0.3 ~ 4.0	V
Input voltage	V_I	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
Power dissipation	P_D	350	mW
Operating temperature	T_{OPR}	- 25 ~ + 75	℃
Storage temperature	T_{STG}	- 40 ~ + 125	℃

ELECTRICAL CHARACTERISTICS

(Ta = 25℃ , V_{DD1} = 1.0 V , V_{DD2} = 3.0 V , unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating voltage	V_{DD1}	-		0.95	1.0	2.0	V
	V_{DD2}	-		2.0	3.0	3.3	
Operating current	I_{DD1}	F_{OSCI} = 12.8 MHz @ 0.5V_{P-P} V_{DD1} = 1.0 V V_{DD2} = 3.0 V,	F_{FIN} = 90 MHz	-	0.6	-	mA
	I_{DD2}		F_{FIN} = 150MHz	-	0.9	-	
Standby current	I_{SB}	V_{DD1} = 0 V V_{DD2} = 3.0 V		-	-	10	㎂
Input voltage (DATA, CLK, EN, BS)	V_{IL}	-		-	-	0.3	V
	V_{IH}	-		V_{DD2}-0.3	-	-	
Input Current (Fin, Xin)	I_{IH}	V_{IH}=V_{DD1}		-	-	20	㎂
	I_{IL}	V_{IL}=0V,		-	-	20	
Input frequency	F_{FIN}	V_{FIN} = 0.5Vp-p	V_{DD1} = 0.95 V	-	-	120	MHz
			V_{DD1} = 1.0 V	-	-	165	
	F_{OSCI}	V_{OSCI} = 0.5Vp-p		7	-	18	
Output Current (PDA, PDP)	I_{OH1}	V_{OH} = 0.4 V		1.0	-	-	mA
	I_{OL1}	V_{OL} = V_{DD1} - 0.4 V		1.0	-	-	
Output current (Fr, Fn , LDT)	I_{OH2}	V_{OH} = 0.4 V		0.1	-	-	mA
	I_{OL2}	V_{OL} = V_{DD1} - 0.4 V		0.1		-	
Setup-Time (DATA-CLK, CLK-EN)	t_s	-		2	-	-	uS
Hold Time	t_H	-		2	-	-	uS

▶ Program Scheme (μ-controller)

• Rx. Register (17 bits)

Bit	Bit 16 (ND 15) ~ Bit 1 (ND 0)	Bit 0 (LSB)
Name	RxD	PMC
Description	Rx. Program Data (ND 15 ~ ND 0)	Program Mode Control
Function	16-Bit Programmable Rx. N-Counter	0 : Rx. N-Counter 1 : Ref. R-Counter

• Reference Register (17 bits)

Bit	Bit 16 (RD 13) ~ Bit 3 (RD 0)	Bit 2	Bit 1	Bit 0 (LSB)
Name	RefD	FRC	FnFr	PMC
Description	Ref. Program Data (RD 13 ~ RD 0)	CONTROL MODE ※		Program Mode Control
Function	14 Bit Programmable Ref. R-Counter	0 : No FRC (OSCI / 4R) 1 : FRC (OSCI / R)	0 : Fn,Fr function 1 : Fn,Fr Low	0 : Rx. N-Counter 1 : Ref. R-Counter

※ CONTROL MODE

FRC	FnFr	Fn (Pin14)	Fr (Pin15)
0	0	Fn out (Fin / N counter)	Fr out (OSCI / 4 x R)
0	1	LOW	LOW
1	0	Fn out (Fin / N counter)	Fr out (OSCI / R)
1	1	LOW	LOW

- **Rx. Register Programming Timing (PMC=0 → 16-Bit N_Counter)**

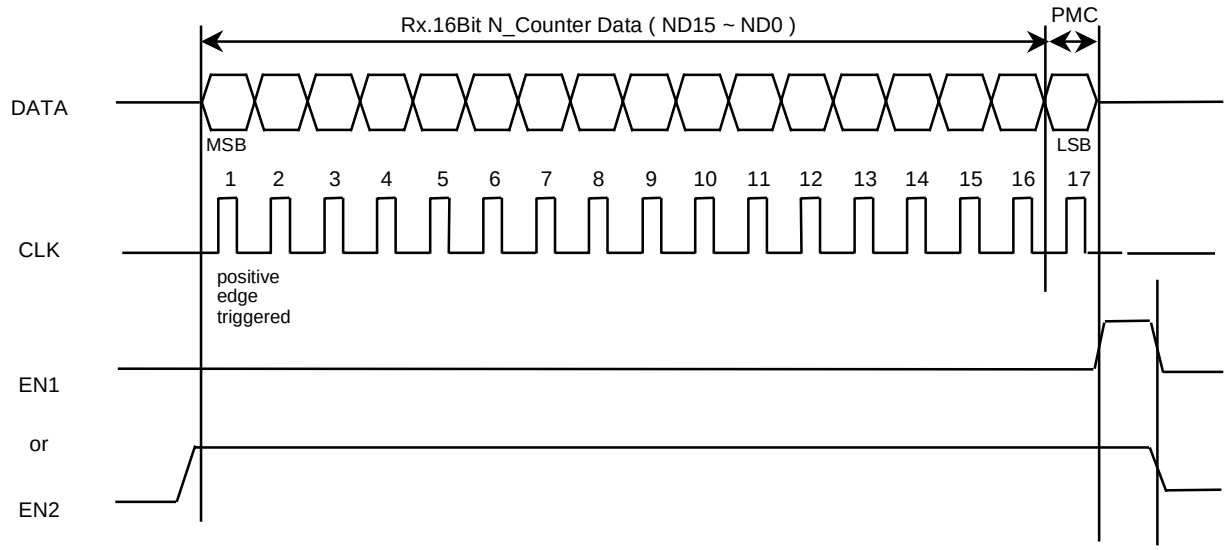


Figure 1

- **Ref.Register Programming Timing (PMC= 1 → 14-Bit R_Counter, FRC , FnFr)**

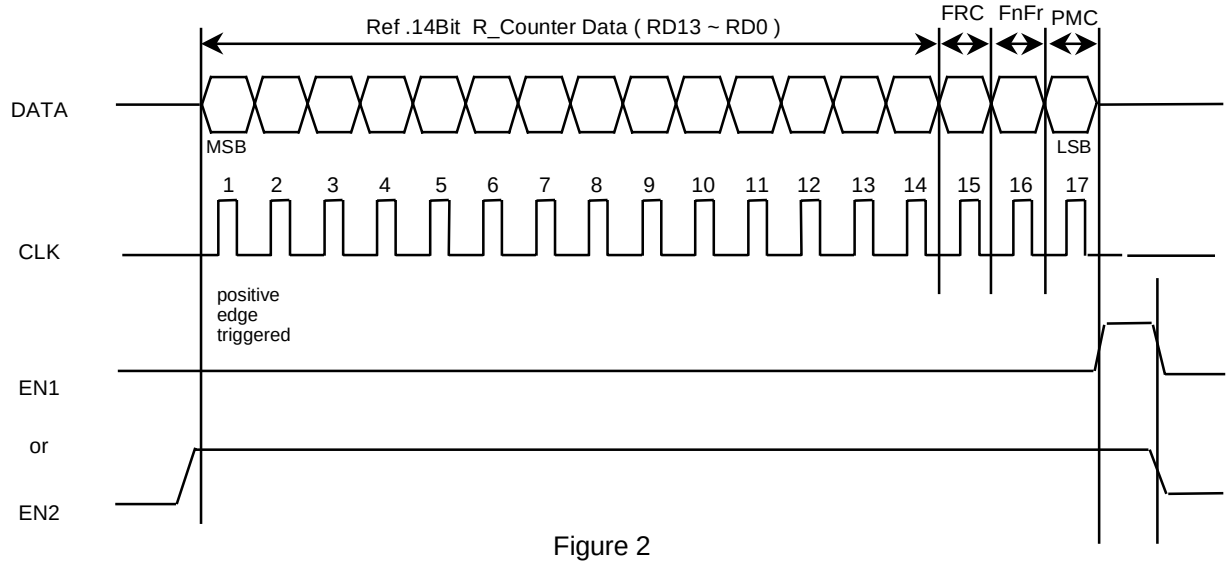


Figure 2

* It is possible to use Optional selection of EN1, EN2 (when used EN)

•Serial DATA Input Timing
& Phase Detector / Lock Detector Output Waveforms

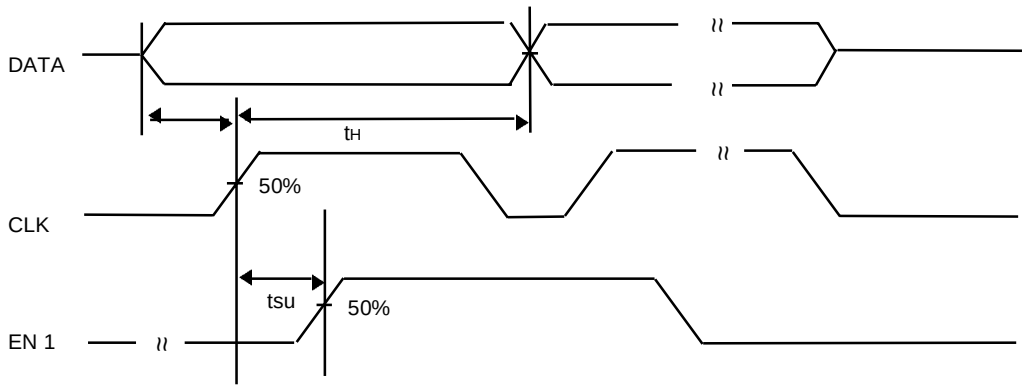


Figure 3. Serial Data Input Timing

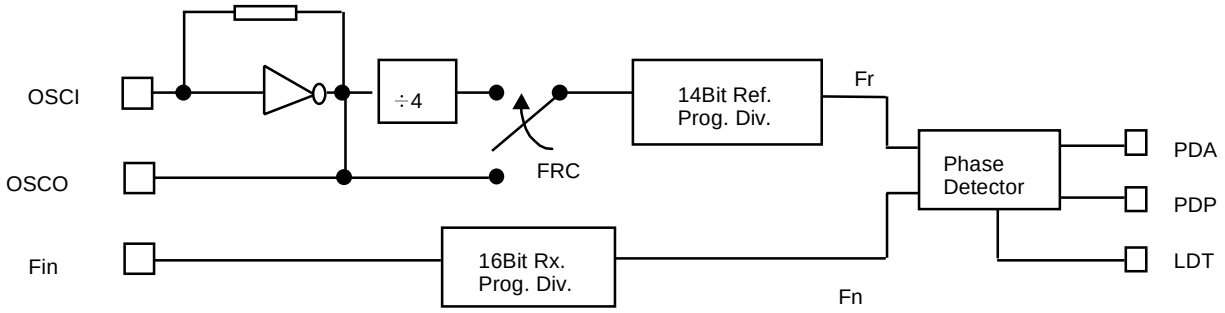


Figure 4-1. Phase Detector / Lock Detector Block Diagram

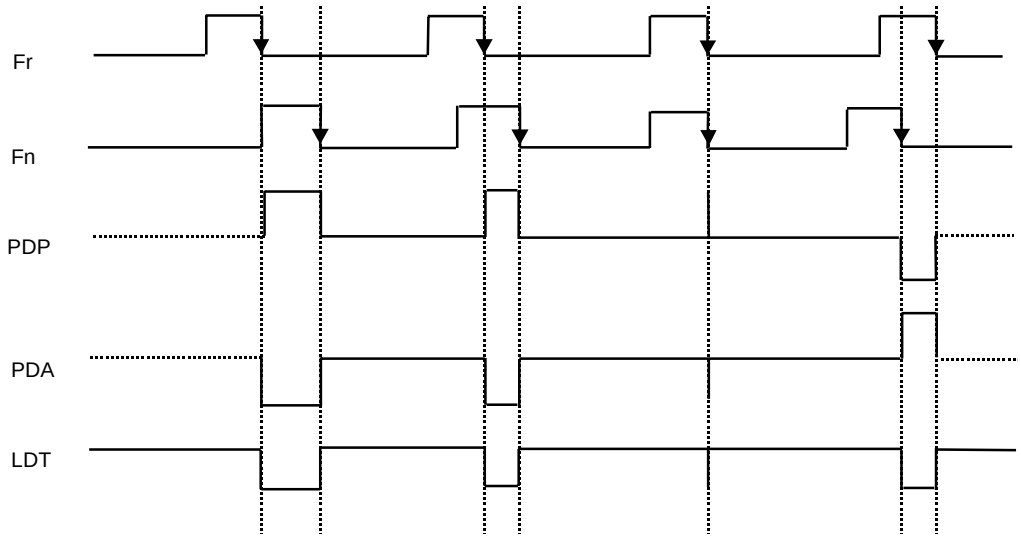
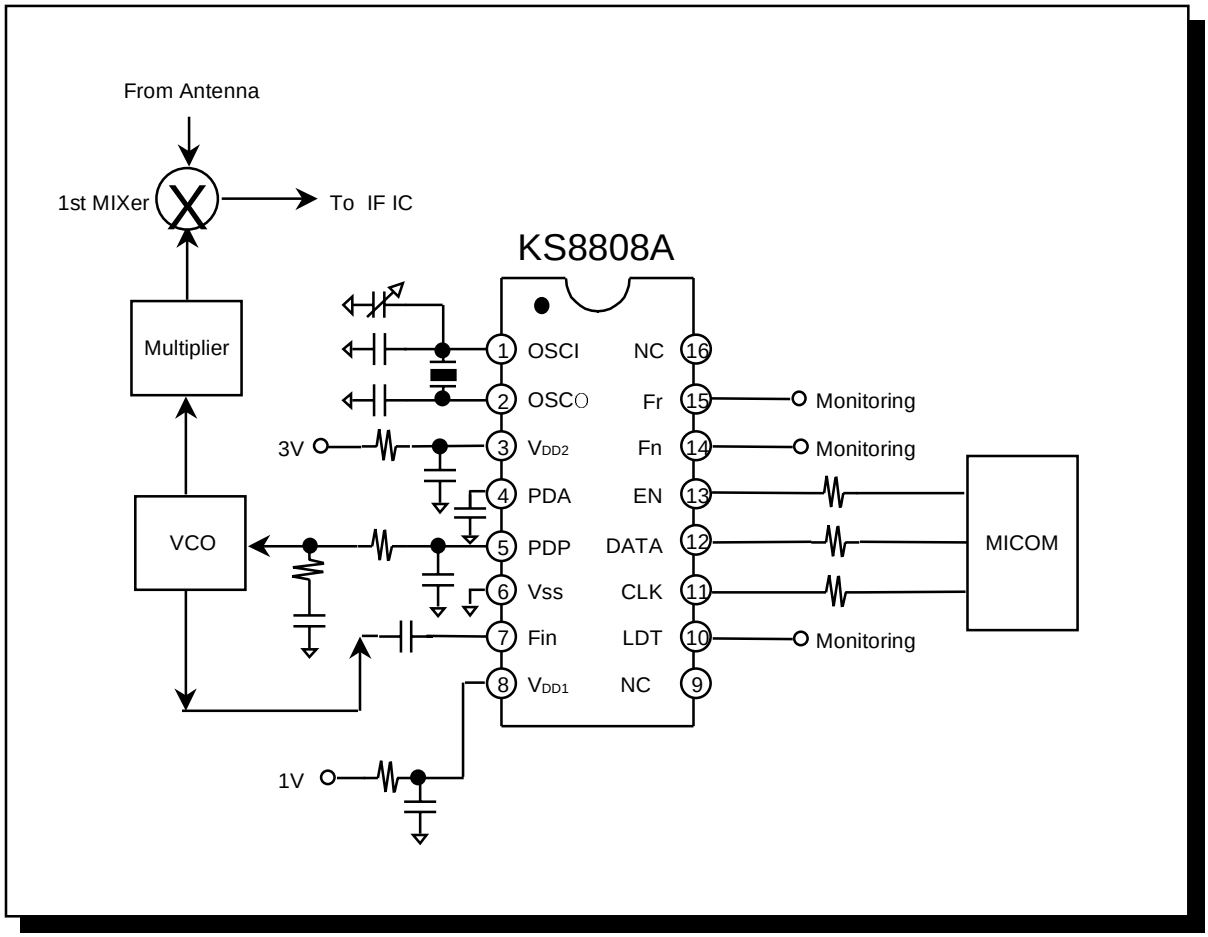


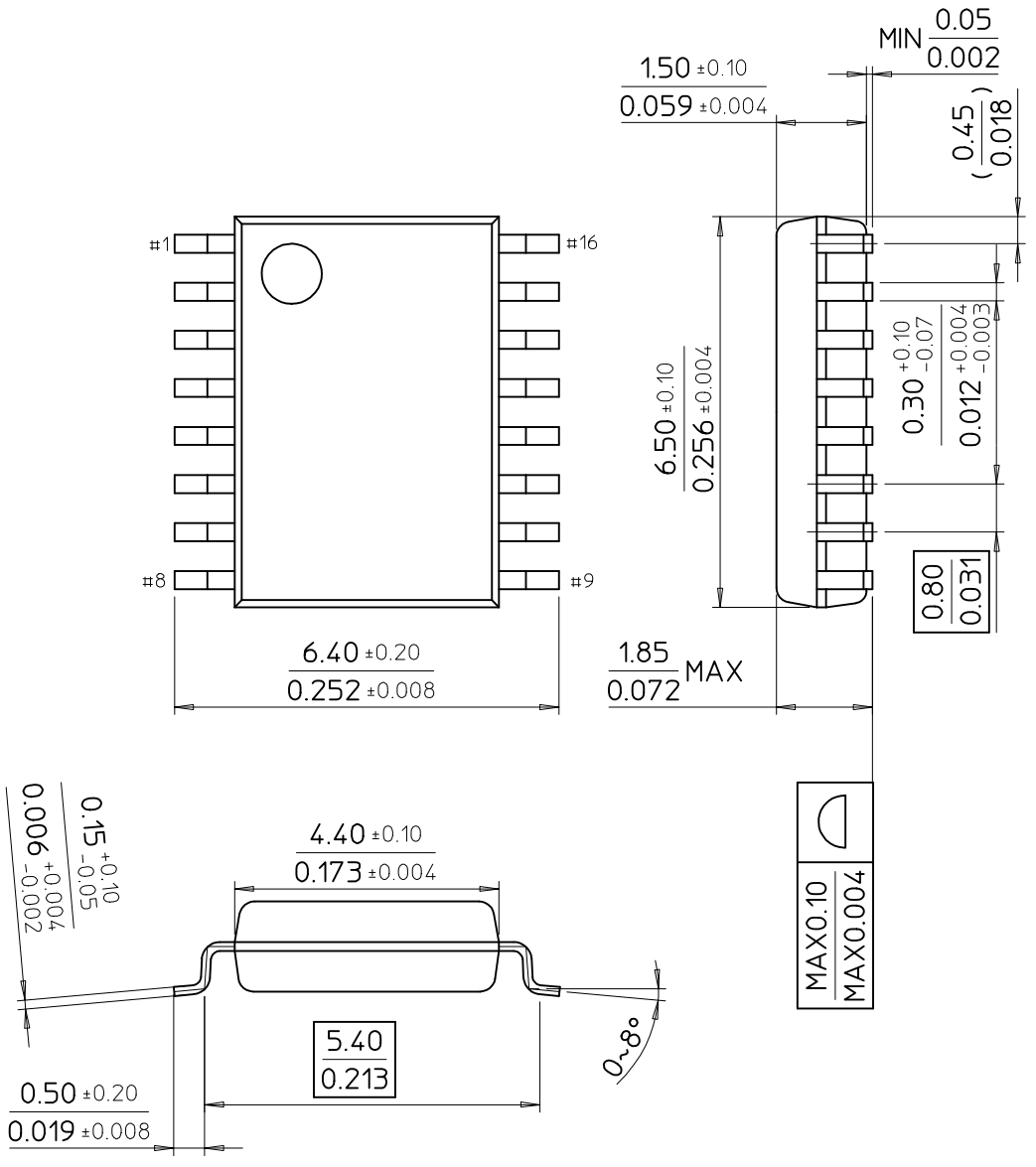
Figure 4-2. Phase Detector / Lock Detector Output Waveforms

▶ APPLICATION CIRCUIT



16–SSOP–0044

Dimensions in Milimeters/inches



SAMSUNG ELECTRONICS CO.,LTD.