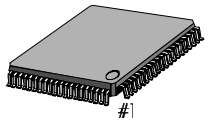
INTRODUCTION

The KS7314 offers enlarged images through the zoom effect attained by horizontal and vertical interpolation of luminance and chrominance signal input supplied from the CCD digital signal processor (KS7306). The signal input is implemented by employing a 2nd generation electronic zoom IC, which electronically enlarges the image picked up by the CCD of a camcorder. In addition, it corrects the wobble of hand-held cameras, and also provides the functions of a gyro-sensor and a mosaic mirror.

80-QFP-1212



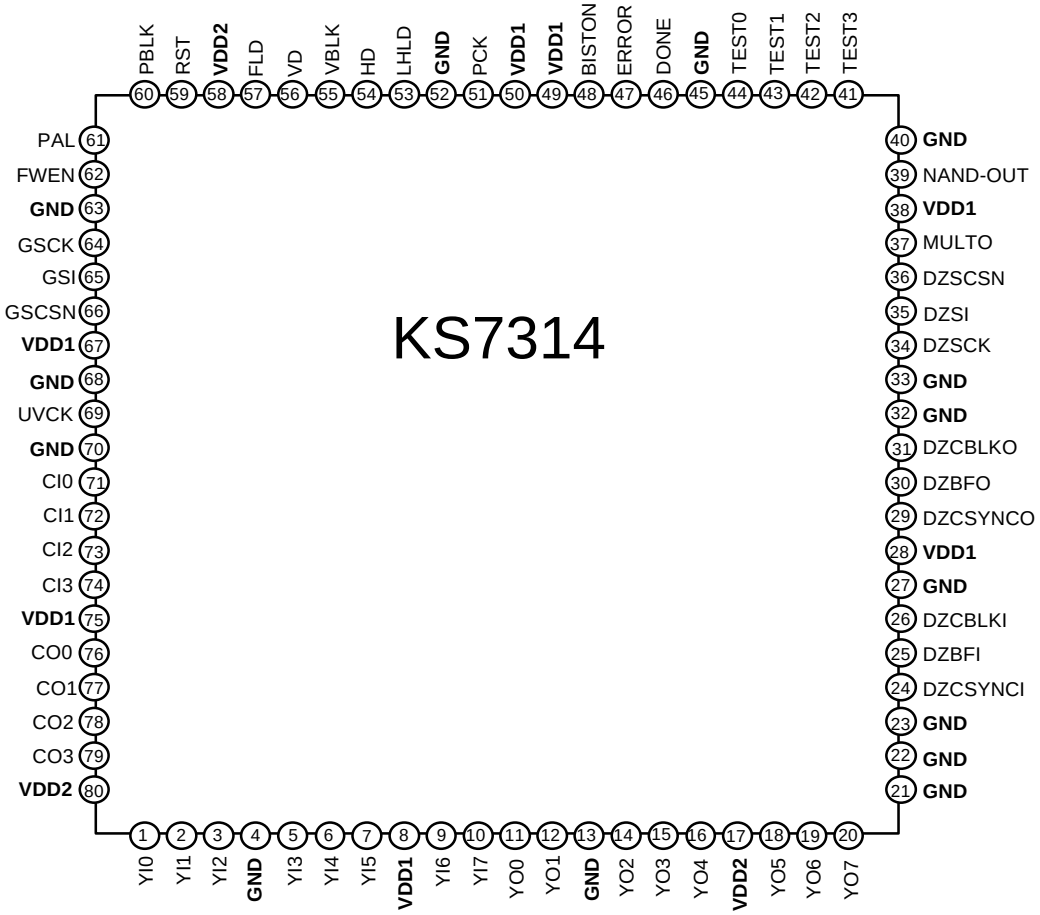
ORDERING INFORMATION

Device	Package	Operating Temperature
KS7314	80-QFP-1212	0 ~ +70°C

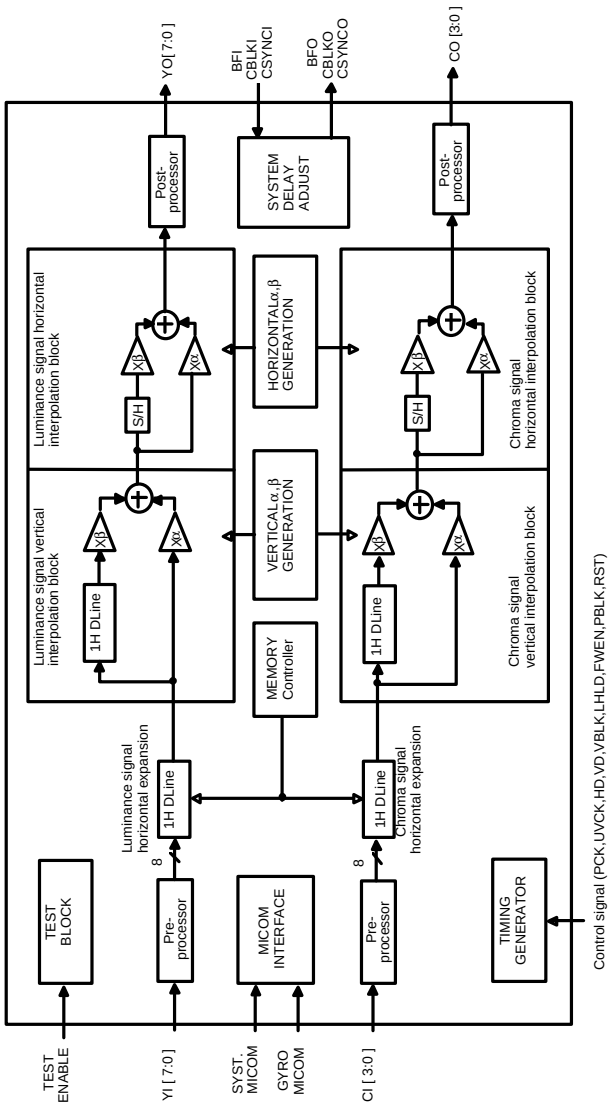
FEATURES

- 256 discrete zoom steps
- Zoom operation withart using field memory
- Vertical image expansion and vertical interpolation by the control of a built-in 2H delay line
- Zoom operation dependent upon Y, R-Y, B-Y signal input (Source Format → 4:1:1)
- Variable zoom ratio technology applicable to horizontal and vertical directions (Styling Effect)
- Correction of wobbling hand by the sub-pixels in vertical direction
- Correction of wobbling hand in horizontal direction
- Provision of special effects such as:
  - Horizontal mirror technology
  - Variable 16 mode mosaic block size technology
    (Mosaic function available in EIS mode)
- Linear interpolation algorithm applied to both luminance and chroma signals in horizontal and vertical directions
- Applicable to wide TV screen with 630,000 pixels
- Applicable to world-wide models, of different systems like NTSC/PAL, HI8/NORMAL, and DVC
- Electronic zoom ratio
  Expansion available upto four times (4×) the maximum, and more in horizontal zooming
- Operable normally at 3.3V, and 5.0 V

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

No	Symbol	I/O	From / To	Description
1	YI0	I	DCP /	Luminance signal input
2	YI1	I	DCP /	Luminance signal input
3	YI2	I	DCP /	Luminance signal input
4	**GND**	**G**	**-**	**Ground**
5	YI3	I	DCP/	Luminance signal input
6	YI4	I	DCP /	Luminance signal input
7	YI5	I	DCP /	Luminance signal input
8	**VDD1**	**P**	**-**	**Power(3.3 V)**
9	YI6	I	DCP/	Luminance signal input
10	YI7	I	DCP /	Luminance signal input
11	YO0	O	DCP /	Luminance signal output
12	YO1	O	DCP /	Luminance signal output
13	**GND**	**G**	**-**	**Ground**
14	YO2	O	DCP/	Luminance signal output
15	YO3	O	DCP /	Luminance signal output
16	YO4	O	DCP /	Luminance signal output
17	**VDD2**	**P**	**-**	**Power(5.0 V)**
18	YO5	O	DCP/	Luminance signal output
19	YO6	O	DCP /	Luminance signal output
20	YO7	O	DCP /	Luminance signal output
21	**GND**	**G**	**-**	**Ground**
22	**GND**	**G**	**-**	**Ground**
23	**GND**	**G**	**-**	**Ground**
24	DZCSYNC1	I	DCP/	CSYNC input for delay adjust
25	DZBFI	I	DCP /	Burst Flag input for delay adjust
26	DZCBLKI	I	DCP /	CBLK input for delay adjust
27	**GND**	**G**	**-**	**Ground**
28	**VDD1**	**P**	**-**	**Power(3.3 V)**
29	DZCSYNCO	O	/ DCP	Delayed CSYNC output
30	DZBFO	O	/ DCP	Delayed BURST FLAG output
31	DZCBLKO	O	/ DCP	Delayed CBLK output

(Continued)

No	Symbol	I/O	FROM / TO	Description
32	**GND**	**G**	**-**	**Ground**
33	**GND**	**G**	**-**	**Ground**
34	DZSCK	I	S.MICOM /	System micom data sampling clock
35	DZSI	I	S.MICOM /	System micom data serial input
36	DZSCSN	I	S.MICOM /	System micom data enable Signal input
37	MUL-TO	O	-	Multiplier test output
38	**VDD1**	**P**	**-**	**Power(3.3 V)**
39	NAND-OUT	O	-	NAND TREE TEST output
40	**GND**	**G**	**-**	**Ground**
41	TEST3	I	-	Test signal input
42	TEST2	I	-	Test signal input
43	TEST1	I	-	Test signal input
44	TEST0	I	-	Test signal input
45	**GND**	**G**	**-**	**Ground**
46	DONE	O	-	Memory bist end signal output
47	ERROR	O	-	Memory bist error signal input
48	BISTON	I	-	Memory bist enable signal input
49	**VDD1**	**P**	**-**	**Power(3.3 V)**
50	**VDD1**	**P**	**-**	**Power(3.3 V)**
51	PCK	I	TGM /	System clock
52	**GND**	**G**	**-**	**Ground**
53	LHLD	I	L	Linememory hold signal input
54	HD	I	TGM /	Horizontal drive pulse input
55	VBLK	I	TGM /	Vertical blank signal input
56	VD	I	TGM /	Vertical drive pulse input
57	FLD	I	TGM /	Field selection signal input
58	**VDD2**	**P**	**-**	**Power(5.0 V)**
59	RST	I	SYSTEM /	System reset signal input
60	PBLK	I	TGM /	Pre-blank Signal input for Linememory Reset
61	PAL	I	-	NTSC/PAL Signal input (PAL : High)
62	FWEN	I	TGM /	Linememory hold signal 1

(Continued)

No	Symbol	I/O	FROM / TO	Description
63	**GND**	**G**	**-**	**Ground**
64	GSCK	I	G.MICOM /	Gyro micom data sampling clock
65	GSI	I	G.MICOM /	Gyro micom data serial input
66	GSCSN	I	G.MICOM /	Gyro micom data enable signal input
67	**VDD1**	**P**	**-**	Power(3.3 V)
68	**GND**	**G**	**-**	**Ground**
69	UVCK	I	DCP /	Clock input for (R.Y)/(B-Y) judgement
70	**GND**	**G**	**-**	**Ground**
71	CI0	I	DCP /	Chroma signal input
72	CI1	I	DCP /	Chroma signal input
73	CI2	I	DCP /	Chroma signal input
74	CI3	I	DCP /	Chroma signal input
75	**VDD1**	**P**	**-**	**Power(3.3 V)**
76	CO0	O	DCP /	Chroma signal output
77	CO1	O	DCP /	Chroma signal output
78	CO2	O	DCP /	Chroma signal output
79	CO3	O	DCP /	Chroma signal output
80	**VDD2**	**P**	**-**	**Power(5.0 V)**

FUNCTIONS OF BLOCKS

Function Block	Function Performed
LUMINANCE HORIZONTAL INTERPOLATION	Interpolates linearly of luminance signal in horizontal direction
LUMINANCE VERTICAL INTERPOLATION	Interpolates linearly of luminance signal in vertical direction
CHROMA HORIZONTAL INTERPOLATION	Interpolates linearly of chroma signal in horizontal direction
CHROMA VERTICAL INTERPOLATION	Interpolates linearly of chroma signal in vertical direction
HORIZONTAL COEFFICIENT GENERATION	Generates the horizontal interpolation coefficient for luminance and chroma signals
VERTICAL COEFFICIENT GENERATION	Generates EVEN/ODD field vertical interpolation coefficient for luminance and chroma signals
LINE MEMORY CONTROLLER	Generates READ/WRITE ADDRESS for 1H DELAY LINE for horizontal image expansion and 1H delay line for vertical interpolation
TIMING GENERATION	Generates time signals for controls
MICOM INTERFACE	Decodes zoom/DVC/Special Effect mode
GYRO MICOM INTERFACE	Decodes wobbling hand correction level signal

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 ~ +7.0	V
Input voltage	V_I	-0.3 ~ VDD+0.3	V
Output voltage	V_O	-0.3 ~ VDD+0.3	V
Storage temperature	T_{STG}	-40 ~ +125	°C
Operating temperature	T_{OPR}	0 ~ +70	°C
Latch-up current	I_{LU}	100	mA

ELECTRICAL CHARACTERISTICS

DC

(T_{OPR} = 0 ~ +70°C)

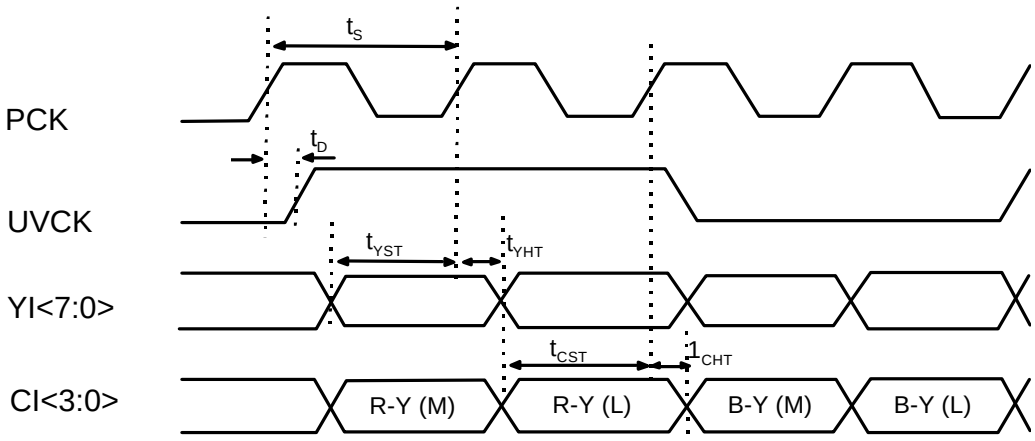
Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage for Internal	V_{DD1}	3.1	3.3	3.5	V
Operating voltage for I/O cell	V_{DD2}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	$0.7V_{DD2}$	-	-	V
Input low voltage	V_{IL}	-		$0.3V_{DD2}$	V
Operating current	I_{DD}	-	-	100	mA
Standby current	I_{DS}	-	-	1	mA
Output high voltage (IOH = -1mA)	V_{OH}	2.4	-	-	V
Output low voltage (IOL = 1mA)	V_{OL}	-	-	0.4	V
Input high leakage current(V_I = 0 ~ V_{DD})	I_{IH}	-10	-	+10	μA
Input low leakage current(V_I = 0 ~ V_{DD})	I_{IL}	-10	-	+10	μA

***** VDD1 : Pin No 8, 28, 38, 49, 50, 67, 75
VDD2 : Pin No 17, 58, 80

AC

(T_{OPR} = 0 ~ +70°C, ts = 100 ns)

Characteristics	Symbol	Min	Typ	Max	Unit
YI Data setup time	t_{YST}	25	-	-	ns
YI Data hold time	t_{YHT}	10	-	-	
CI Data setup time	t_{CST}	25	-	-	
CI Data hold time	t_{CHT}	10	-	-	
UVCK clock delay time	t_D	10	-	35	

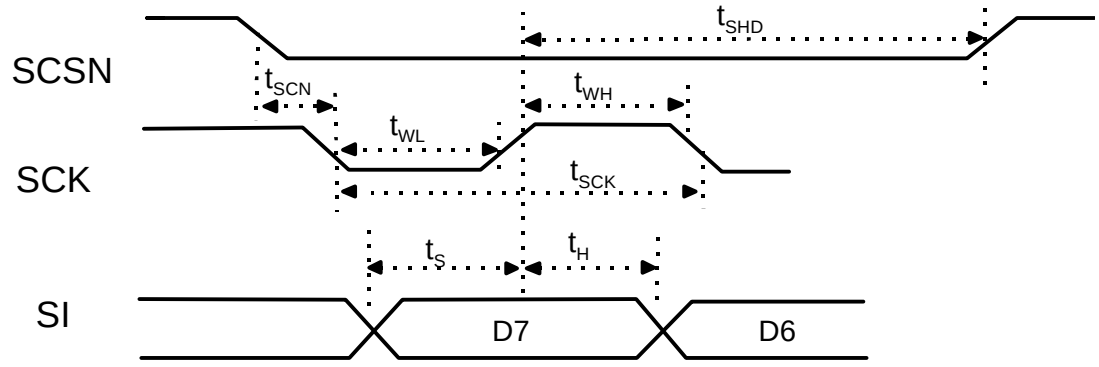


MICOM INTERFACE

1. NEC SYSTEM MICOM INTERFACE (μPD78014)

Serial Port Timing Characteristics (f_{CLK} = 12 MH_Z)

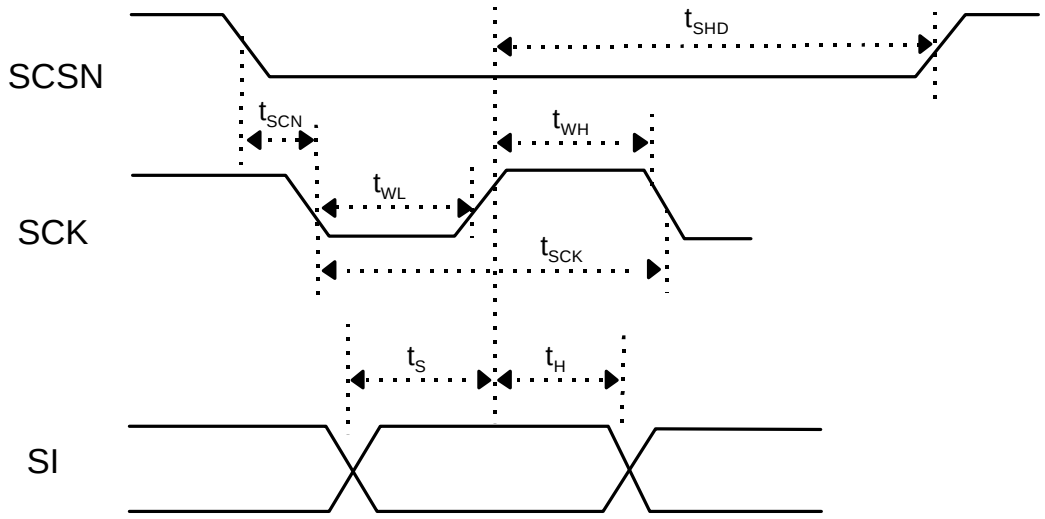
Characteristics	Symbol	Min	Typ	Max	Unit
Serial port clock cycle time	t_{SCK}	1300	-	-	ns
Serial port clock high, low width	t_{WH}, t_{WL}	556	-	-	
Input data setup to clock rising edge	t_S	30	-	-	
Input data hold after clock rising edge	t_H	30	-	-	
SCSN setup time	t_{SCN}	30			
SCSN hold time	t_{SHD}	30			



<Serial I/O Timing Diagram>

2.GYRO MICOM INTERFACE(CXD81120)

Characteristics	Symbol	Min	Typ	Max	Unit
Serial port clock cycle time	t_{SCK}	2000	-	-	ns
Input data setup to clock rising edge	t_S	30	-	-	
Input data hold after clock rising edge	t	30	-	-	
Serial port clock high, low width	t_{WH}, t_{WL}	700	-	-	
SCSN Setup Time	t_{SCN}	30	-	-	
SCSN Hold Time	t_{SHD}	30	-	-	



<Serial I/O Timing Diagram>

SYSTEM CONFIGURATION AND OPERATION

(Implementation of 2nd generation electronic zoom)

1. System block configuration I (EIS+D.Zoom + Spec. Effect)

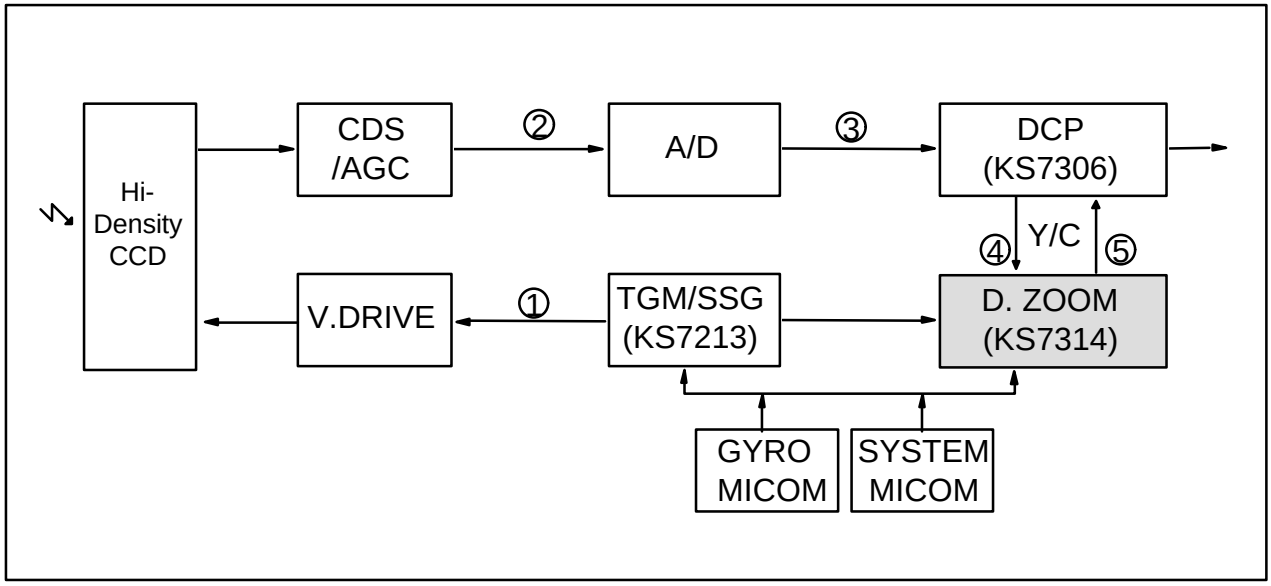


Fig.1 2nd generation EIS/Electronic zoom applied camcorder camera system

The 2nd generation electronic zoom which enlarges images without using field memory, performs the electronic zooming process by means of image extension first, and then by signal interpolation.

In the 1st process of image zooming, the vertical zooming is accomplished by the control of image data read-out pulse from CCD. The generation of CCD read-out pulse is accomplished at TGM(KS7213) with the input of electronic zooming ratio data supplied from the System Micom.

The image being vertically extended for the electronic zooming is fed to DCP(KS7306) in its form of an image extended only vertically.

At the DCP(KS7306), image interpolation for the vertically zoomed image by NNI is first performed according to the line hold signal.

This is the process of removing blank data existing in between lines of a vertically zoomed image.

The image data is first interpolated at the fed to the electronic zoom (KS7314).

The image input separated in luminance and chroma signals snaped in a 4:1:1 formation from the fed to the DCP is then processed for horizontal extension within the electronic zoom for the horizontal zooming. Horizontal extension is accomplished through the address control of line memory self-contained in the electronic zoom processor.

The image data of the horizontally extended is interpolated in vertical and horizontal directions by the inner-interpolation function of the electronic zoom processor. The discussion so far relates the functional process of the electronic zoom. The hand wobble correction is accomplished in the following manner. The hand wobble data of the camcorder detected by the gyro-sensor and the gyro-micom are fed to TGM for vertical compensation by lines. The vertical compensation is performed by the control of CCD read out pulse supplied by TGM. The image data compensated for vertical agitation by lines is then fed to the electronic zoom througn DCP to perform horizontal correction of hand wobble through the use of the line memories for horizontal extension within the electronic zoom. In other words, the correction of horizontal hand wobble is implemented by pixels with the use of read address of the line memories. The correction of hand wobble in vertical and horizontal detailed to sub-pixels is reflected in the creation of interpolation coefficient with which the interpolation is implemented.

For horizontal wobble correction, a fixed ratio of electronic zooming needs to be maintained in the electronic zoom, and for vertical wobble correction, employment of a high density CCD is required. The threshold for the correction of hand wobble is dependent upon the number of effective lines of the high density CCD and the horizontal zoom ratio of the electronic zoom.

2. System block configuration II (electronic zoom and special effect blocks)

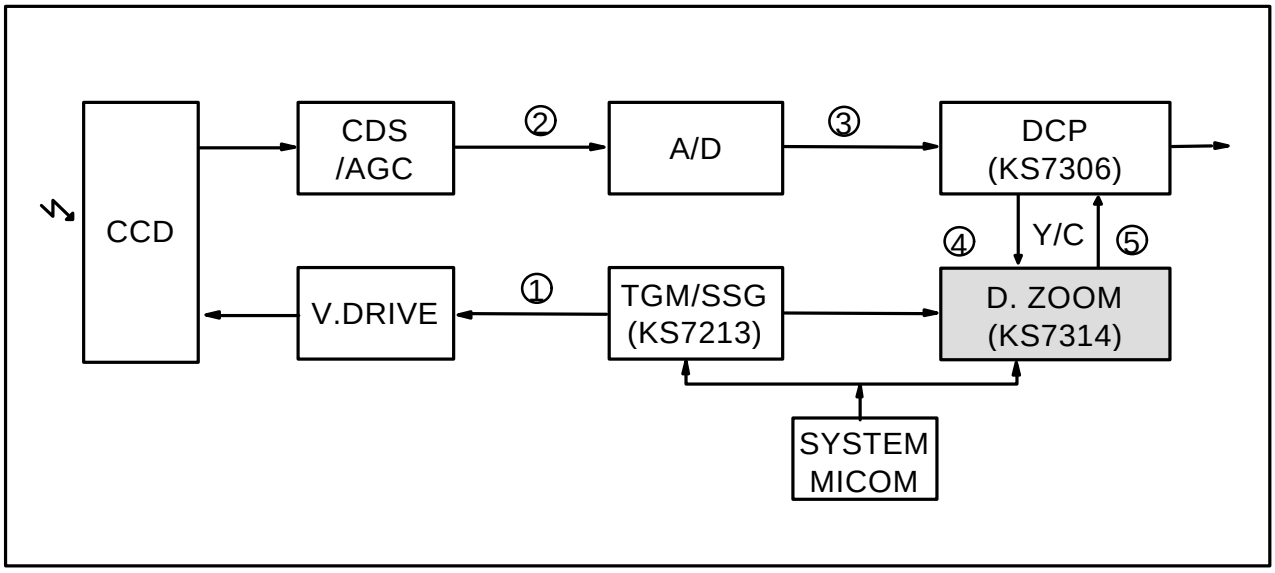


Fig. 2 Camcorder camera system of electronic zoom 2nd generation application

Fig. 2 above illustrates a camcorder a camera system with an electronic zoom function. The difference between the above system to the camcorder camera system with electronic zoom and hand wobble correction function is that, the former does not, for the attainment of image stability, employ high density CCD intended for the vertical correction of hand wobble. The signal process system explained below and electronic zoom signal process system are identical to the one illustrated in Fig.1. As for this camcorder camera system, it is important that all aspects of signal procesing must go through the electronic zoom process (KS7314) since the repetition of the KS7314 chip enable/disable occuring every time the electronic zoom turns to on/off would entail screen shift of the image. So to speak, the screen shift occurs just as much as the electronic zoom processing is delayed develops. In order to compensate for the electronic zoom system, the video data is delayed to match, the processing delay of electronic zoom, using the synchronizing signal (burst flag, CBLK or CSYNC), and is then passed to the signal processor (KS7306). The special effect is implemented in the following manner. The special effects data in serial format, supplied from the system micom, is first converted to parallel format. The mirror effect in horizontal direction and the mosaic effect in vertical direction are implemented, controlled by the read address of line memories for horizontal expansion. The read/write enable signal while the mosaic effect in horizontal direction is achieved by the conversion of sampling frequency against the fully interpolated image data. In particular, the mosaic effect can also be achieved in EIS mode.

3. EIS / System micom interface

EIS MICOM INTERFACE		TO	Remarks
Level of horizontal hand whole	INTEGER	Digital Zoom (KS7314)	2′s Complement
	SUB-PIXEL OFFSET	Digital Zoom (KS7314)	2′s Complement
Level of vertical hand whole	INTEGER	TGM (KS7213)	2′s Complement
	SUB-PIXEL	TGM (KS7213)	2′s Complement
	SUB-PIXEL OFSET	Digital Zoom (KS7314)	Positive only

Table 1. EIS micom interface

SYSTEM MICOM INTERFACE		TO	Remarks
Horizontal zoom Start Point	INTEGER	Digital Zoom (KS7314)	LINEMEMORY READ ADDRESS to decide
	SUB-PIXEL OFFSET	Digital Zoom (KS7314)	Entered into horizontal interpolation coefficient part
Horizontal electronic zoom		Digital Zoom (KS7314)	Entered into horizontal interpolation coefficient part
Vertical zoom Start Point	INTEGER	TGM (KS7213)	CCD LINE SKIP to decide
	SUB-PIXEL OFFSET	TGM (KS7213) Digital ZOOM(KS7314)	Entered into vertical interpolation coefficient part
Vertical electronic zoom RATIO INVERSE		TGM (KS7213) Digital Zoom(KS7314)	Generate line hold signal Vertical coefficient part

Table 2. SYSTEM MICOM INTERFACE

Tables 1 and 2 summarize the interfacing data formats of the EIS micom (Gyro micom) and the system micom respectively. In the EIS micom interfacing of Table 1, the data for horizontal hand tremble is supplied to KS7314. The default line skip level and vertical hand tremble level are not computed by EIS micom, but the line skip is determined finally by KS7213 after the operation of vertical hand tremble level data entries taken in the form of 2's complement. The vertical sub-pixel hand tremble level data are, however, converted to positive value before they are entered. In the system micom interfacing of Table 2, the start point data of horizontal/vertical electronic zooming are computed by the following formulae and then transmitted to KS7314 and KS7213.

Electronic zoom start point = Width(or Height) * (1-(1/Zoom Ratio))/2

= Width(or Height) * (Elec. Zoom Step)/(2*256)

where width or height represent the value of effective pixels of CCD and in case the high density CCD and FCM of the EIS application are used, they then represent effective line output of high density CCD and effective pixel number respectively. The figure 256 standing in above formulae explains that each of pixel is devided in 256 parts for the electronic zooming. The electronic zoom ratio data are generated in the form of electronic zoom step for the horizontal element and electronic zoom ratio inverse for the vertical element.

4. KS7314 input video data format

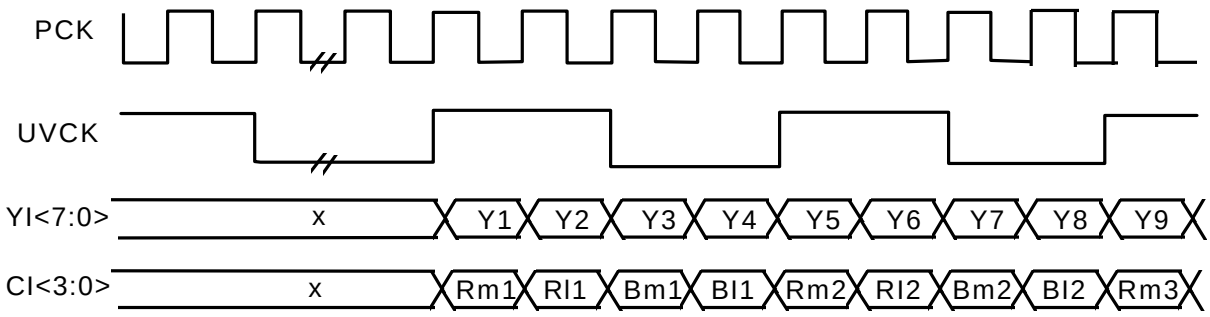
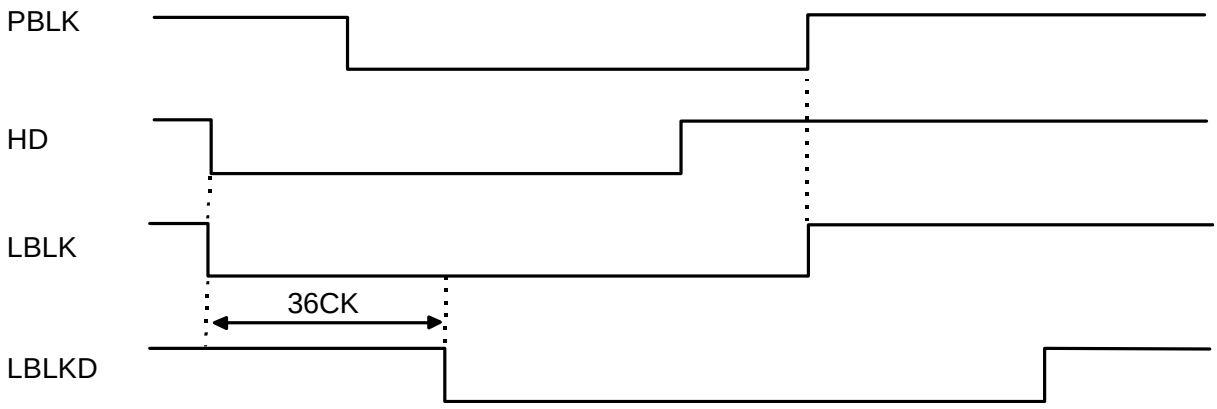


Fig. 3 Electronic zoom input video data format(4:1:1)

Fig. 3 illustrates the video data format input to KS7314, fed from KS7306. The Luminance and chroma D Data are in the 4:1:1 format, and the chroma data is entered in sequence of (R-Y) LSB, (B-Y) MSB, and (B-Y) LSB. The UVCH signal distinguishs R-Y from B-Y. The LBLKO is the signal used to reset the counter during the process of generating the READ/WRITE address of the line memory. The duration in which LBKO is at high level is the effective pixel section. KS7314 generates LBLK signal that is used as the counter reset signal of line memory address self-contained in the line memory address of KS7314. Considering that 28CK is developed while processing the effective data of KS7306, LBLK is delayed to create LBLKD for use as a reset signal of the line memory counter.

The chroma input of 4 formation is restructered to 8 bit signal before the application to the interpolation.

5. Line memory reset signal (LBLK) generation



6. Vertical interpolation

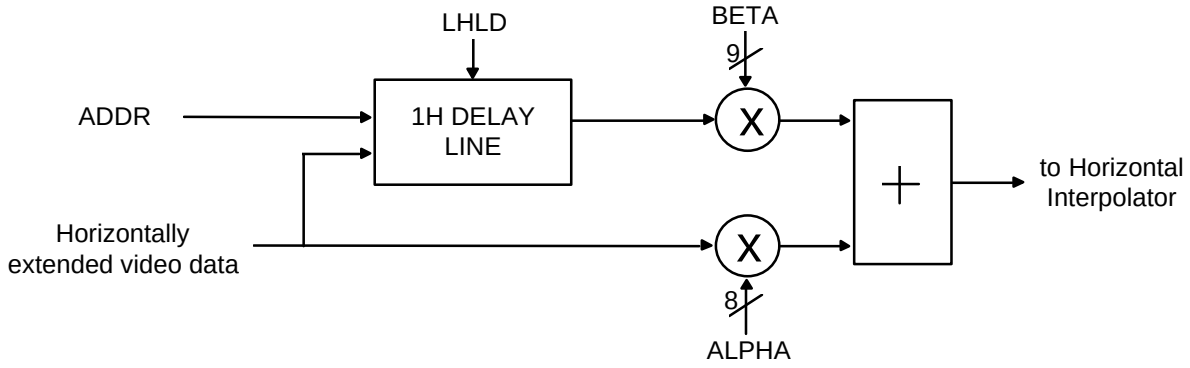


Fig. 4-1 Vertical interpolation circuit

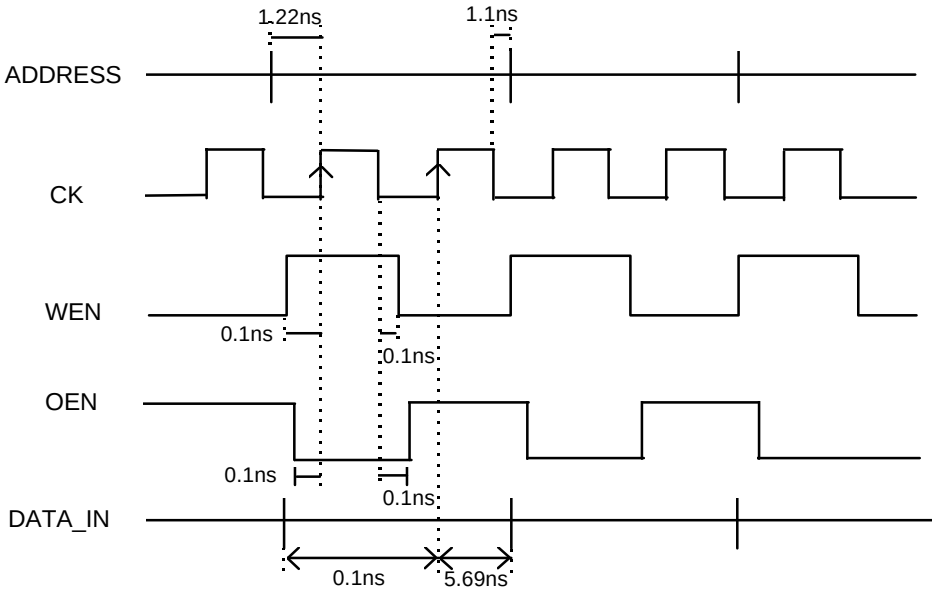


Fig. 4-2 H delay line timing specification for vertical interpolation application

Fig. 4-1 is the vertical interpolating circuit applicable to both luminance and chroma signals. The vertical video input data for the vertical interpolator is readily processed for horizontal video extension, using the linememory at the former stage of luminance and the chroma signal horizontal extender. In the vertical interpolation block, the interpolation coefficients Alpha and Beta, generated by the vertical interpolating coefficient generator, are applied in the interpolation operation.

Fig. 4-2 dipicts 1H delay line timing specification applied to vertical interpolation. The function of READ and WRITE is performed in the method of READ first and WRITE second, in 2 cycles of the linememory clock. The AC timing above should be regarded as the minimum.

7. Horizontal interpolation procedure

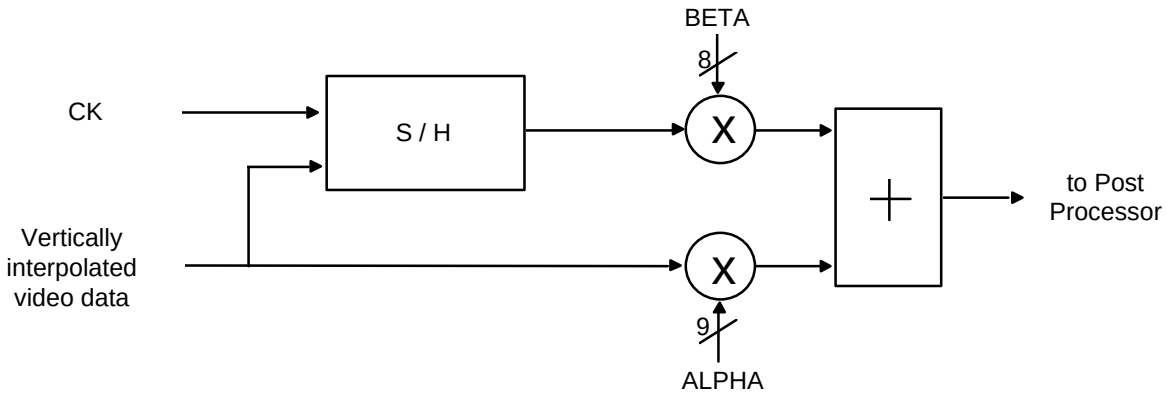


Fig. 5 Luminance signal horizontal interpolation circuit

Prior to the horizontal interpolation process, the video data are extended at the horizontal extension and passed to the vertical interpolation part for the vertical process and then entered into the horizontal interpolation part. The horizontal interpolation part is configured of the luminance data horizontal interpolation part and the the chroma data horizontal interpolation part.

The chroma data and are entered R-Y and B-Y components alternatively, so that the data are interpolated separately by the components before they are put to liner interpolation process.

8. Generation of interpolating coefficient

1) Generation of horizontal interpolating coefficient

Data (zrd) supplied by micom	Interpol. Coeff.(α)	Interpol. Coeff.(β)	Zooming ratio(256/(256-ZRD))	Zoom Step.
00000000	1	0	x1	0
00000001	255/256	1/256	256/255	1
:	:	:	:	:
10000000	128/256	128/256	x2	128
:	:	:	:	:
11000000	64/256	192/256	x4	192

Table 3. Zoom ratio data(horizontal) supplied by the system micom

Motion vector decimal	Interpolation coeff. (α)	Interpolation coeff. (β)
0.75 (11000000)	192/256	64/256
0.5 (10000000)	128/256	128/256
0.25 (01000000)	64/256	192/256
0 (00000000)	1	0

Table 4. Relation of EIS micom output decimals of horizontal hand tremble level to interpolation coefficient

Table 3 Illustrates the system micom transmission data(ZRD) for generating the horizontal interpolating coefficient for electronic zooming.

Table 4 Illustrates the EIS micom transmission data for generating the interpolating coefficient for decimal level correction of hand trembles.

2) Generation of vertical interpolation coefficient

Table 5. Zoom ratio inverse data(vertical) transmitted by system micom

Micom supplied data(ZMIV)	Interpolating coefficient(α)	Interpolating coefficient(β)	Zoom ratio (256/ZMIV)	ZOOM STEP
00000000	0	1	X1	0
11111111	255/256	1/256	256/255	1
:	:	:	:	:
10000000	128/256	128/256	X2	128
:	:	:	:	:
01000000	64/256	192/256	X4	192

Table 6. An example of generating vertical interpolating coefficient based on zoom ratio data

Zoom ratio data(ZMIV)	Interpolating coefficient(α)	Interpolating coefficient(β)
0	0, 0, 0, 0, 0, . . .	1, 1, 1, 1, 1, . . .
255	0, 255/256, 254/256, 253/256, 252/256, . .	1, 1/256, 2/256, 3/256, 4/256, . .
254	0, 254/256, 252/256, 250/256, 248/256,. .	1, 2/256, 4/256, 6/256, 8/256, . .
:	:	:
128	0, 128/256, 0, 128/256, 0, . . .	1, 128/256, 1, 128/256, 1, . .
:	:	:
64	0, 64/256, 128/256, 192/256, 0, . .	1, 192/256, 128/256, 64/256, 1, . .

The data entered to the vertical interpolating coefficient generation part consist of zoom ratio inverse data, and vertical sub-pixel hand tremble data, supplied from the EIS micom. The vertical interpolating coefficient is generated, based on the above data.

The vertical sub-pixel hand tremble data supplied by the EIS micom would look identical to that shown in Table 4 above. The vertical interpolating coefficient applies equally to luminance and chroma.

The vertical interpolating coefficients α and β responding to specific zoom ratio are tabulated in Table 6 above. Upon the entry of zoom ratio data, interpolation coefficient α, interpolation coefficient β are generated.

The interpolation coefficients shown on Table 3 are generated continuously, and then the zooming process is implemented after a separate operation of the coefficient and the pixel data, entered in the zoom processor.

9. Special effect I (Horizontal mirror effect)

Horizontal mirror effect is termed after the fact that the function offers symmetrical images siding by the upright axis in the center of screen, just like a mirror reflection. The effect is achieved by the control of the Read Address of 1H delay line, used in the horizontal expansion of luminance and hue signals inside the zoom processor. The function is implemented by means of counting the number of effective pixels in the image input to KS7314, assigning half the count as the horizontal mirror point, and then performing control up/down of the read address counter when read address is generated.

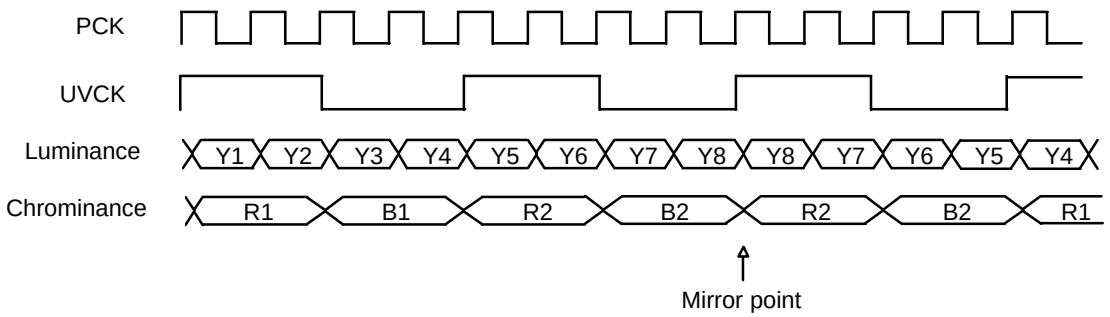


Fig. 6 Mirror read address timing diagram

10. Special effect II (Style)

The function allows image expansion in horizontal or vertical direction, independently from each other. The supply of zoom ratio data from the micom, separated in horizontal and vertical directions, enables to stage such effect of an image.

In case the zoom ratio data from the micom specify 2 power in horizontal, and single power in vertical direction, the zoom processor needs to perform interpolation only in horizontal direction. In this way, an image of different magnification, either in the horizontal or the vertical, independently from each other, is obtainable. The application of zoom ratio data, separated in directions supplied by the micom to the circuit of the zoom processor where the horizontal and vertical interpolating coefficients are gernerated, can implement the special effect function easily.

11. Special effect III (Mosaic)

The mosaic function offers the user an ability to form a blocked area of a set size on screen, to display the image with an obscure outline. The room processor supports a mosic effect implemented in block sizes of 4×4, 8×8, 12×12, 16×16, . . . 60×60, 64×64, making 16 sizes altogether. To obtain the mosaic effect, first decide on the mosaic size and then fill out the block with uniform pixel value for every pixel in the block. The process should be performed according to luminance and chroma signals separately. As for the process of luminance signal, in order to maintain uniform brightness of pixels, take the value of the uppermost-left pixel of the block as the representative value, and then replace all the rest of the pixel values in the block. For the process of replacing all the pixel values with the representative value, first adapt the system clock to conform to the selected mosaic mode by means of demultiplying the clock by 4, 8, . . . 64, and use this demultiplied clock as the mosaic clock. The case of chroma signal is fairly complicated. Since the chroma signal alternates R-Y to B-Y by the clock, the luminance method can not be directly applied and that the adjustment of the mosaic clock is necessary to maintain R-Y and B-Y chroma components. The replacement of a vertical pixel value with the representative value can be achieved by the read/write enable control of 1H delay line, applied in horizontal expansion. In the vertical signal process for a mosaic, attention is invited to the fact that the standard TV screen comes separated in even and odd fields by interlaced scanning. Signal process only in a half of that required in the horizontal process would be sufficient.

For example, in an 8×8 mosaic mode, only 4 lines of mosaic video process vertical will display a square mosaic block on screen.

In the same manner, the mosaic process of luminance and chroma signals in vertical direction can be performed. In case of a vertical mosaic, the system delay in vertical direction may vary, depending on the type of camcorder usage. That user may, in case of a vertical mosaic operation, take the dummy data of black level appearing on the top side of the screen for the initial mosaic start line, and a symptom, in which the black level on the top side would grow as the mosaic block size grows, may develop. The system micom is, therefore, designed to be capable of controlling the vertical mosaic start line in order to avoid such symptoms. The mosaic function is enabled in EIS electronic image stabilizer mode of operation.

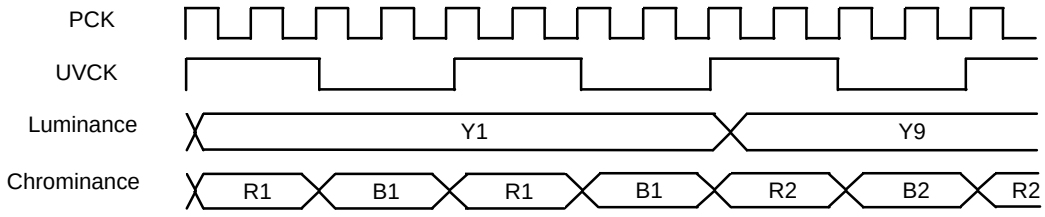


Fig. 7 Horizontal mosaic timing diagram (8×8 mosaic)

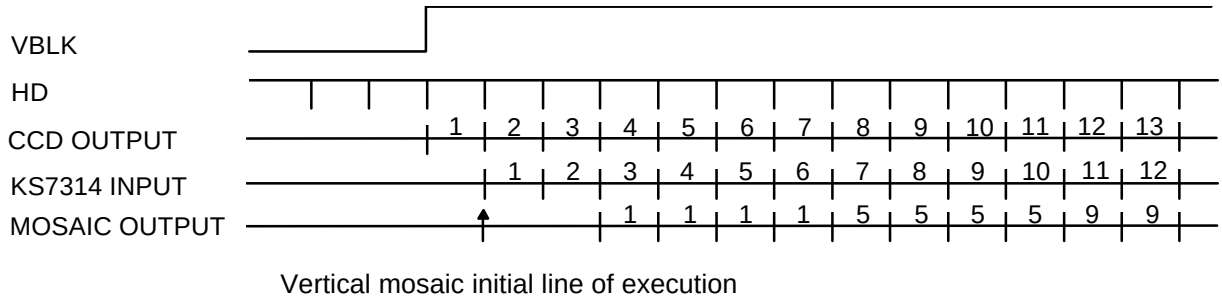


Fig. 8 Vertical mosaic timing diagram (8×8 mosaic)

12. Digital video interface

KS7314 has a built-in DVC interface for application to digital video camcorders. In other words, the luminance and chroma signal output of KS7314 can be used as an input to DVC encorder, without the need of transmitting the output to KS7306, which is the signal processor. For this purpose, it is able to adjust chroma signal timing in DVC mode against luminance signal and synchronization signal ± 8CK by the system clock unit. KS7314 takes the input of the DVC mode recognition signal and the delay adjustment value for the chroma signal from the micom.

13. Delay adjust

The processing delay developed in the process of electronic zooming should be compensated, and the compensation can be achieved by delaying the signals related to active display of image, equal to the electronic zoom processing delay. Namely, the input of signals CBLK, CSYNC, and CBF from the digital camera processor(DCP) is taken to process and then entered back to DCP. The vertical delay is not adjusted particulary in the electronic zoom process, now that PBLK is used in DCP as the line memory reset. The signal gets readily processed before the image effective pixel process and thus vertical delay is not considered. The electronic zoom processing delay lasts 20 system clock in total and it develops to 28 system clock for KS7314 in DVC mode.

REGISTER TABLE

1. Micom command register

REG. Name: COMMAND (HEADER)

REGISTER DESCRIPTION

COMMAND REGISTER (HEADER)

7					0
DZ	EIS	EFCT	VADJ	HADJ	DVC

MODE)

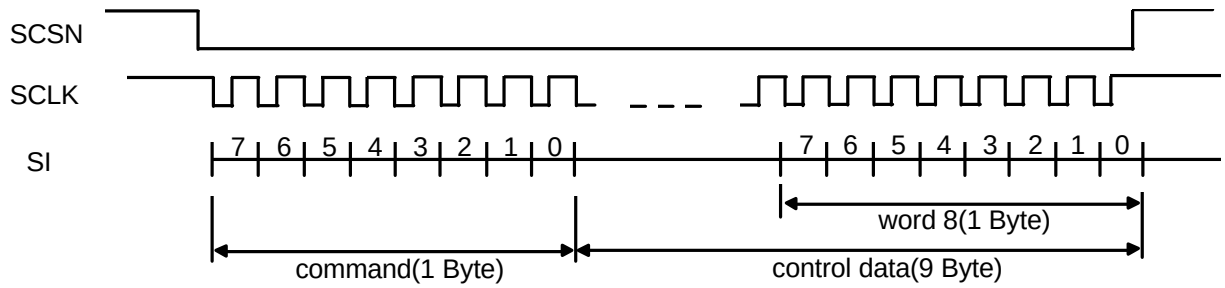
DZ	MODE	EIS	MODE	EFCT	MODE
0	DZ OFF	0	EIS OFF	0	EFFECT OFF
1	D.ZOOM	1	EIS ON	1	EFFECET ON

VADJ	MODE	HADJ	MODE
0 0	2 H DELAY	0 0	32 CK DELAY
0 1	3 H DELAY	0 1	36 CK DELAY
1 0	4 H DELAY	1 0	40 CK DELAY
1 1	5 H DELAY	1 1	44 CK DELAY

DVC	MODE
0	NORMAL ZOOM
1	ZOOM for DVC

notes) VADJ : VBLK DELAY ADJUST
HADJ : LBLK DEALY ADJUST
Possible synchronous realization of Mosaic and EIS
Impossible synchronous realization of Mirror and D.Zoom

Note) System micom interface timing



2. System Micom Register Table

1) Zoom register table

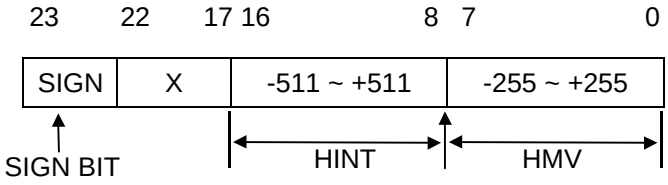
<table>
<tr><th></th><th>REG. Name</th><th>REGISTER DESCRIPTION</th></tr>
<tr><td>WORD 0</td><td>HZOOM (ZRD)</td><td>HORIZONTAL ZOOM STEP. (0 ~ 192 : X 1 ~ X 4)</td></tr>
<tr><td>WORD 1</td><td>VZOOM (ZMIV)</td><td>VERTICAL ZOOM STEP. (256 ~ 64 : X 1 ~ X 4)</td></tr>
<tr><td>WORD 2
WORD 3</td><td>HSP</td><td>HORIZONTAL START READ ADDRESS.(16 BIT)
15 9 8 0
<table><tr><td>0</td><td>0 ~ 511</td></tr></table></td></tr>
<tr><td>WORD 4</td><td>HSUB</td><td>HORIZONTAL ZOOM START SUB PIXEL. (0 ~ 255)</td></tr>
<tr><td>WORD 5</td><td>VOFFO</td><td>VERTICAL ZOOM START SUB PIXEL ODD FIELD (0~255)</td></tr>
<tr><td>WORD 6</td><td>VOFFE</td><td>VERTICAL ZOOM START SUB PIXEL EVEN FIELD (0~255)</td></tr>
<tr><td>WORD 7</td><td>DVC_DLY</td><td>DELAY ADJUST(2′s COMPLEMENT) for DVC
7 0
<table><tr><td>SIGN</td><td>X</td><td>X</td><td>X</td><td>DL3</td><td>DL2</td><td>DL1</td><td>DL0</td></tr></table><table><tr><th>SIGN</th><th>DL3 DL2 DL1 DL0</th><th>MODE</th></tr><tr><td>0</td><td>0000</td><td>0 PCK DELAY</td></tr><tr><td>0</td><td>0001</td><td>+1 PCK DELAY</td></tr><tr><td>0</td><td>0010</td><td>+2 PCK DELAY</td></tr><tr><td>0</td><td>0011</td><td>+3 PCK DELAY</td></tr><tr><td>0</td><td>0100</td><td>+4 PCK DELAY</td></tr><tr><td>0</td><td>0101</td><td>+5 PCK DELAY</td></tr><tr><td>0</td><td>0110</td><td>+6 PCK DELAY</td></tr><tr><td>0</td><td>0111</td><td>+7 PCK DELAY</td></tr><tr><td>0</td><td>1000</td><td>+8 PCK DELAY</td></tr><tr><td>1</td><td>1000</td><td>-8 PCK DELAY</td></tr><tr><td>1</td><td>1001</td><td>-7 PCK DELAY</td></tr><tr><td>1</td><td>1010</td><td>-6 PCK DELAY</td></tr><tr><td>1</td><td>1011</td><td>-5 PCK DELAY</td></tr><tr><td>1</td><td>1100</td><td>-4 PCK DELAY</td></tr><tr><td>1</td><td>1101</td><td>-3 PCK DELAY</td></tr><tr><td>1</td><td>1110</td><td>-2 PCK DELAY</td></tr><tr><td>1</td><td>1111</td><td>-1 PCK DELAY</td></tr></table></td></tr>
</table>

2) Effect register table

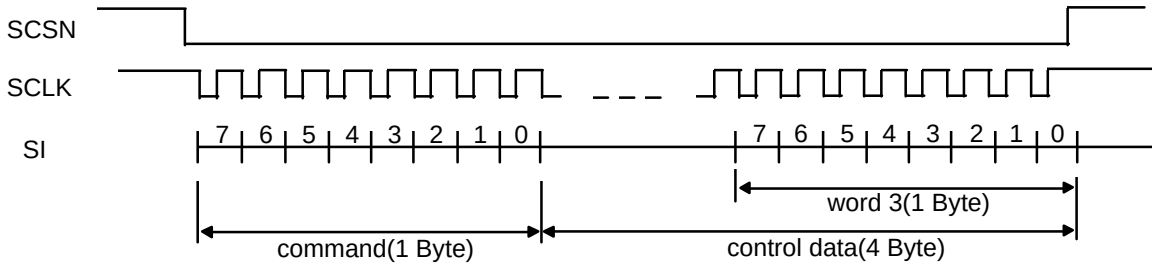
<table>
<tr><th></th><th>REG. Name</th><th>REGISTER DESCRIPTION</th></tr>
<tr><td>WORD 8</td><td>EFFECT</td><td>
<table>
<tr><td>7</td><td>6</td><td>0</td></tr>
<tr><td>MIRROR</td><td colspan="2">MOSAIC</td></tr>
</table>
MODE)
<table>
<tr><th>VALUE</th><th>MODE</th></tr>
<tr><td>0</td><td>MOSAIC OFF</td></tr>
<tr><td>4</td><td>4 X 4 MOSAIC</td></tr>
<tr><td>8</td><td>8 X 8 MOSAIC</td></tr>
<tr><td>12</td><td>12 X 12 MOSAIC</td></tr>
<tr><td>16</td><td>16 X 16 MOSAIC</td></tr>
<tr><td>. . .</td><td>. . .</td></tr>
<tr><td>60</td><td>60 X 60 MOSAIC</td></tr>
<tr><td>64</td><td>64 X 64 MOSAIC</td></tr>
<tr><td>128</td><td>Horizontal MIRROR</td></tr>
</table>
</td></tr>
</table>

COMMAND REGISTER	CONTROL DATA REGISTER
1 1 1 X X X X 0	D.ZOOM / EIS / MOSAIC ON (Non-DVC Mode)
0 0 1 X X X X 0	EFFECT ON (MIRROR /MOSAIC) (Non-DVC Mode)
0 1 0 X X X X 0	EIS ON (Non-DVC Mode)
1 0 0 X X X X 0	D.ZOOM ON (Non-DVC Mode)
1 1 0 X X X X 0	D.ZOOM / EIS ON (Non-DVC Mode)
1 1 1 X X X X 1	D.ZOOM / EIS / MOSAIC ON (DVC Mode)
0 0 1 X X X X 1	EFFECT ON (MIRROR / MOSAIC) (DVC Mode)
0 1 0 X X X X 1	EIS ON (DVC Mode)
1 0 0 X X X X 1	D.ZOOM ON (DVC Mode)
1 1 0 X X X X 1	D.ZOOM / EIS ON (DVC Mode)

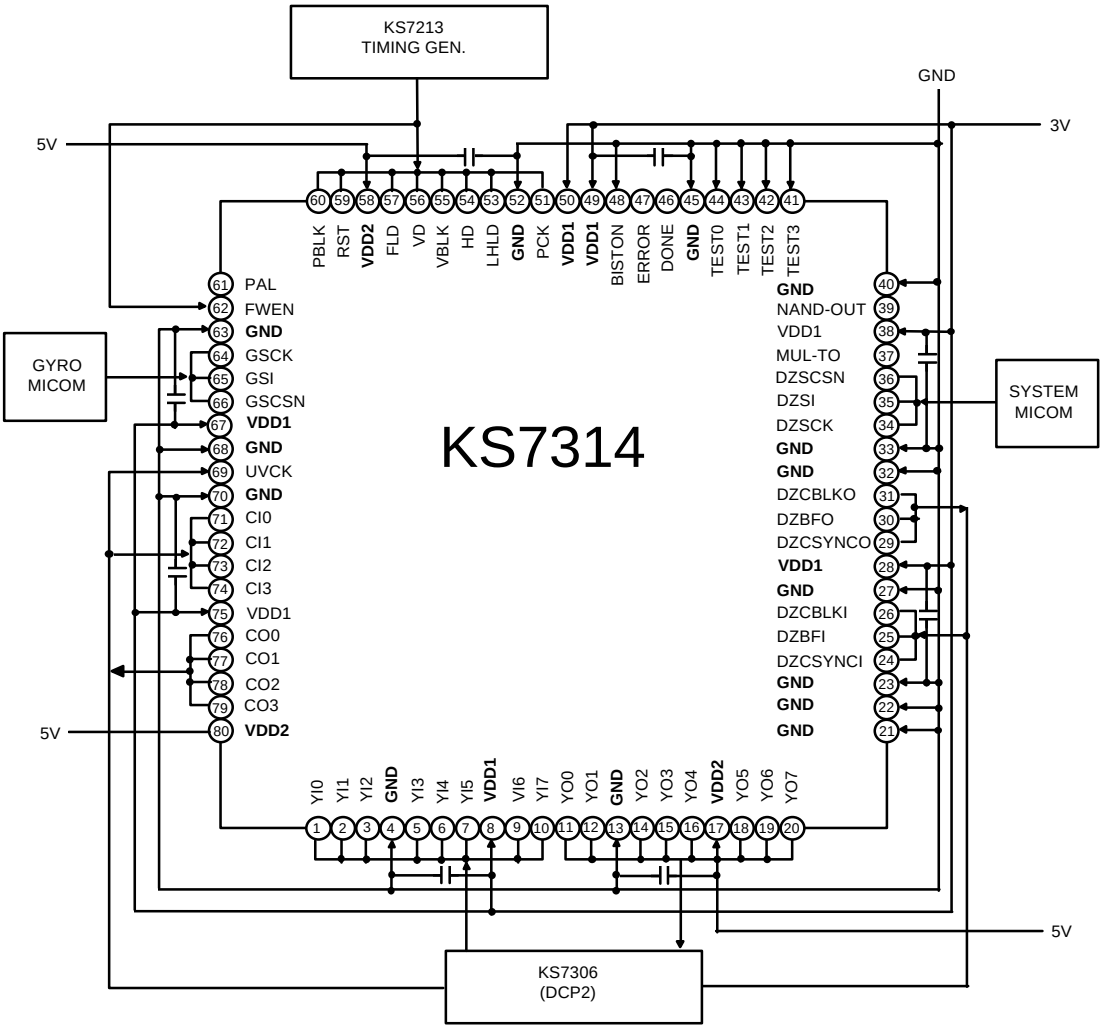
3. Gyro micom register table (2¢s complement)

	REG. Name	REGISTER DESCRIPTION
WORD1 WORD2 WORD3	HINT HMV	HINT(9BIT) : HORIZONTAL MOTION VECTOR(2's COMPLEMENT INTEGER) HMV(8BIT) : HORIZONTAL MOTION VECTOR(2's COMPLEMENT SUB-PIXEL)  MSB 1 bit is the sign bit and relates to the integrals and the decimals both.
WORD 4	VMV	VERTICAL MOTION VECTIO SUB-PIXEL. (0 ~ 255)

Note) Gyro micom interface timing



APPLICATION CIRCUIT



PACKAGE DIMENSIONS

80 - QFP - 1212

unit: mm