KS57C3108
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C3108 single-chip CMOS microcontroller has been designed for very high performance using Samsung's newest 4-bit CPU core, SAM4 (Samsung Arrangeable Microcontrollers). With an up-to-14-digit LCD direct drive capability, a 4-channel A/D converter, 8-bit timer/counter, and PLL frequency synthesizer, the KS57C3108 offers you an excellent design solution for a wide variety of DTS applications.

Up to 40 pins of the 80-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the KS57C3108's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

FEATURES

Memory

- 512 × 4-bit RAM
- 8,192 × 8-bit ROM

56 I/O pins

- Input only: 4 pins
- Output only: 28 pins
- I/O: 24 pins

LCD Controller/Driver

- Maximum 14-digit LCD direct drive capability
- 28 segments × 4 common signals
- Display modes: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-bit Basic Timer

- 4 interval timer functions

8-bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Serial I/O interface clock generator

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32768 Hz
- 4 frequency outputs to BUZ pin
- Clock source generation for LCD

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

A/D Converter

- 4 channels with 8-bit resolution
- 17.8 µs conversion speed at 4.5 MHz

Bit Sequential Carrier

- Support 16-bit serial data transfer in arbitrary format

PLL Frequency Synthesizer

- Level = 300 mVp-p (min)
- AMVCO range = 0.1 MHz to 30 MHz
- FMVCO range = 30 MHz to 150 MHz

16-Bit Intermediate Frequency (If) Counter

- Level = 300 mVp-p (min)
- AMIF range = 100 kHz to 1.0 MHz
- FMIF range = 5 MHz to 15 MHz

Interrupts

- Four internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Four Power-Down Modes

- Idle: Only CPU clock stops
- Stop 1: Main system clock stops
- Stop 2: Main and subsystem clocks stop
- CE low: PLL stops

Oscillation Sources

- Crystal, ceramic, main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 4.5 MHz
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.9, 1.8, 14.2 µs at 4.5 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V (4.0 V to 6.0 V in PLL mode)

Package Type

- 80-pin QFP

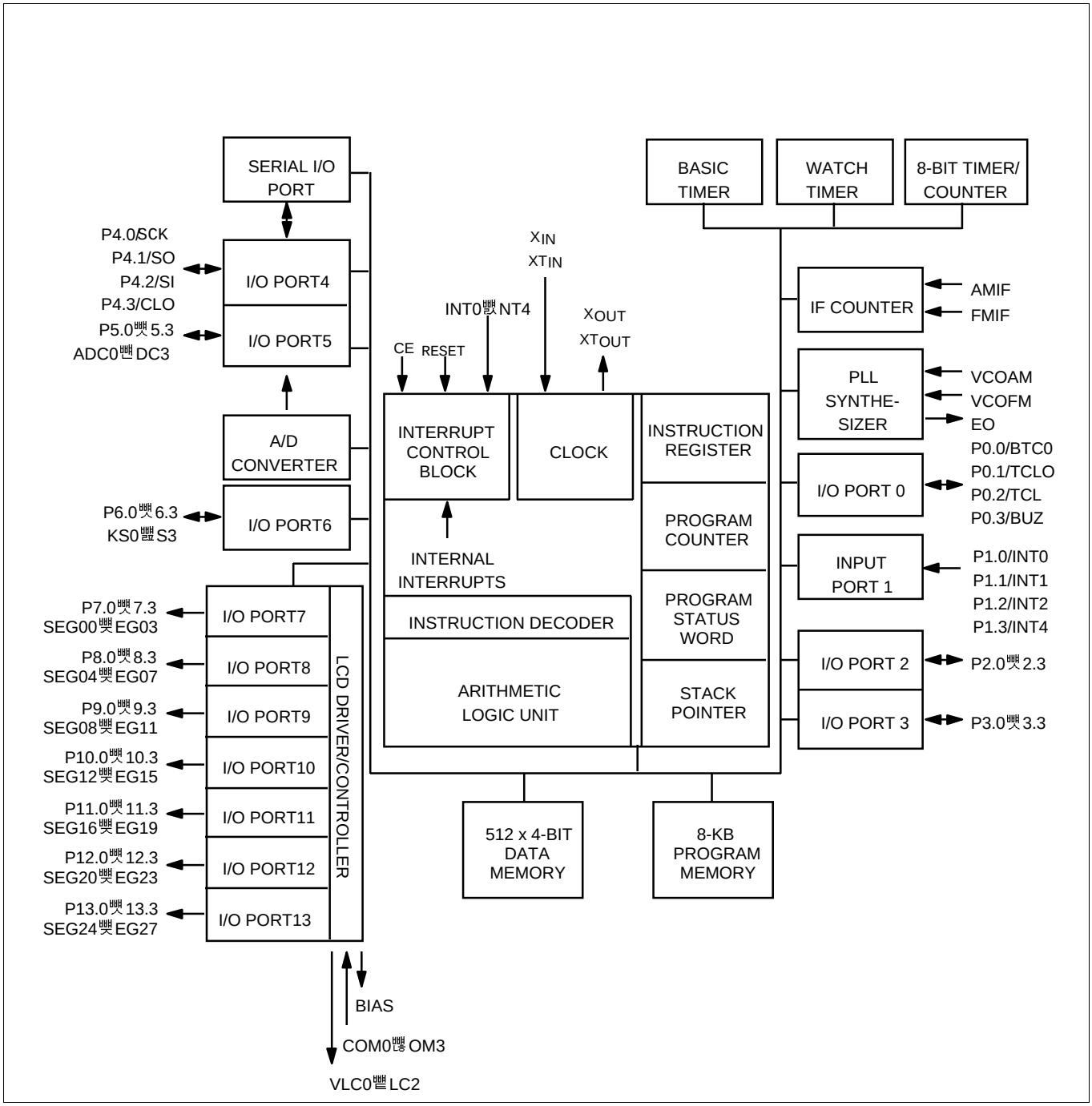


Figure 1. KS57C3108 Block Diagram

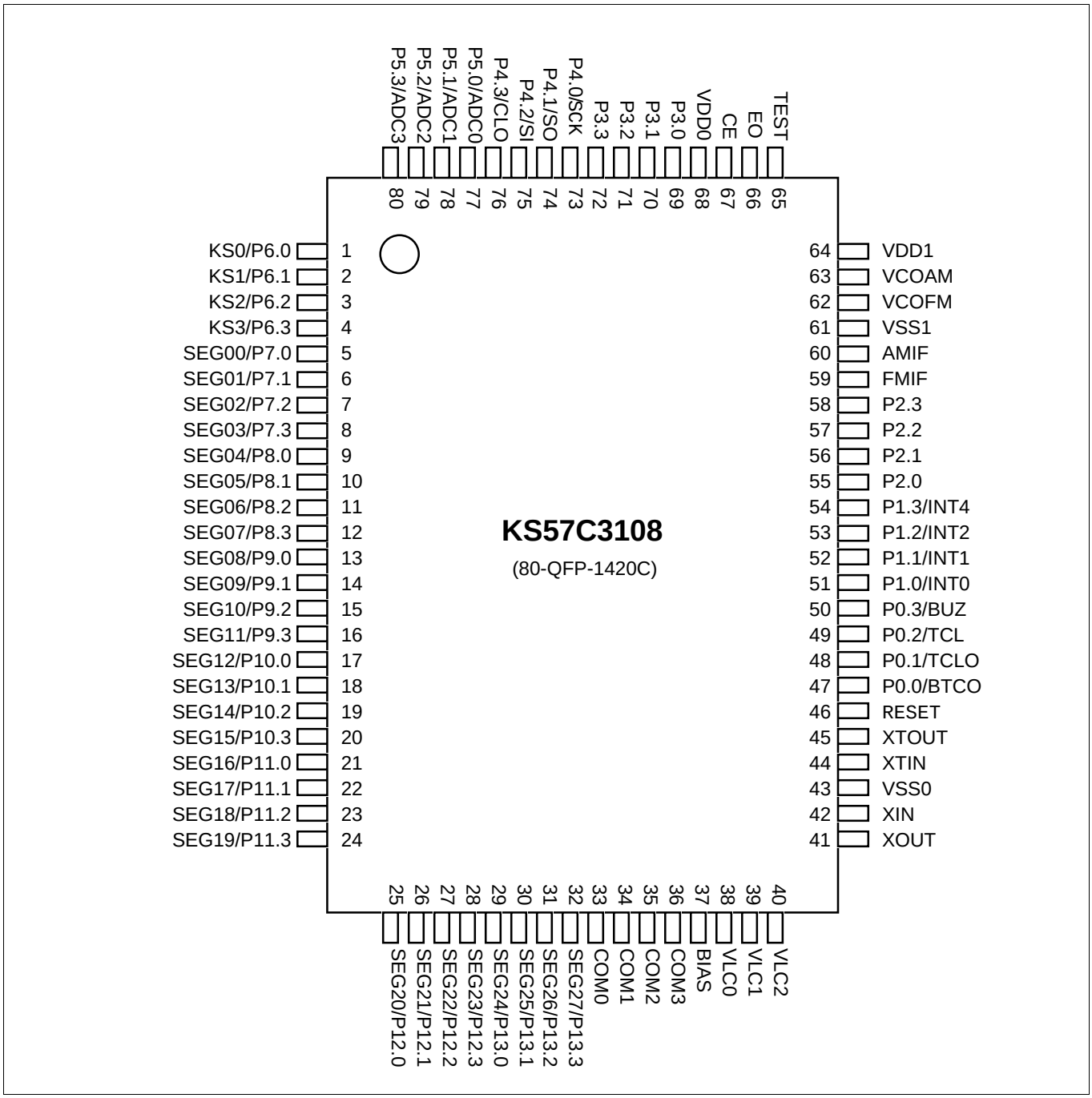


Figure 2. KS57C3108 (80-pin QFP) Pin Assignment Diagram

Table 1. KS57C3108 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write/test is possible. Pull-up resistors can be configured by software	47 48 49 50	BTCO TCLO TCL BUZ
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit or 4-bit read and test is possible. Pull-up resistors can be configured to P1.0, P1.1, and P1.2.	51 52 53 54	INT0 INT1 INT2 INT4
P2.0 – P2.3 P3.0 – P3.3	I/O	4-bit I/O port. 1-bit or 4-bit or 8-bit read/write/test are possible. Pull-up resistors can be configured by software. Ports 2 and 3 can be paired to support 8-bit data transfer.	55–58 69–72	—
P4.0 P4.1 P4.2 P4.3 P5.0 P5.1 P5.2 P5.3	I/O	4-bit I/O port. 1-bit or 4-bit or 8-bit read/write/test are possible. Pull-up resistors can be configured by software. Ports 4 and 5 can be paired to support 8-bit data transfer.	73 74 75 76 77 78 79 80	SCK SC SI CLO ADC0 ADC1 ADC2 ADC3
P6.0 P6.1 P6.2 P6.3	I/O	4-bit I/O port. 1-bit or 4-bit or 8-bit read/write/test is possible. Pull-up resistors can be configured by software.	1 2 3 4	KS0 KS1 KS2 KS3
P7.0 P7.1 P7.2 P7.3	O	4-bit output port. Alternatively used for LCD segment output.	5 6 7 8	SEG00 SEG01 SEG02 SEG03
P8.0 P8.1 P8.2 P8.3	O	4-bit output port. Alternatively used for LCD segment output.	9 10 11 12	SEG04 SEG05 SEG06 SEG07
P9.0 P9.1 P9.2 P9.3	O	4-bit output port. Alternatively used for LCD segment output.	13 14 15 16	SEG08 SEG09 SEG10 SEG11
P10.0 P10.1 P10.2 P10.3	O	4-bit output port. Alternatively used for LCD segment output.	17 18 19 20	SEG12 SEG13 SEG14 SEG15

Table 1. KS57C3108 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
P11.0 P11.1 P11.2 P11.3	O	4-bit output port. Alternatively used for LCD segment output.	21 22 23 24	SEG16 SEG17 SEG18 SEG19
P12.0 P12.1 P12.2 P12.3	O	4-bit output port. Alternatively used for LCD segment output.	25 26 27 28	SEG20 SEG21 SEG22 SEG23
P13.0 P13.1 P13.2 P13.3	O	4-bit output port. Alternatively used for LCD segment output.	29 30 31 32	SEG24 SEG25 SEG26 SEG27
COM0 COM1 COM2 COM3	O	Common signal output for LCD display	33 34 35 36	–
BIAS	I	LCD power control.	37	–
VLC0 VLC1 VLC2	I	LCD power supply. Voltage dividing resistors are assignable by software.	38 39 40	–
CE	I	Input pin for checking device power. Normal operation is High level and PLL operation stop is Low level.	67	–
V_{DD0}	–	Main power supply	68	–
V_{SS0}	–	Main ground pin	43	–
VCOFM VCOAM	I	External VCOFM/AM input pins	62 63	–
EO	O	Output pin for PLL error information	66	–
FMIF AMIF	I	FM/AM intermediate frequency input pins	59 60	–
V_{SS1}	–	PLL ground	61	–
V_{DD1}	–	PLL power supply	64	–
RESET	I	Chip reset signal pin	46	–
X_{OUT}	–	Main system clock output pin	41	–
X_{IN}	–	Main system clock input pin	42	–
XT_{IN}	–	Subsystem clock input pin	44	–
XT_{OUT}	–	Subsystem clock output pin	45	–
TEST	I	Chip test signal input (must be connected to V_{SS})	65	–

Table 2. Overview of KS57C3108 Pin Data

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
47–49	P0.0–P0.1, P0.3	BTCO, TCLO, BUZ	I/O	Input	5
50	P0.2	TCL	I/O		6
51–53	P1.0–P1.2	INT0, INT1, INT2	I		3
54	P1.3	INT4	I		2
55–58	P2.0–P2.3	–	I/O		5
69–72	P3.0–P3.3	–			5
73–75	P4.0–P4.2	SCK, SO, SI			6
76	P4.3	CLO			5
77–80	P5.0–P5.3	AD0–AD3			7
1–4	P6.0–P6.3	KS0–KS3			14
5–8	P7.0–P7.3	SEG00–SEG03	O	Output	11
9–12	P8.0–P8.3	SEG04–SEG07			
13–16	P9.0–P9.3	SEG08–SEG11			
17–20	P10.0–P10.3	SEG12–SEG15			
21–24	P11.0–P11.3	SEG16–SEG19			
25–28	P12.0–P12.3	SEG20–SEG23			
29–32	P13.0–P13.3	SEG24–SEG27			
33–36	COM0–COM3	–			10
37	BIAS		I	–	–
38–40	VLC0–VLC2			–	–
67	CE			Input	12
68	V_{DD0}		–	–	–
43	V_{SS0}		–	–	–
62, 63	VCOFM, VCOAM		I	Input	8
66	EO		O	Output	9
59, 60	FMIF, AMIF		I	Input	8
61	V_{SS1}		–	–	–
64	V_{DD1}		–	–	–

Table 2. Overview of KS57C3108 Pin Data(Continued)

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
46	RESET		–	Input	13
41	X_{OUT}		–	–	–
42	X_{IN}		–		
44	XT_{IN}		–		
45	XT_{OUT}		–		
65	TEST		I		

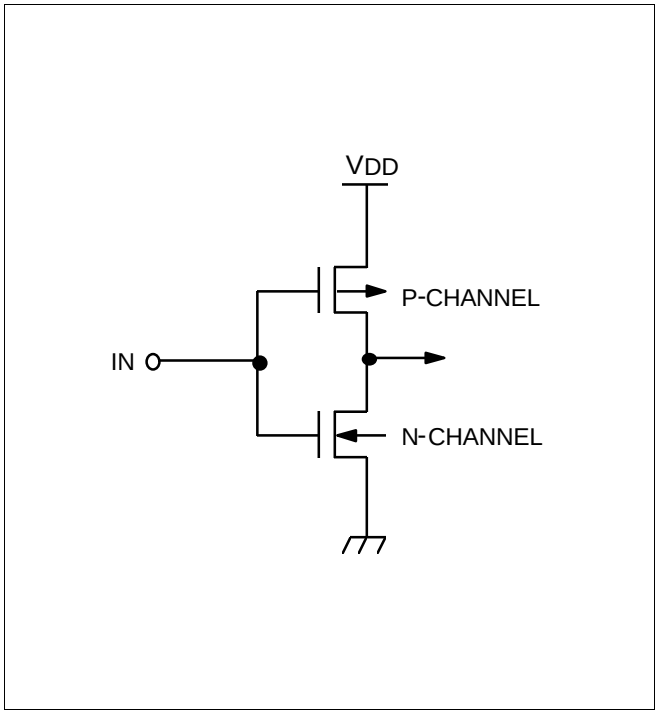
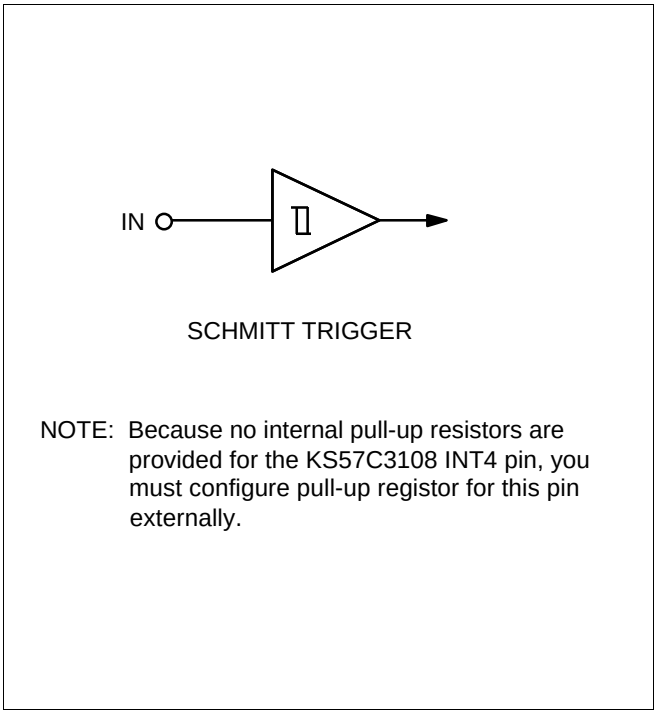


Figure 3. Pin Circuit Type 1



NOTE: Because no internal pull-up resistors are provided for the KS57C3108 INT4 pin, you must configure pull-up registor for this pin externally.

Figure 4. Pin Circuit Type 2