KS57C2504
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C2504 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM4 (Samsung Arrangeable Microcontrollers).With a two-channel comparator, up-to-320-dot LCD direct drive capability, 8-bit timer/counter, and serial I/O, the KS57C2504 offers an excellent design solution for a wide variety of applications which require LCD functions.

Up to 27 pins of the 80-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the KS57C2504's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

FEATURES

Memory

- 512 × 4-bit RAM
- 4096 × 8-bit ROM

27 I/O Pins

- I/O: 15 pins
- Input only: 4 pins
- Output only: 8 pins

Comparator

- Two-channel mode: internal reference (4-bit resolution)
- One-channel mode: external reference

LCD Controller/Driver

- 40 segments and 8 common terminals
- 3, 4 and 8 common selectable
- Internal resistor circuit for LCD bias
- All dot can be switched on/off

8-Bit Basic Timer

- 4 interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Serial I/O interface clock generator

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32768 Hz
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Interrupts

- Three internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 80-pin QFP

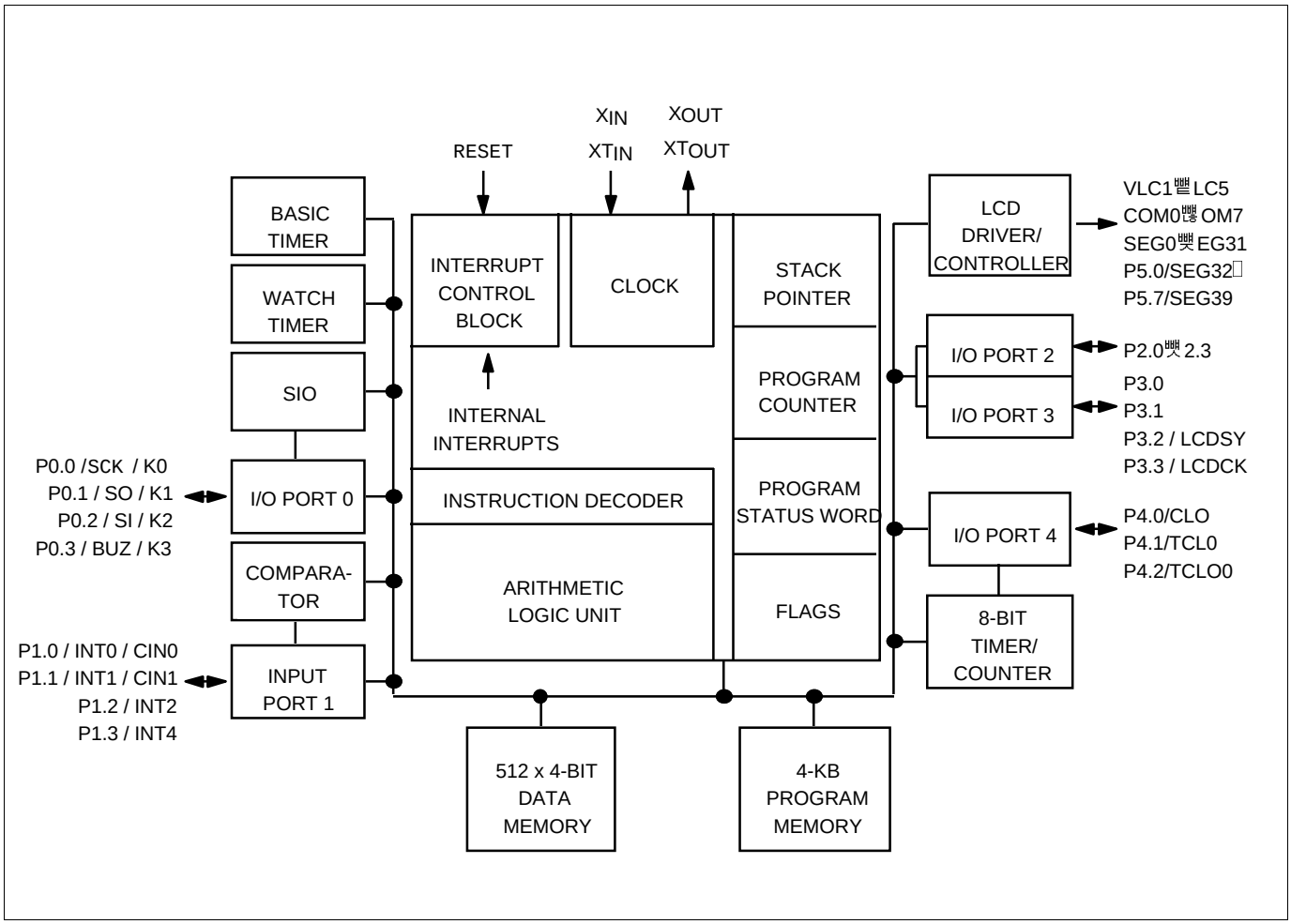

Figure 1. KS57C2504 Simplified Block Diagram

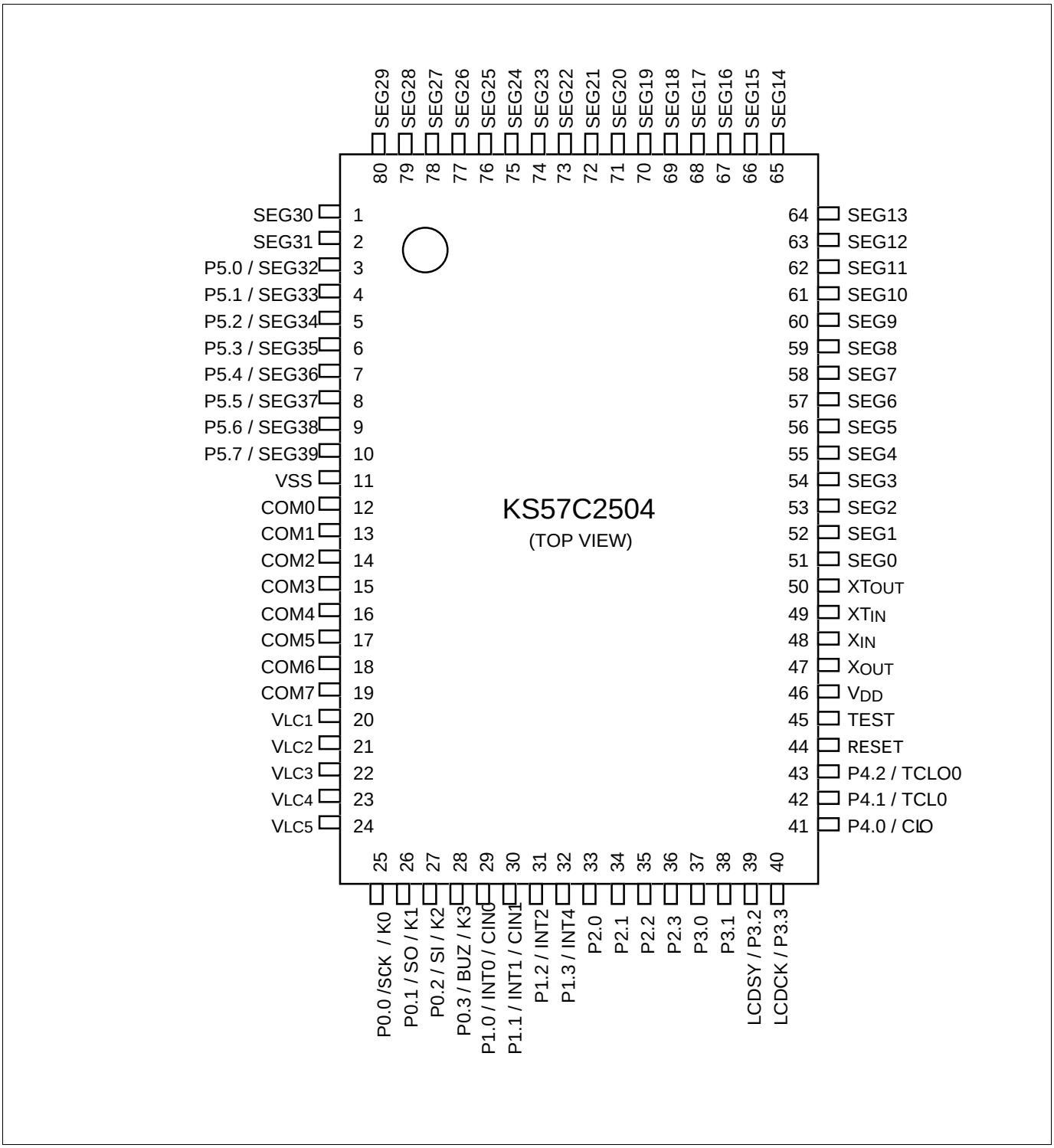

Figure 2. KS57C2504 80–Pin QFP Assignment Diagram

Table 1. KS57C2504 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	25 26 27 28	K0/SCK K1/SO K2/SI K3/BUZ
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit or 4-bit read and test are possible. The 1-bit unit pull-up resistors are assigned to input pins by software. An interrupt is generated by digital input at P1.0, P1.1.	29 30 31 32	INT0/CIN0 INT1/CIN1 INT2 INT4
P2.0–P2.3	I/O	Same as port 0 except that 8-bit read/write and test is possible.	33–36	–
P3.0 P3.1 P3.2 P3.3			37 38 39 40	– – LCDSY LCDCK
P4.0 P4.1 P4.2	I/O	Same as port 0 except that port 4 is 3-bit I/O port.	41 42 43	CLO TCL0 TCLO0
P5.0–P5.7	O	Output port for 1-bit data	3–10	SEG32– SEG39
SCK	I/O	Serial I/O interface clock signal	25	P0.0/K0
SO	I/O	Serial data output	26	P0.1/K1
SI	I/O	Serial data input	27	P0.2/K2
BUZ	I/O	2 KHz, 4 KHz, 8 KHz or 16 KHz frequency output for buzzer sound	28	P0.3/K3
K0–K3	I/O	External interrupt. The triggering edge is selectable.	25–28	P0.0–P0.3
INT0 INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	29 30	P1.0/CIN0 P1.1/CIN1
INT2	I	Quasi-interrupt with detection of rising or falling edges	31	P1.2
INT4	I	External interrupts with detection of rising and falling edges	32	P1.3

Table 1. KS57C2504 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
CIN0 CIN1	I	2-channel comparator input. CIN0: comparator input or external reference input CIN1: comparator input only.	29 30	P1.0/INT0 P1.1/INT1
LCDSY	I/O	LCD synchronization clock output for display expansion	39	P3.2
LCDCK	I/O	LCD clock output for display expansion	40	P3.3
CLO	I/O	Clock output	41	P4.0
TCL0	I/O	External clock input for timer/counter 0	42	P4.1
TCLO0	I/O	Timer/counter 0 clock output	43	P4.2
SEG32–SEG39	O	LCD segment signal output	3–10	P5.0–P5.7
SEG0–SEG29 SEG30–SEG31	O	LCD segment signal output	51–80 1–2	–
COM0–COM7	O	LCD common signal output	12–19	–
V_{LC1}–V_{LC5}	–	LCD power supply. Voltage dividing resistors are assignable by mask option.	20–24	–
X_{IN}, X_{OUT}	–	Crystal, ceramic or RC oscillator pins for system clock.	48, 47	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator pins for subsystem clock.	49, 50	–
V_{DD}	–	Main power supply	46	–
V_{SS}	–	Ground	11	–
RESET	I	Chip reset signal input	44	–
TEST	I	Chip test signal input (must be connected to V_{SS})	45	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

Table 2. KS57C2504 Pin Descriptions

Pin Name	Pin Type	Share Pin	Circuit Type	Reset Value
P0.0–P0.3	I/O	SCK/K0, SO/K1, SI/K2, BUZ/K3	6	Input
P1.0–P1.1	I	INT0/CIN0, INT1/CIN1	10	Comparator
P1.2–P1.3	I	INT2, INT4	3	Input
P2.0–P2.3	I/O	–	5	Input
P3.0–P3.1	I/O	–	5	Input
P3.2–P3.3	I/O	LCDSY, LCDCK	5	Input
P4.0, P4.2	I/O	CLO, TCLO0	5	Input
P4.1	I/O	TCL0	6	Input
P5.0–P5.7	O	SEG32–SEG39	7	High
COM0–COM7	O	–	8	High
SEG0–SEG31	O	–	8	High
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
RESET	I	–	2	–
VLC1–VLC5	–	–	–	–
X_{IN}, X_{OUT}	–	–	–	–
XT_{IN}, XT_{OUT}	–	–	–	–
TEST	I	–	–	–