1 PRODUCT OVERVIEW

OVERVIEW

The KS57C21116/C21124/C21132 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).
With an up-to-1280-dot LCD direct drive capability, segment expandable circuit, 8-bit and 16-bit timer/counter, and serial I/O, the KS57C21116/C21124/C21132 offers an excellent design solution for a wide variety of applications which require LCD functions.
Up to 51 pins of the 128-pin QFP package can be dedicated to I/O. Nine vectored interrupts provide fast response to internal and external events. In addition, the KS57C21116/C21124/C21132's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C21116/C21124/C21132 microcontroller is also available in OTP (One Time Programmable) version, KS57P21132. KS57P21132 microcontroller has an on-chip 32-Kbyte one-time-programmable EPROM instead of masked ROM. The KS57P21132 is comparable to KS57C21116/C21124/C21132, both in function and in pin configuration except ROM size.

FEATURES SUMMARY

Memory

- 3,584 × 4-bit RAM (Excluding LCD Display RAM)
- 16,384/24,576/32,768 × 8-bit ROM

51 I/O Pins

- I/O: 47 pins (32 pins are configurable as SEG pins)
- Input only: 4 pins

LCD Controller/Driver

- 80 SEG × 16 COM, 88 SEG × 8 COM Terminals
- Internal resistor circuit for LCD bias
- 16 Level LCD contrast control (software)
- Segment expandable circuit
- All dot can be switched on/off

8-bit Basic Timer

- 4 interval timer functions
- Watch-dog timer

8-bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider

16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Configurable as two 8-bit Timers
- Serial I/O interface clock generator

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32,768 Hz
- 4 frequency outputs to BUZ pin
- Clock source generation for LCD

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Comparator

- 3 Channel mode: internal reference (4-bit resolution)
- 2 Channel mode: external reference

Interrupts

- Five internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system clock stops)
- Subsystem clock stop mode

Oscillation Sources

- Crystal, Ceramic or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 0.4–6 MHz
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8 or 64)

Instruction Execution Times

- 0.67, 1.33, 10.7 µs at 6 MHz
- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 128-pin QFP

BLOCK DIAGRAM

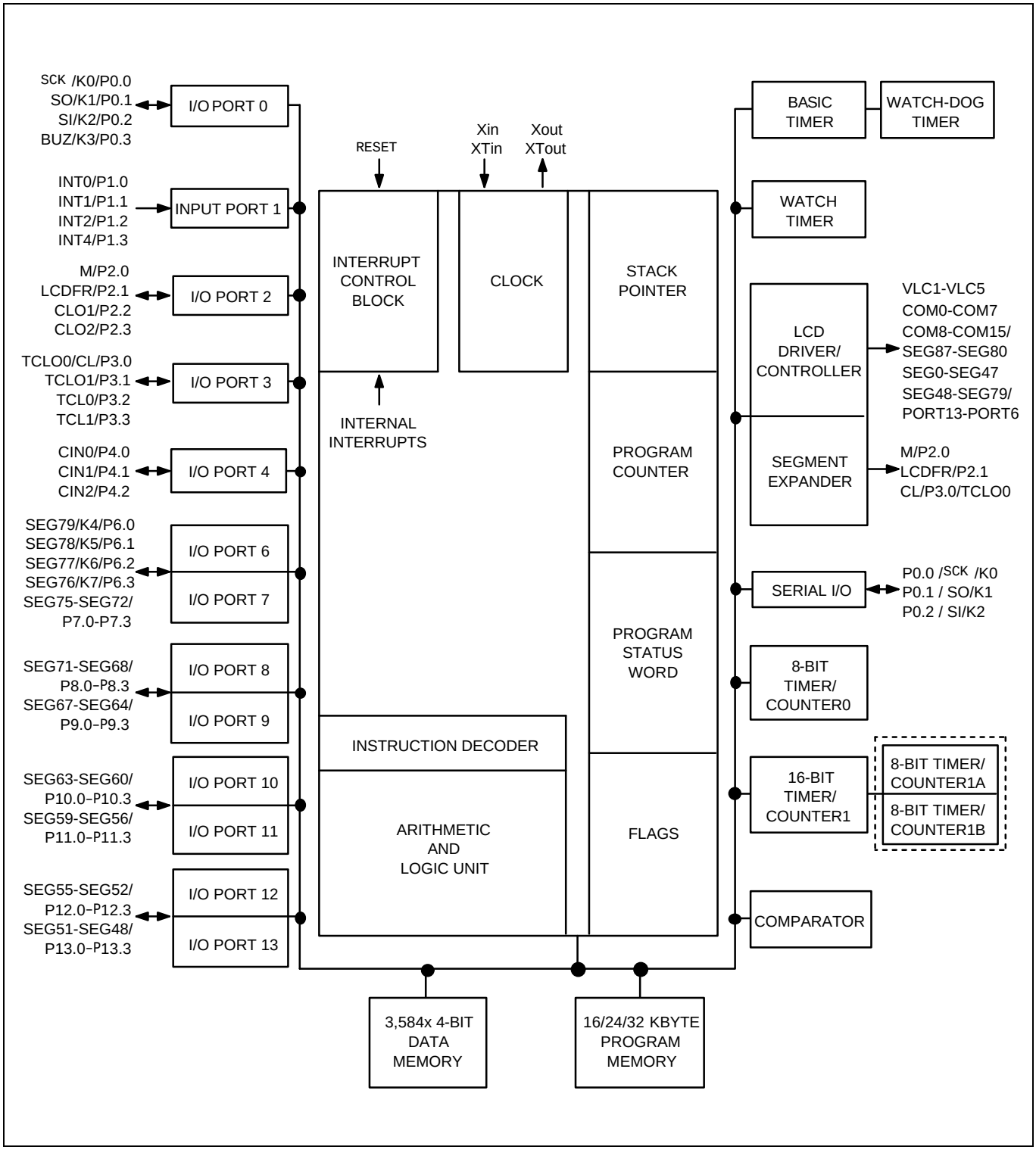

Figure 1-1. KS57C21116/C21124/C21132 Simplified Block Diagram

PIN ASSIGNMENTS

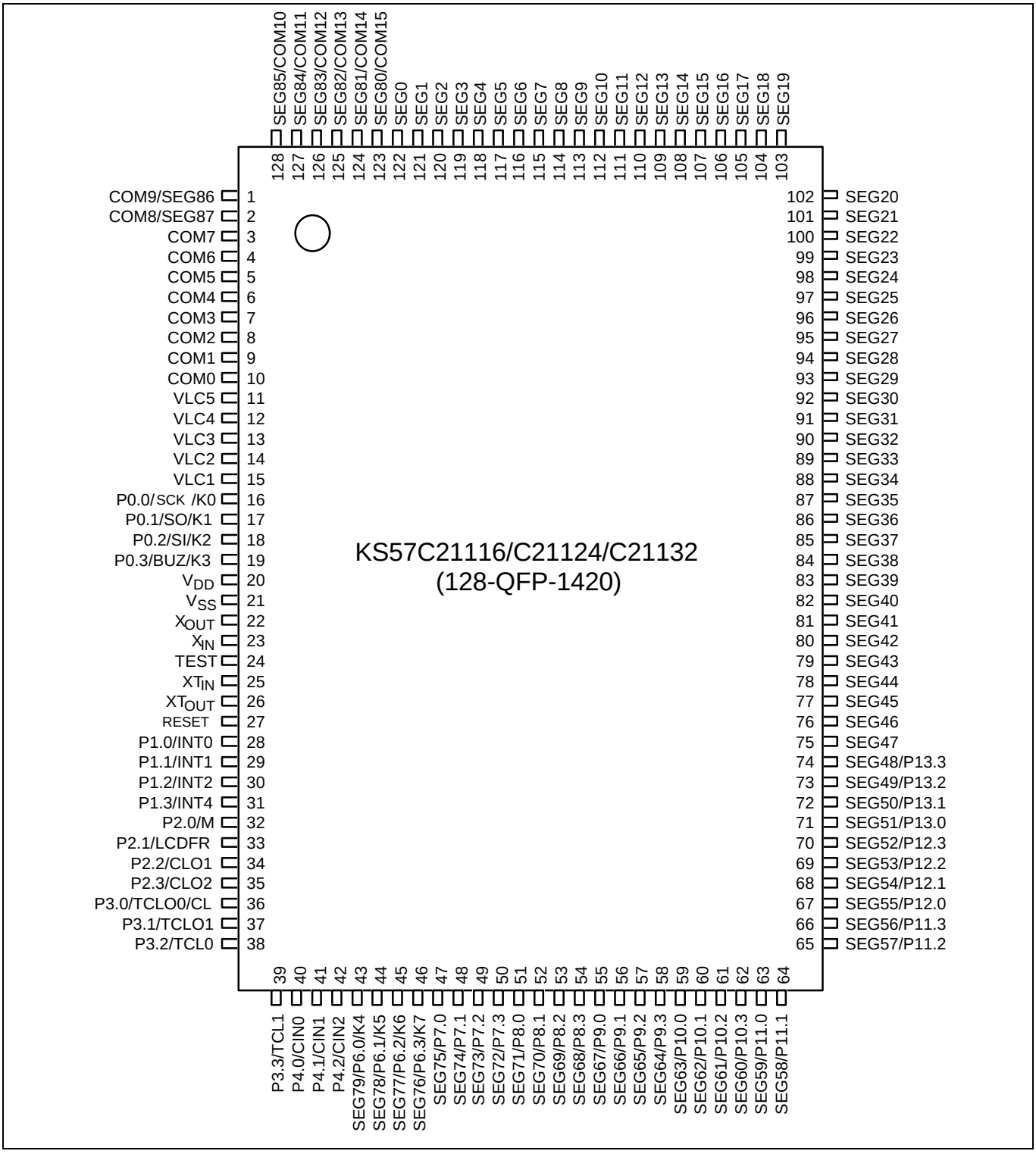

Figure 1-2. KS57C21116/C21124/C21132 128-QFP Pin Assignment

PIN DESCRIPTIONS

Table 1-1. KS57C21116/C21124/C21132 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. 4-bit unit pull-up resisters are assignable to input pins by software and are automatically disabled for output pins. Each bit pin can be allocated as input or output (1-bit unit). The N-ch open drain or push-pull output may be selected by software (1-bit unit).	16 17 18 19	SCK/K0 SO/K1 SI/K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 4-bit unit pull-up resistors are assignable to input pins by software.	28 29 30 31	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. I/O function is same as port 0.	32 33 34 35	M LCDFR CLO1 CLO2
P3.0 P3.1 P3.2 P3.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. I/O function is same as port 0.	36 37 38 39	TCLO0/CL TCLO1 TCL0 TCL1
P4.0 P4.1 P4.2	I/O	3-bit I/O port. I/O function is same as port 0 except that port 4 is 3-bit I/O port.	40 41 42	CIN0 CIN1 CIN2
P6.0 P6.1 P6.2 P6.3 P7.0–P7.3	I/O	4-bit I/O port. 1-, 4-bit and 8-bit read/write and test is possible. 4-bit unit pull-up resisters are assignable to input pins by software and are automatically disabled for output pins. Each bit pin can be allocated as input or output (1-bit unit). The N-ch open drain or push-pull output may be selected by software (4-bit unit).	43 44 45 46 47–50	K4/SEG79 K5/SEG78 K6/SEG77 K7/SEG76 SEG75–72
P8.0–P8.3 P9.0–P9.3	I/O	4-bit I/O port. 1-, 4-bit and 8-bit read/write and test is possible. I/O function is same as port 6, 7.	51–54 55–58	SEG71–68 SEG67–64
P10.0–P10.3 P11.0–P11.3	I/O	4-bit I/O port. 1-, 4-bit and 8-bit read/write and test is possible. I/O function is same as port 6, 7.	59–62 63–66	SEG63–60 SEG59–56
P12.0–P12.3 P13.0–P13.3	I/O	4-bit I/O port. 1-, 4-bit and 8-bit read/write and test is possible. I/O function is same as port 6, 7.	67–70 71–74	SEG55–52 SEG51–48
SCK	I/O	Serial I/O interface clock signal	16	P0.0
SO	I/O	Serial data output	17	P0.1
SI	I/O	Serial data input	18	P0.2
BUZ	I/O	2, 4, 8, 16 kHz frequency output for buzzer sound	19	P0.3
K0–K3 K4–K7	I/O	External interrupts with rising/falling edge detection	16–19 43–46	P0.0–P0.3 P6.0–P6.3

Table 1-1. KS57C21116/C21124/C21132 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
INT0	I	External interrupts with rising/falling edge detection	28	P1.0
INT1	I	External interrupts with rising/falling edge detection	29	P1.1
INT2	I	External quasi-interrupts with rising/falling edge detection	30	P1.2
INT4	I	External interrupts with rising/falling edge detection	31	P1.3
M	I/O	Alternated signal for SEG driver	32	P2.0
LCDFR	I/O	Synchronous frame signal for SEG driver	33	P2.1
CLO1	I/O	Clock output or operating clock for SEG driver	34	P2.2
CLO2	I/O	Clock output or operating clock for SEG driver	35	P2.3
CL	I/O	Data shift clock for SEG driver	36	P3.0
TCLO0	I/O	Timer/counter0 clock output	36	P3.0
TCLO1	I/O	Timer/counter1 clock output	37	P3.1
TCL0	I/O	External clock input for timer/counter 0	38	P3.2
TCL1	I/O	External clock input for timer/counter 1	39	P3.3
CIN0–CIN2	I/O	CIN0,1: comparator input only CIN2: comparator input or external reference input	40, 41 42	P4.0–P4.1 P4.2
SEG0–SEG47	O	LCD segment data output	122–75	–
SEG48–SEG79	O	LCD segment data output	74–43	Port13–6
SEG80–SEG87	O	LCD segment data output	2,1, 128–123	COM15–8
COM0–COM7	O	LCD common data output	10–3	–
COM8–COM15	O	LCD common data output	123–128 1, 2	SEG87–80
V_{LC1}–V_{LC5}	–	LCD power supply. Voltage dividing resistors are fixed.	15–11	–
V_{DD}	–	Main power supply	20	–
V_{SS}	–	Ground	21	–
X_{in}, X_{out}	–	Crystal, Ceramic, or RC oscillator signal I/O for main system clock.	23, 22	–
XT_{in}, XT_{out}	–	Crystal oscillator signal I/O for subsystem clock.	25, 26	–
TEST	I	Test signal input (must be connected to V_{SS})	24	–
RESET	I	Reset signal	27	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

Table 1-2. Overview of KS57C21116/C21124/C21132 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	SCK, SO, SI, BUZ/K0–K3	I/O	Input	E-2
P1.0–P1.3	INT0–INT2, INT4	I	Input	A-3
P2.0–P2.3	M, LCDFR, CLO1, CLO2	I/O	Input	E
P3.0–P3.1	TCLO0/CL, TCLO1	I/O	Input	E
P3.2–P3.3	TCL0, TCL1	I/O	Input	E-1
P4.0–P4.2	CIN0–CIN2	I/O	Input	F-4
P6.0–P6.3	K4–K7/SEG79–SEG76	I/O	Input	H-15
P7.0–P7.3	SEG75–SEG72	I/O	Input	H-8
P8.0–P8.3	SEG71–SEG68	I/O	Input	H-8
P9.0–P9.3	SEG67–SEG64	I/O	Input	H-8
P10.0–P10.3	SEG63–SEG60	I/O	Input	H-8
P11.0–P11.3	SEG59–SEG56	I/O	Input	H-8
P12.0–P12.3	SEG55–SEG52	I/O	Input	H-8
P13.0–P13.3	SEG51–SEG48	I/O	Input	H-8
COM0–COM7	–	O	Low output	H-4
COM8–COM15	SEG87–SEG80	O	Low output	H-6
SEG0–SEG47	–	O	Low output	H-5
V_{LC1}–V_{LC5}	–	–	–	–
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
X_{IN}, X_{OUT}	–	–	–	–
XT_{IN}, XT_{OUT}	–	–	–	–
RESET	–	I	–	B
TEST	–	I	–	–