SAMSUNG ELECTRONICS

KS57C2102
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C2102 single-chip CMOS microcontroller is designed for high-performance using Samsung's advanced modular development approach, SAM4 (Samsung Arrangeable 4-bit Microcontrollers).Pull-up resistors are assignable by software to all four I/O pins. Four vectored interrupts provide fast response to system events.

With LCD direct drive capability (up to six digits), up to 12 pins for LCD segment data output, a versatile 8-bit timer/counter, basic timer, and watch timer, the KS57C2102 is an excellent design solution for a wide variety of general-purpose applications.

FEATURES

Memory

- 256 × 4-bit RAM
  (Data: 244, display: 12)
- 2048 × 8-bit program memory (ROM)

I/O Pins

- I/O: 4 pins
- Output only: 4 pins

LCD Controller/Driver

- Maximum 6-digit LCD direct drive capability
- 12 segments x 4 common signals
- Display modes: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer

- Programmable interval timer

8-Bit Timer/Counter

- Programmable interval timer
- External event counter function
- Timer/counter external clock input (TCL0)

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz
- Four frequency outputs to the BUZ pin

Bit Sequential Carrier

- 16-bit serial data transfer in arbitrary format

Interrupts

- Two external interrupt vectors
- Two internal interrupt vectors
- One quasi-interrupt

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: System clock stops

Oscillation Sources

- Crystal, ceramic, or RC for system clock
- Crystal or ceramic: 4.19 MHz (typical)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- Three main system clocks: 0.9, 1.8, 14.2 µs at 4.19 MHz
- Three subsystem clocks: 122 µs at 32.768 kHz

Operating Temperature

- – 40°C to + 85°C

Operating Voltage Range

- 2.7 V to 5.5 V

Package Types

- 28-pin DIP, 28-pin SOP

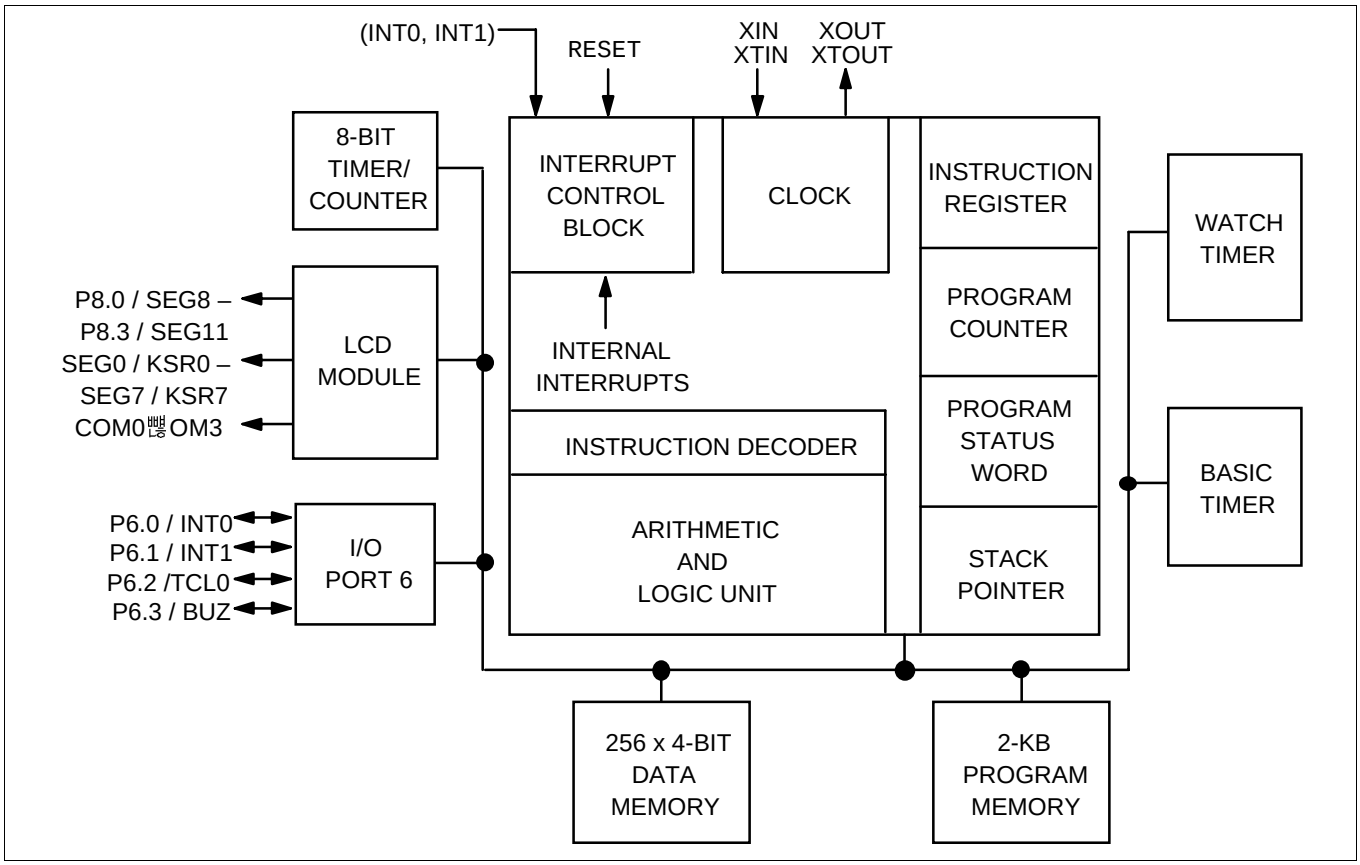

Figure 1. KS57C2102 Simplified Block Diagram

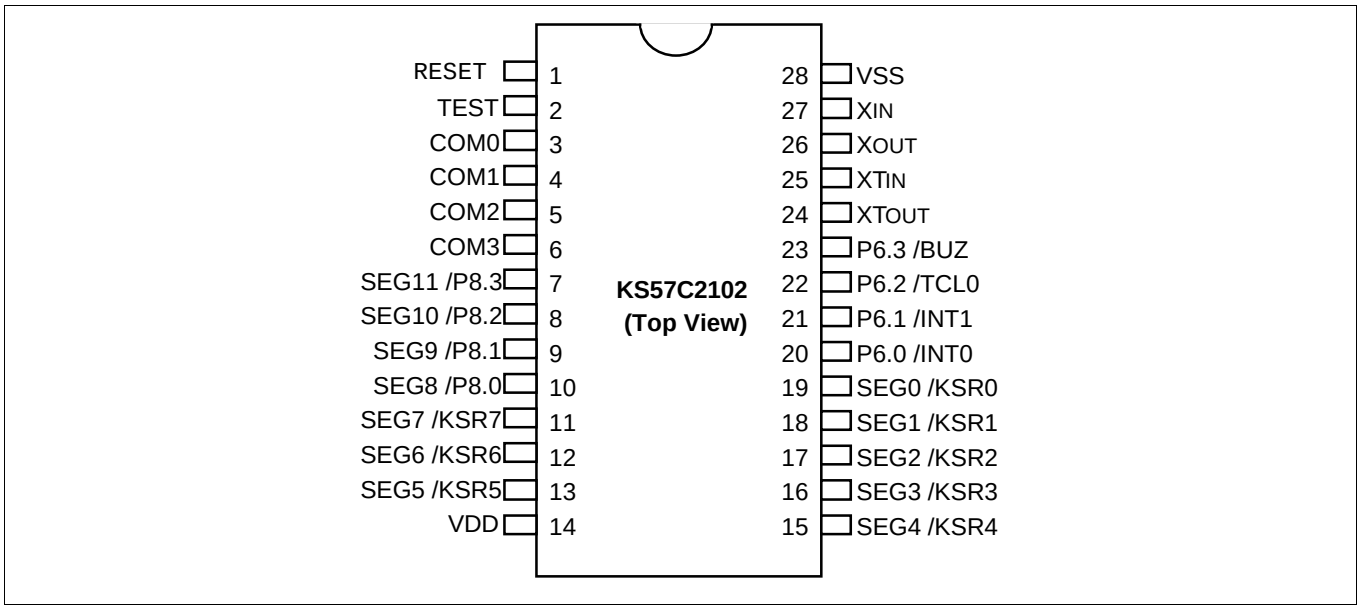

Figure 2. KS57C2102 Pin Assignment Diagram

Table 1. KS57C2102 Pin Descriptions

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
P6.0–P6.3	I/O	4-bit input/output port. Bit programmable pins. 1-bit and 4-bit read/write, and test is supported . Pins can be configured either to input mode or to push-pull or n-channel open-drain output mode. Pull-ups are also assignable by software.	4	20–23	INT0 INT1 TCL0 BUZ
P8.0–P8.3	O	Output port for 1-bit data (only if port8 is not used for LCD segment output)	3	10–7	SEG8–SEG11
SEG0–SEG7	O	LCD segment display signal output pins	1	19–15 13–11	KSR0–KSR7
SEG8–SEG11	O	LCD segment display signal output pins	3	10–7	P8.0–P8.3
COM0–COM3	O	LCD common signal output pins	2	3–6	—
KSR0–KSR7	O	Key strobe outputs	1	19–15, 13–11	SEG0-SEG7
INT0, INT1	I/O	External interrupt inputs	4	20, 21	P6.0, P6.1
BUZ	I/O	Frequency output to buzzer	4	23	P6.3
TCL0	I/O	Timer/counter external clock input	4	22	P6.2
X_{IN}, X_{OUT}	—	Clock input and output pins for main system clock	—	27, 26	—
XT_{IN}, XT_{OUT}	—	Clock input and output pins for subsystem clock	—	25, 24	—
RESET	I	Chip reset signal input	5	1	—
TEST	I	Chip test signal input(must be connected to V_{SS})	—	2	—
V_{DD}	—	Power supply pin	—	14	—
V_{SS}	—	Ground pin	—	28	—