# 1 PRODUCT OVERVIEW

The KS57C0502/C0504 single-chip CMOS microcontroller has been designed for high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

The KS57P0504 is the microcontroller which has 4 Kbyte one-time-programmable ROM and the functions are the same to KS57C0502/C0504. With a four-channel comparator, eight LED direct drive pins, serial I/O interface, and its versatile 8-bit timer/counter, the KS57C0502/C0504 offers an excellent design solution for a wide variety of general-purpose applications.

Up to 24 pins of the 30-pin SDIP package can be dedicated to I/O. Five vectored interrupts provide fast response to internal and external events. In addition, the KS57C0502/C0504's advanced CMOS technology provides for very low power consumption and a wide operating voltage range —all at a very low cost.

## FEATURES SUMMARY

### MEMORY

512 × 4-bit data memory (RAM)
2048 × 8-bit program memory (ROM):KS57C0502
4096 × 8-bit program memory (ROM):KS57C0504

### 24 I/O PINS

I/O: 18 pins, including 8 high current pins
Input only: 6 pins

### COMPARATOR

4-channel mode:
  Internal reference (4-bit resolution)
  16-step variable reference voltage
3-channel mode:
  External reference
150 mV resolution (worst case)

### 8-BIT BASIC TIMER

Programmable interval timer
Watch-dog timer

### 8-BIT TIMER/COUNTER

Programmable interval timer
External event counter function
Timer/counter clock output to TCLO0 pin

### WATCH TIMER

Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz
4 frequency outputs to BUZ pin

### 8-BIT SERIAL I/O INTERFACE

8-bit transmit/receive mode
8-bit receive-only mode
LSB-first or MSB-first transmission selectable
Internal or external clock source

### BIT SEQUENTIAL CARRIER

Supports 16-bit serial data transfer in arbitrary format

### INTERRUPTS

Two external interrupt vectors
Three internal interrupt vectors
Two quasi-interrupts

### MEMORY-MAPPED I/O STRUCTURE

Data memory bank 15

### TWO POWER-DOWN MODES

Idle mode: Only CPU clock stops
Stop mode: System clock stops

### OSCILLATION SOURCES

Crystal, Ceramic for system clock
Crystal/ceramic: 0.4 - 6.0 MHz
CPU clock divider circuit (by 4. 8, or 64)

### INSTRUCTION EXECUTION TIMES

0.95, 1.91, 15.3 µs at 4.19 MHz
0.67, 1.33, 10.7 µs at 6.0 MHz

### OPERATING TEMPERATURE

– 40 °C to 85 °C

### OPERATING VOLTAGE RANGE

1.8 V to 5.5 V

## BLOCK DIAGRAM

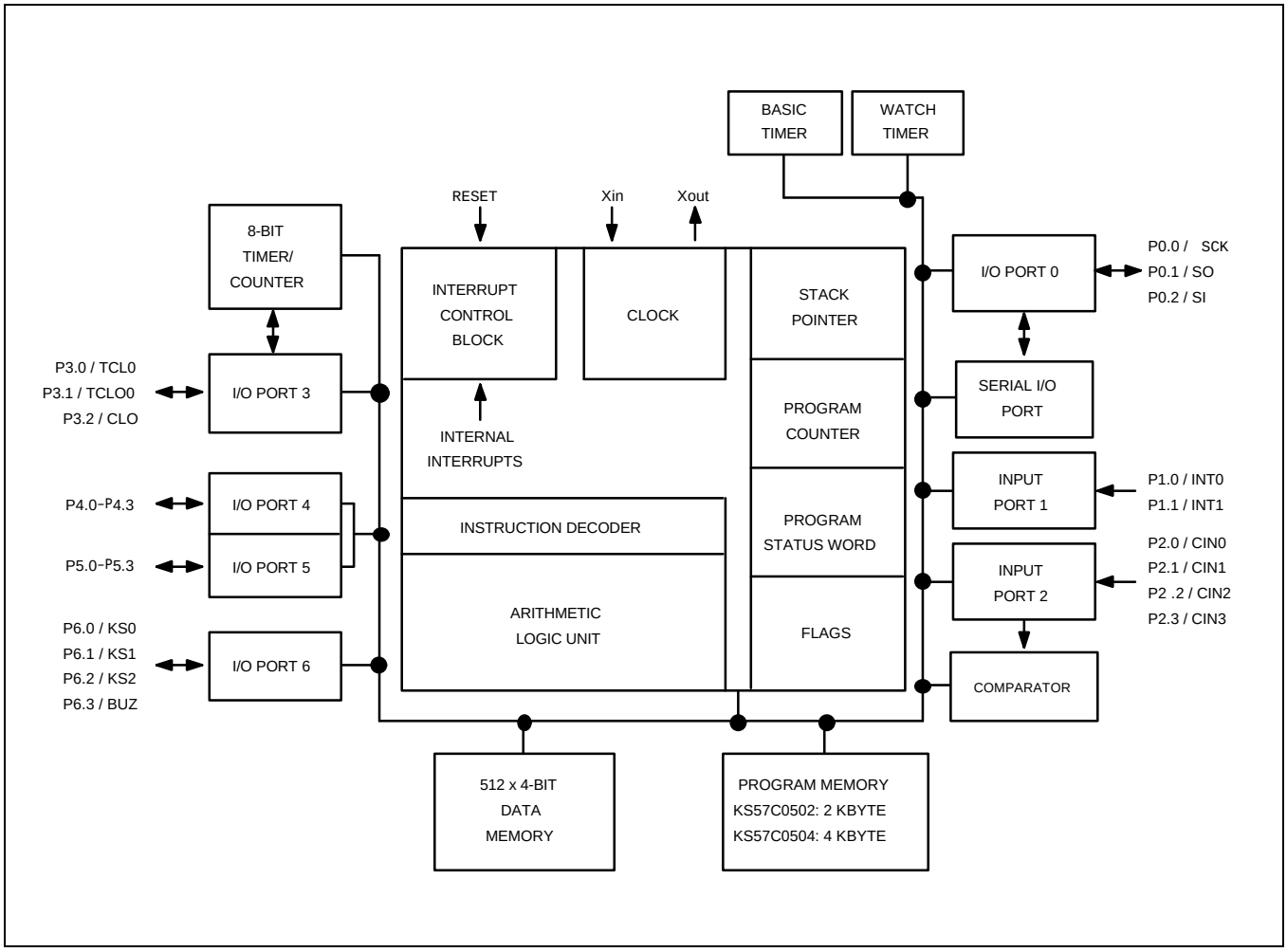
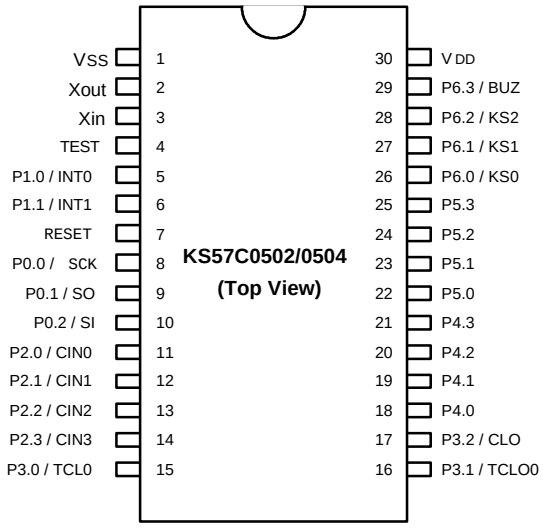
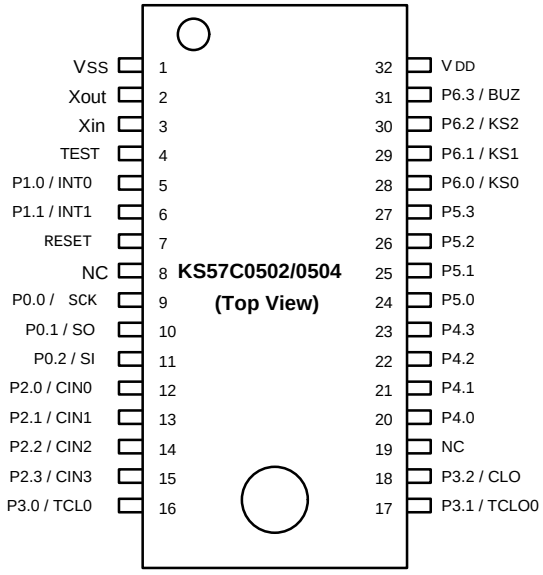



**Figure 1–1. KS57C0502/C0504 Simplified Block Diagram**

## PIN ASSIGNMENTS




**30-pin SDIP**




**32-pin SOP**

**Figure 1–2. KS57C0502/C0504 Pin Assignment Diagram**

## PIN DESCRIPTIONS

**Table 1–2. KS57C0502/C0504 Pin Descriptions**

| Pin Name | Pin Type | Description | Number | Share Pin |
|---|---|---|---|---|
| P0.0<br>P0.1<br>P0.2 | I/O | 3-bit I/O port. 1-bit or 3-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output. | 8(9)<br>9(10)<br>10(11) | SCK<br>SO<br>SI |
| P1.0<br>P1.1 | I | 2-bit input port. 1-bit or 2-bit read and test is possible. Pull-up resistors are assignable by software. | 5(5)<br>6(6) | INT0<br>INT1 |
| P2.0–P2.3 | I | 4-bit input port. 1-bit or 4-bit read and test is possible. | 11-14<br>(12-15) | CIN0–CIN3 |
| P3.0<br>P3.1<br>P3.2 | I/O | Same as port 0 | 15(16)<br>16(17)<br>17(18) | TCL0<br>TCLO0<br>CLO |
| P4.0–P4.3<br>P5.0–P5.3 | I/O | 4-bit I/O ports. 1-, 4-, or 8-bit read/write and test is possible. Pins are individually configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. The N-channel open-drain or push-pull output can be selected by software (1-bit unit) | 18-21(20-23)<br>22-25(24-27) | — |
| P6.0<br>P6.1<br>P6.2<br>P6.3 | I/O | 4-bit I/O port.<br>1-bit or 4-bit read/write and test is possible.<br>Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output. | 26(28)<br>27(29)<br>28(30)<br>29(31) | KS0<br>KS1<br>KS2<br>BUZ |
| INT0 | I | External interrupts with detection of rising and falling edges | 5(5) | P1.0 |
| INT1 | I | External interrupts with detection of rising or falling edges | 6(6) | P1.1 |
| CIN0–CIN3 | I | 4-channel comparator input.<br>CIN0–CIN2: comparator input only.<br>CIN3: comparator input or external reference input | 11-14(12-15) | P2.0–P2.3 |
| SCK | I/O | Serial interface clock signal | 8(9) | P0.0 |
| SO | I/O | Serial data output | 9(10) | P0.1 |
| SI | I/O | Serial data input | 10(11) | P0.2 |
| TCL0 | I/O | External clock input for timer/counter | 15(16) | P3.0 |
| TCLO0 | I/O | Timer/counter clock output | 16(17) | P3.1 |
| CLO | I/O | CPU clock output | 17(18) | P3.2 |
| BUZ | I/O | 2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at 4.19 MHz for buzzer sound | 29(31) | P6.3 |

**NOTE**: Pin numbers shown in parentheses '( )' are for 32-pin SOP package; other pin numbers are for the 30-pin SDIP.

**Table 1–2. KS57C0502/C0504 Pin Descriptions (Continued)**

| Pin Name | Pin Type | Description | Number | Share Pin |
|---|---|---|---|---|
| KS0–KS2 | I/O | Quasi-interrupt input with falling edge detection | 26-28(28-30) | P6.0–P6.2 |
| $V_{DD}$ | — | Main power supply | 30(32) | — |
| $V_{SS}$ | — | Ground | 1(1) | — |
| RESET | I | Reset signal | 7(7) | — |
| TEST | I | Test signal input (must be connected to $V_{SS}$) | 4(4) | — |
| $X_{in}$, $X_{out}$ | — | Crystal or ceramic oscillator signal for system clock | 3,2(3,2) | — |

**NOTE**: Pin numbers shown in parentheses '( )' are for 32-pin SOP package; other pin numbers are for the 30-pin SDIP.

**Table 1–3. Overview of KS57C0502/C0504 Pin Data**

| SDIP Pin Numbers | Pin Names | Share Pins | I/O Type | Reset Value | Circuit Type |
|---|---|---|---|---|---|
| 1 | $V_{SS}$ | — | — | — | — |
| 2,3 | Xout, Xin | — | — | — | — |
| 4 | TEST | — | I | — | — |
| 5,6 | P1.0, P1.1 | INT0, INT1 | I | Input | A-3 |
| 7 | RESET | — | I | — | B |
| 8-10 | P0.0 - P0.2 | SCK, SO, SI | I/O | Input | D-1 |
| 11-14 | P2.0 - P2.3 | CIN0 - CIN3 | I | Input | F-1, F-2 (note) |
| 15-17 | P3.0 - P3.2 | TCL0, TCLO0, CLO | I/O | Input | D-1 |
| 18-21 | P4.0 - P4.3 | — | I/O | Input | E |
| 22-25 | P5.0 - P5.3 | — | I/O | Input | E |
| 26-29 | P6.0 - P6.3 | KS0, KS1, KS2, BUZ | I/O | Input | D-1 |
| 30 | $V_{DD}$ | — | — | — | — |

**NOTE**: I/O circuit type F-2 is implemented for P2.3 only.