KS57C0002/0004
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C0002/0004 single-chip CMOS microcontroller is designed for high-performance using Samsung's newest 4-bit CPU core. With a four-channel comparator, eight LED direct drive pins, serial I/O interface, and a versatile
8-bit timer/countkxcellent design solution for a variety of general-purpose applications.

Up to 24 pins of the 30-pin SDIP package can be dedicated to I/O. Five vectored interrupts provide fast response to internal and external events. In addition, the KS57C0002/0004's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory

- 256 × 4-bit data memory (KS57C0002)
  512 × 4-bit data memory (KS57C0004)
- 2048 × 8-bit program memory (KS57C0002)
  4096 × 8-bit program memory (KS57C0004)

24 I/O Pins

- I/O: 18 pins, including 8 high-current pins
- Input only: 6 pins

Comparator

- 4-channel mode with internal reference (4-bit resolution) and 16-step variable reference voltage
- 3-channel mode with external reference
- 150 mV resolution (minimum)

8-Bit Basic Timer

- Programmable interval timer

8-Bit Timer/Counter

- Programmable interval timer
- External event counter function
- Timer/counter clock output to TCLO0 pin

Watch Timer

- Interval generation: 0.5 s, 3.9ms at 32768 Hz
- Four frequency outputs to the BUZ pin

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive-only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Bit Sequential Carrier

- Support for 16-bit serial data transfer in arbitrary format

Interrupts

- Two external interrupt vectors
- Three internal interrupt vectors
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (system clock stops)

Oscillation Sources

- Crystal, ceramic, or RC for system clock (RC is only for the KS57C0002)
- Crystal, ceramic: 4.19 MHz (typical)
- RC: 1 MHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 μs at 4.19 MHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 30 SDIP, 32 SOP

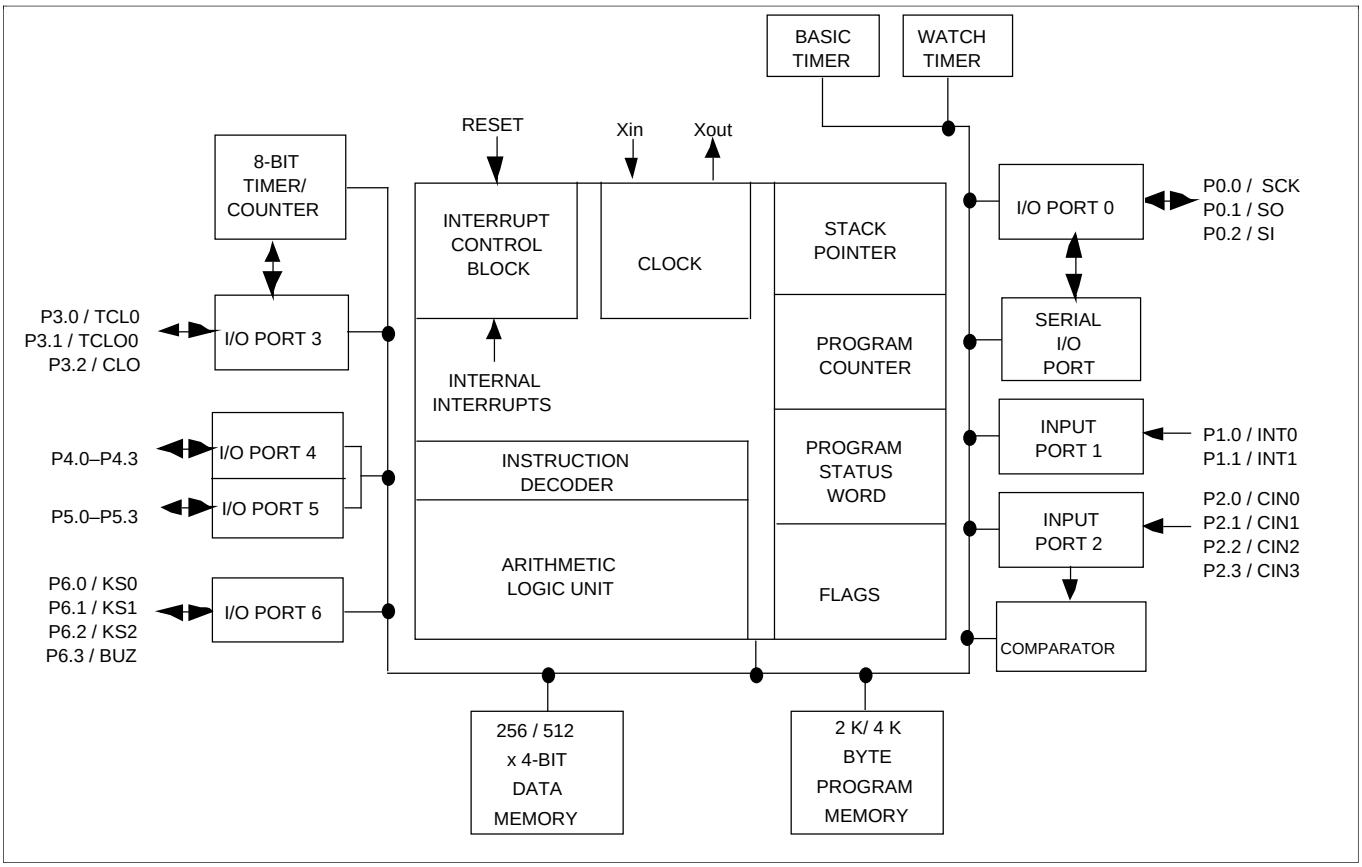

Figure 1. KS57C0002/0004 Block Diagram

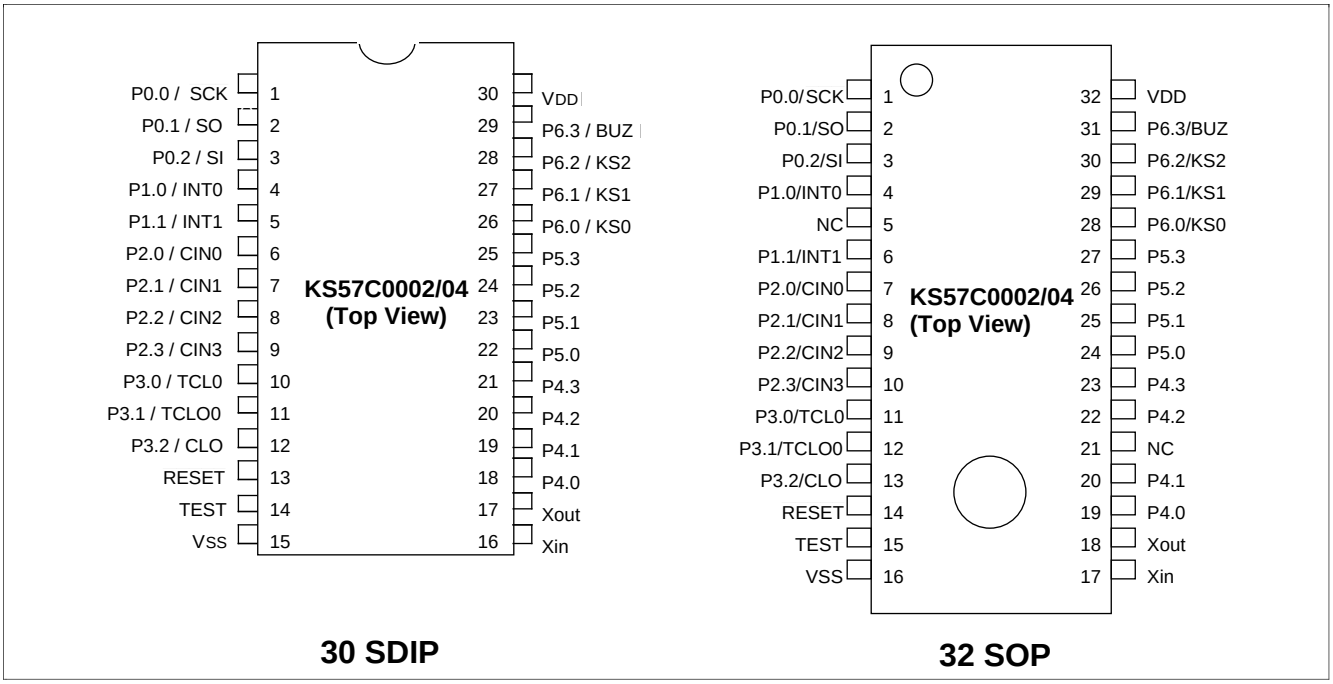

Figure 2. KS57C0002/0004 Pin Assignments (32 SOP, 30 SDIP)

Table 1. KS57C0002/0004 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2	I/O	3-bit I/O port. 1-bit or 3-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	1 2 3	SCK SO SI
P1.0 P1.1	I	2-bit input port. 1-bit or 2-bit read and test is possible. Pull-up resistors are assignable by software.	4 5	INT0 INT1
P2.0–P2.3	I	4-bit input port. 1-bit or 4-bit read and test is possible.	6–9	CIN0–CIN3
P3.0 P3.1 P3.2	I/O	Same as port 0	10 11 12	TCL0 TCLO0 CLO
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-, 4-, or 8-bit read/write and test is possible. Pins are individually configurable as input or output. Ports can be configurable as n-channel open-drain by mask option (maximum 9V).	18–21 22–25	—
P6.0 P6.1 P6.2 P6.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins individually configurable as input or output.	26 27 28 29	KS0 KS1 KS2 BUZ
INT0	I	External interrupts with rising/falling edge detection	4	P1.0
INT1	I	External interrupts with rising/falling edge detection	5	P1.1
CIN0–CIN3	I	4-channel comparator input. CIN0–CIN2: comparator input only. CIN3: comparator input or external reference input	6–9	P2.0–P2.3
SCK	I/O	Serial interface clock signal	1	P0.0
SO	I/O	Serial data output	2	P0.1
SI	I/O	Serial data input	3	P0.2
TCL0	I/O	External clock input for timer/counter	10	P3.0
TCLO0	I/O	Timer/counter clock output	11	P3.1
CLO	I/O	CPU clock output	12	P3.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at 4.19 MHz for buzzer sound	29	P6.3
KS0–KS2	I/O	Quasi-interrupt input with falling edge detection	26–28	P6.0–P6.2
V_{DD}	—	Main power supply	30	—
V_{SS}	—	Ground	15	—
RESET	I	Reset signal	13	—
TEST	I	Test signal input (must be connected to V_{SS})	14	—
X_{in}, X_{out}	—	Crystal, ceramic, or RC oscillator signal for system clock	16, 17	—

Table 2. Supplemental KS57C0002/0004 Pin Data

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1, 2, 3	P0.0–P0.2	SCK, SO, SI	I/O	Input	5
4, 5	P1.0, P1.1	INT0, INT1	I	Input	3
6–9	P2.0–P2.3	CIN0–CIN3	I	Input	6, 8 *
10–12	P3.0–P3.2	TCL0, TCLO0, CLO	I/O	Input	5
13	RESET	—	I	—	9
14	TEST	—	I	—	—
15	V_{SS}	—	—	—	—
16, 17	Xin, Xout	—	—	—	—
18–21	P4.0–P4.3	—	I/O	Input	7
22–25	P5.0–P5.3	—	I/O	Input	7
26–29	P6.0–P6.3	KS0, KS1, KS2, BUZ	I/O	Input	5
30	V_{DD}	—	—	—	—

* I/O circuit type 8 is for P2.3 only.