OVERVIEW

Samsung's KS32C6100 16/32-bit RISC microcontroller provides a cost-effective and high-performance microcontroller solution for laser beam printers (LBP) with PCL/PDL interpreters. To accelerate raster image generation, the KS32C6100 directly processes scanned image data for the laser printer engine.

An outstanding feature of the KS32C6100 is its CPU core, a 16/32-bit RISC processor (ARM7TDMI) designed by Advanced RISC Machines, Ltd. The ARM7TDMI core is a low-power, general-purpose, microprocessor macro-cell that was developed for use in application-specific and customer-specific integrated circuits. Its simple, elegant, and fully static design is particularly suitable for cost-sensitive and power-sensitive applications.

The KS32C6100 was developed using the ARM7TDMI core, 0.5-µm standard cells, and a data path compiler. Most of the on-chip function blocks were designed using a HDL synthesizer. The KS32C6100 has been fully verified in Samsung′s ASIC test environment.

By providing a complete set of common system peripherals, the KS32C6100 minimizes overall system costs and eliminates the need to configure additional components.

The main integrated on-chip function blocks which are described in this document include:

- ROM/SRAM/DRAM controller
- 4Kbyte Instruction/Data cache
- Three-channel DMA controller
- UART/Serial IO
- Parallel port interface controller (PPIC)
- Five 16-bit timers including tone generator and watch dog timer
- Printer interface controller (PIFC)
- Graphic engine unit (GEU)
- Image functional unit including image expander, image rotator, VIS and halftoner
- Programmable I/O ports
- Interrupt controller

FEATURES

Architecture

- Completely integrated system for embedded applications, especially laser beam printers
- Fully 16/32-bit RISC architecture
- Efficient and powerful ARM7TDMI CPU core
- 4-kbyte instruction/data cache
- External bus master mode support
- Cost-effective JTAG-based debug solution

Unified Cache

- 4-Kbyte unified cache
- 2-way set-associative configuration
- Two non-cacheable data regions can be specified
- Cache disable by software
- Four-word depth write buffer

System manager

- 256-Mbyte virtually addressable space support
- 8-bit, 16-bit, or 32-bit external bus support for ROM, SRAM, DRAM, and external I/O
- Separate address and control signals specially for DRAM access, and CAS before RAS refresh, DRAM self-refresh, fast page and EDO DRAM access modes support
- Programmable memory bank size and location definition to provide a flexible memory map.
- Programmable memory access times (2 to 7 waiting cycles)
- Cost-effective memory-to-peripheral interface

DMA

- Three-channel general-purpose DMA controller
- Memory-to-memory, serial port-to/from-memory, parallel port-to/from-memory data transfers without CPU intervention
- Run-length compression/decompression support for memory-to-memory data transfer in CDMA channel
- Initiated by software, peripherals or external DMA request
- Increment or decrement of source or destination addresses, and 8-bit (byte), 16-bit(half-word) or 32-bit (word) data transfer support

UART/SIO

- Two-channel SIO with DMA-based or interrupt-based operation; supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive
- Programmable baud rates
- Loop back mode for testing
- Infra-red (IR) Tx/Rx support

Parallel Port Interface Controller

- DMA-based or interrupt-based operation
- Support IEEE Standard 1284 communication modes (Compatibility mode, nibble mode, byte mode, and ECP mode)
- Hardware support for RLE data compression or decompression in ECP mode
- Automatic hardware handshaking for forward or reverse data transfers in Compatibility and ECP modes.

Timer/Tone Generator/Watch Dog Timer

- Five programmable 16-bit timers, including one tone generator and one watch dog timer
- Watch dog timer output support for system reset
- Interval mode or toggle mode operation support for tone generator

Graphic Engine Unit (GEU)

- Hardware support for up to 256 Bit Block Transfer (Bitblt) operations
- X-Y coordinates support for source, pattern and destination data
- Scanline transfer support to reduce image storage requirements
- Source or pattern flipping
- Band fault check support

Image Functional Block

- Two and three-times image expanding function support
- 90/270 degree rotation support for 16x16 data block
- Variable image scaling operation support
- Halftoning operation support for gray-level image conversion

Printer Interface Controller

- Cost-effective, high-performance DMA-based interface to the printer engine
- Dedicated DMA for fast data transfers between page memory and the printer engine
- Consecutive zero string (Blank data) output for banded bit maps (no memory access required)
- Queuing operation to facilitate smooth switching among data blocks of banded page memory
- Pixel chopping mode support for LBP toner save
- Dot shrinking mode support for fine-edged images printing
- Video data/boundary polarity defining support
- Two to four-times image expanding support

I/O Ports

- 16 programmable I/O ports
- Each port pin can be configured individually as input, output, or I/O for a dedicated signal

Interrupts

- 27 interrupt sources (2 external interrupts included)
- Normal or fast interrupt modes (IRQ, FIQ)

Operating Voltage Range

- 4.75 to 5.25 volts

Operating Frequency

- up-to 33MHz

Package Type

- 208-pin QFP

BLOCK DIAGRAM

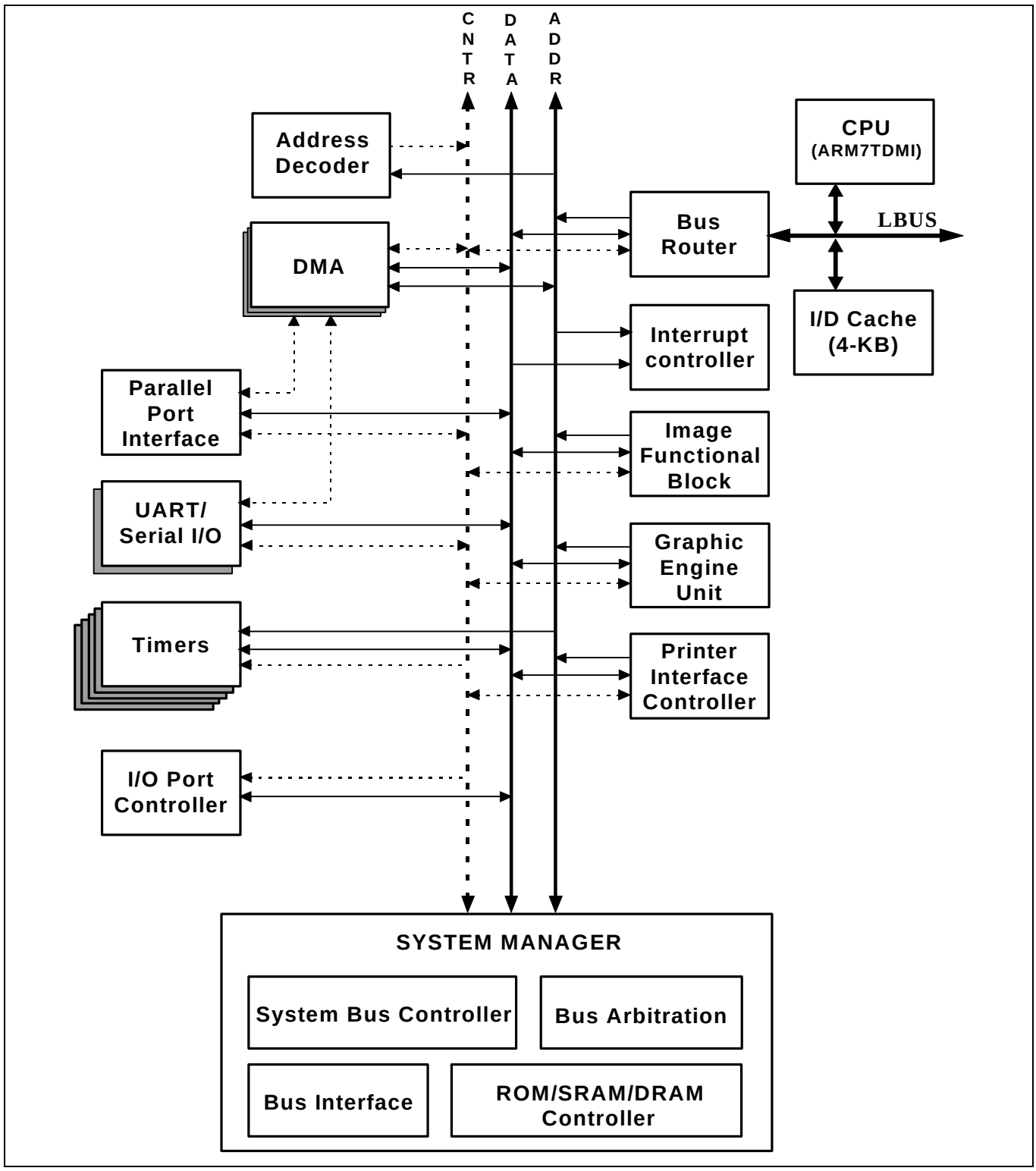

Figure 1-1. KS32C6100 Block Diagram

PIN ASSIGNMENTS

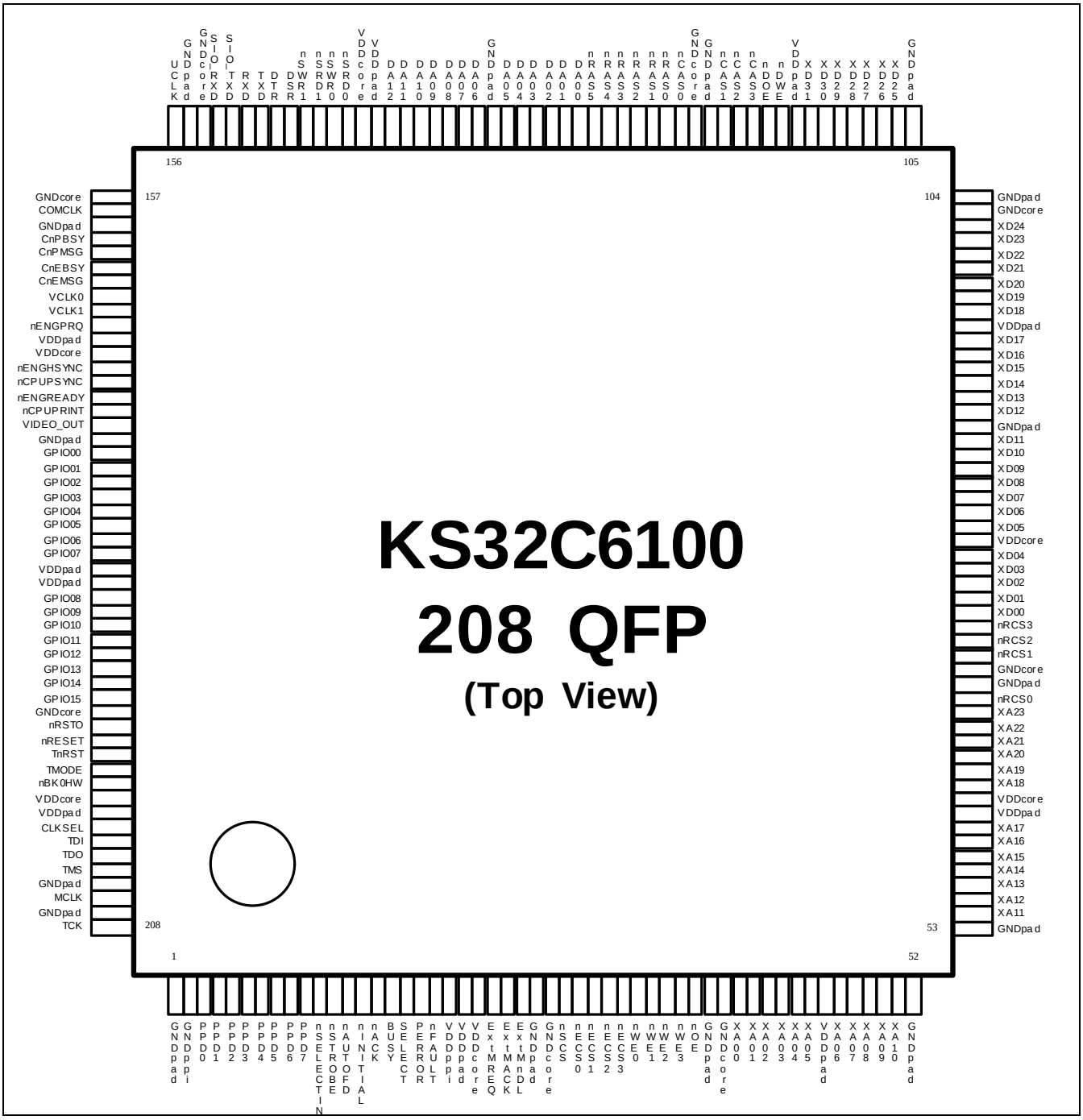

Figure 1-2. KS32C6100 Pin Assignments