INSTRODUCTION

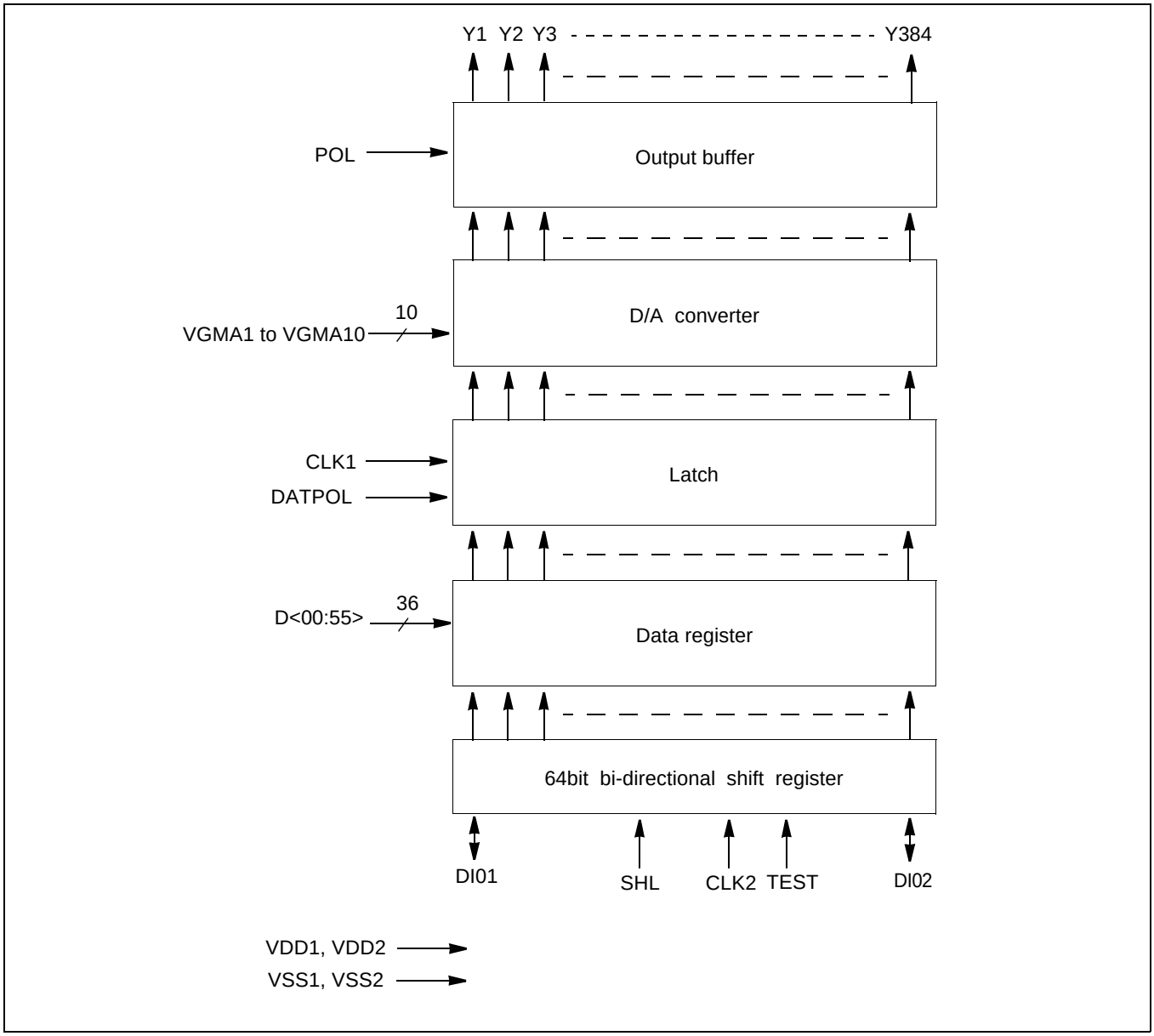
64 G/S 384CH SOURCE DRIVER

The KS0660 is a 384-Channel output, TFT LCD source driver for 64 gray scale displays.
Data input is a digital input consisting of 6 bits by 6 dots, which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected.
This device has an internal D/A (digital-to-analog) converter for each output and utilizes 10 (5×2) external power supplies.
Because the output dynamic range is as large as 6.2 to 9.8 Vp-p, it is unnecessary to operate level inversion of the LCDs common electrode.
Besides, to be able to deal with dot-line inversion when mounted on a single-side, output gray scale voltages with different polarity can be output to the odd number output pins and the even number output pins.
The KS0660 can be adopted to larger panel, and SHL (shift direction selection) pin makes LCD panel connection convenient. Maximum operation clock frequency is 45MHz at a 2.7V logic operation and it can be applied to the TFT LCD panel of XGA to SXGA standards.

FEATURES

- ❑ TFT active matrix LCD source driver LSI
- ❑ 64 outputs are possible through 10 (5×2) external power supply and D/A converter
- ❑ Dot inversion display and, column inversion display line inversion display are possible
- ❑ CMOS level input
- ❑ 6 bit (G/S data) × 6dot(RGB) input (Dual port input)
- ❑ Compatible with γ-correction
- ❑ Input data inversion function.(DATPOL)
- ❑ Logic supply voltage: 2.7 to 3.6V
- ❑ LCD driver supply voltage: 6.4 to 10.0V
- ❑ Output dynamic range: 6.2 to 9.8Vp-p
- ❑ Maximum operating clock frequency: f_{MAX} = 45MHz (internal data transfer speed when operating at 2.7V)
- ❑ Output: 384 outputs
- ❑ Slim type/bent type TCP

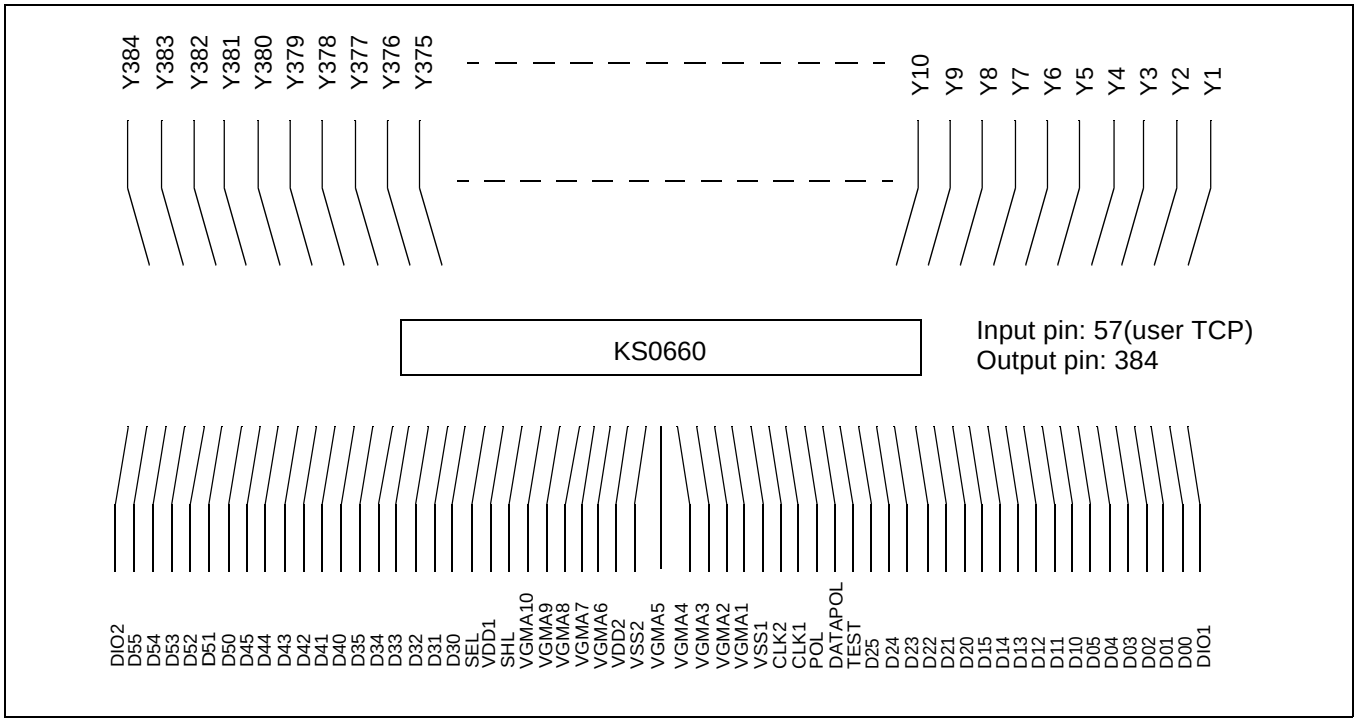
BLOCK DIAGRAM



PIN DESCRIPTION

Pin Symbol	Pin Name	Description
VDD1	Logic power supply	2.7V to 3.6V
VDD2	Driver power supply	6.4V to 10.0V
VSS1	Logic ground	Ground (0V)
VSS2	Driver ground	Ground (0V)
Y1~Y384	Driver Outputs	D/A converted 64G/S analog voltage is output
D0<0:5> D1<0:5> D2<0:5> D3<0:5> D4<0:5> D5<0:5>	Display data input	The display data is input with a width of 36bits, gray scale data (6bit) × 6dot (R. G. B) DX0: LSB, DX5: MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift register is as follows. SHL = H: DI01 input (Y1 → Y384), DI02 output SHL = L: DI02 input (Y384 → Y1), DI01 output
DI01	Right shift/start pulse input/output	SHL=H: Used as the start pulse input pin SHL=L: Used as the start pulse output pin
DI02	Left shift start pulse input/output	SHL=H: Used as the start pulse output pin SHL=L: Used as the start pulse input pin
CLK2	Shift clock input	Refer to shift clock input of the shift register. The display data is loaded to the data register at the rising edge of CLK2.
CLK1	Latch input	Latches the contents of the data register at rising edge and transfers it to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the “Relationship between CLK1 start pulse (DI01, DI02) and blanking period” of the switching characteristic waveform. Outputs the G/S data at falling edge.
VGMA1 to VGMA10	γ–corrected power supplies	Input the γ–corrected power supplies from exernal source. VDD2 ≥ VGMA1>VGMA2>VGMA3> ----- >VGMA9>VGMA10 ≥ VSS2 Keep the γ–corrected power supplies during the gray scale voltage output.
POL	Polarity inverting input	When POL = H, the reference voltages for odd number outputs are VGMA6 to VEMA10 and those for even number outputs are VGMA1 to VGMA5. When POL =L, the reference voltages for odd number outputs are VGMA1 to VGMA5 and those for even number outputs are VGMA6 to VGMA10.
DATPOL	Data inversion input	DATPOL = H: Display data is inverted DATPOL = L: Display data is not inverted. Detects “H” or “L” at rising edge of every CLK2.
SEL	Driving method control input	SEL = L: Dot inversion SEL = H: Column/line inversion
TEST	Test pin	TEST = L: Normal operation TEST = H: TEST MODE → OP AMP CUT-OFF This pin is internally pulled-down. < R_{PD} =. 30kΩ >

TCP PIN CONFIGURATION



NOTES:

1. This figure does not specify the dimensions of the TCP package.
2. This figure shows when you see the chip from the top side(bump side).
3. The SEL pin and TEST pin are not mounted as out lead of the user TCP.
   According to the customer request, it can be a TCP option.SOFD

ABSOLUTE MAXIMUM RATINGS (VSS1=VSS2=0V)

Characteristic	Symbol	Rating	Unit
Digital supply voltage	VDD1	–0.3 to +6.5	V
Analog supply voltage	VDD2	–0.3 to +12.0	V
Input voltage	VGMA1 to 10	–0.3 to VDD2+0.3	V
	Others	–0.3 to VDD1+0.3	
Output voltage	DIO1, DIO2	–0.3 to VDD1+0.3	V
	Y1 to Y384	–0.3 to VDD2+0.3	
Operating power dissipation	Pd	200	mW
Operating Temperature	Topr	–20 to +75	°C
Storage Temperature	Tstg	–55 to +125	°C

* If LSIs are stressed beyond the above absolute maximum ratings, they may be permanently destroyed.
These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the below recommended operating range is not implied.
Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE: Power on sequence: VDD1→ input voltage → VDD2 → VGMA1 to VGMA10

RECOMMENDED OPERATION RANGE (Ta = –20 to +75°C, VSS1 = VSS2 = 0V)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD1	2.7	3.0	3.6	V
Analog supply voltage	VDD2	6.4	9.0	10.0	V
γ–corrected voltage	VGMA1 to VGMA5	0.5VDD2	–	VDD2-0.1	V
	VGMA6 to VGMA10	VSS2 + 0.1	–	0.5VDD2	V
Driver part output voltage	Vyo	+ 0.1	–	VDD2-0.1	V
Max. clock frequency	*Note1 fmax	–	–	45	MHz
Output Load capacitance	CL	–	–	150	pF

NOTE: VDD1 = 2.7V

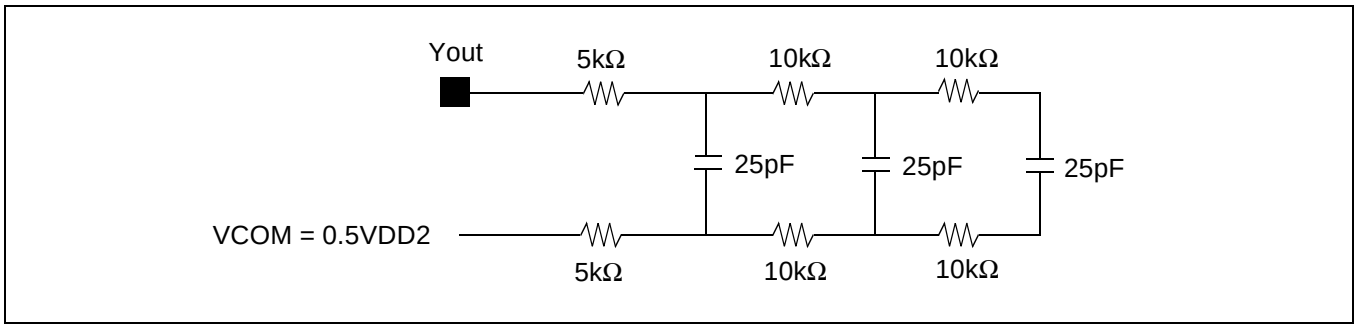
DC CHARACTERISTICS (Ta = –20 TO +75°C, VDD1 = 2.7 to 3.6V, VDD2 = 6.4 to 13.0V, VSS1 = VSS2 = 0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 to D55, DATPOL, CLK1, POL, DIO1(DIO2)	0.8VDD1	–	VDD1	V
Low level input voltage	VIL		0	–	0.2VDD1	
Input leak current	IL	D00 to D55, SHL, CLK2, CLK1 DATPOL, POL	–1	–	1	µA
High level output voltage	VOH	DIO1(DIO2), IO = -1.0mA	VDD1-0.5	–	–	V
Low level output voltge	VOL	DIO1(DIO2), IO = +1.0mA	–	–	0.5	
Resistance between γ-corrected voltage pins	RO to R63	* refer to page 15 resistance ladder circuit	Rn x 0.77	* refer to page 15	Rn x 1.23	Ω
Driver output current	IVOH	VDD2 = 9.0V, Vx= 3.5V, Vyo= 8.0V	–	–0.6	–0.3	mA
	IVOL	VDD2 = 13.0V, Vx= 7.5V, Vyo= 1.5V	0.3	0.6	–	mA
Output voltage deviation	ΔVO	Input: VSS2+0.1V to VSS2+1.5V	–	±20	–	mV
		Input: VSS2+1.5V to VDD2-1.5V	–	±7	± 15	
		Input: VDD2-1.5V to VDD2-0.1V	–	±20	–	
Output voltage range	VYO	Input data: 00H to 3FH	VSS2+0.1	–	VDD2-0.1	V
Logic part dynamic current consumption	IDD1	*Note1: VDD1=3.0V	–	4.0	5.5	mA
Driver part dynamic current consumption	IDD2	VDD1 = 3.0V, VDD2= 9.0V, VGMA1 = 8.5V, VGMA5 = 5.0V VGMA6 = 4.0V, VGMA10 = 0.5V *Note1, *Note2, *Note3	–	6.0	8.0	

(Vyo is the output voltage of analog output pins Y1 to Y384.)
(Vx is the applied voltage of analog output pins Y1 to Y384.)

NOTES:

1. CLK1 cycle = 20µs, fCLK2 = 33MHz,data pattern=1010 ... (Checkerboard pattern) applied, Ta=25°C
2. The current consumption per a driver when XGA single-sided mounting are connected in cascade.
3. Yout Load Condition



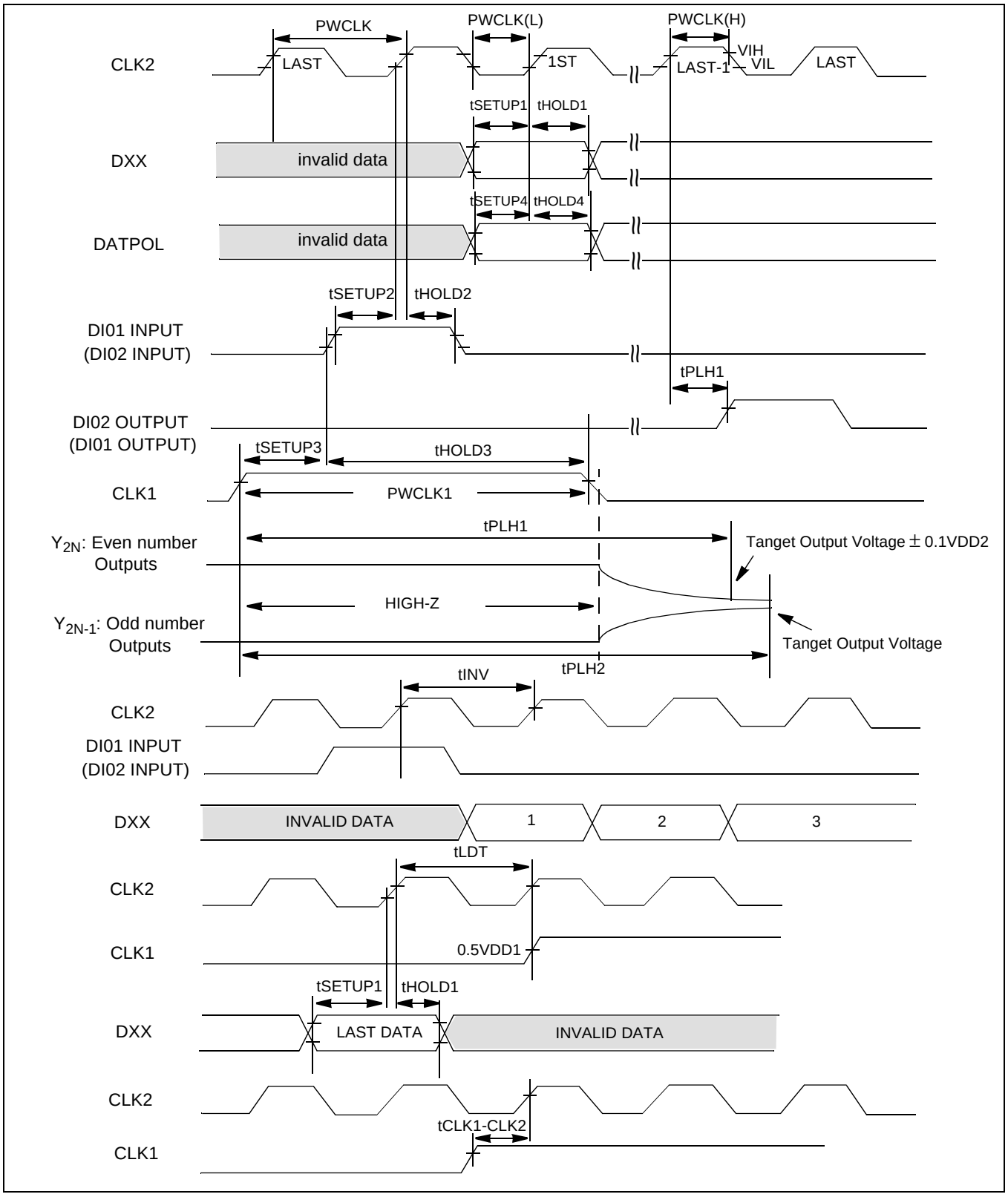
AC CHARACTERISTICS (Ta = –20 to +75°C, VDD1 = 2.7 to 3.6V, VDD2 = 6.4 to 10.0V, VSS1 = VSS2 = 0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	–	22	–	–	ns
Clock pulse low period	PWCLK(L)	–	5	–	–	
Clock pulse high period	PWCLK(H)	–	5	–	–	
Data setup time	tSETUP1	–	5	–	–	
Data hold time	tHOLD1	–	0	–	–	
Start pulse setup time	tSETUP2	–	5	–	–	
Start pulse hold time	tHOLD2	–	0	–	–	
DATPOL-CLK2 setup time	tSETUP 4	–	5	–	–	
DATPOL-CLK2 hold time	tHOLD 4	–	0	–	–	
Start pulse delay time	tPLH1	CL=20pF	-	–	14	
CLK1 setup time	tSETUP3	–	1	–	–	CLK2cycle
CLK1 high pulse width	PWCLK1	–	200	–	–	ns
Driver output delay time 1	tPHL1	refer to Note 3 (page 8), Note 4	-	–	5	µs
Driver output delay time 2	tPHL2	refer to Note 3 (page 8), Note 5	-	–	10	
Data invalid time	tINV	Note 6	1	–	–	CLK2cycle
Last data timing time	tLDT	–	1	–	–	
CLK1-CLK2 time	tCLK1-CLK2	CLK 1 ↑ or ↓ → CLK2 ↑	9	–	–	ns
POL-CLK1 time	tPOL-CLK1	POL ↑ or ↓ → CLK1 ↑	-13	–	–	ns
CLK1-POL time	tCLK1-POL	CLK1 ↓ → POL ↑ or ↓	18	–	–	ns

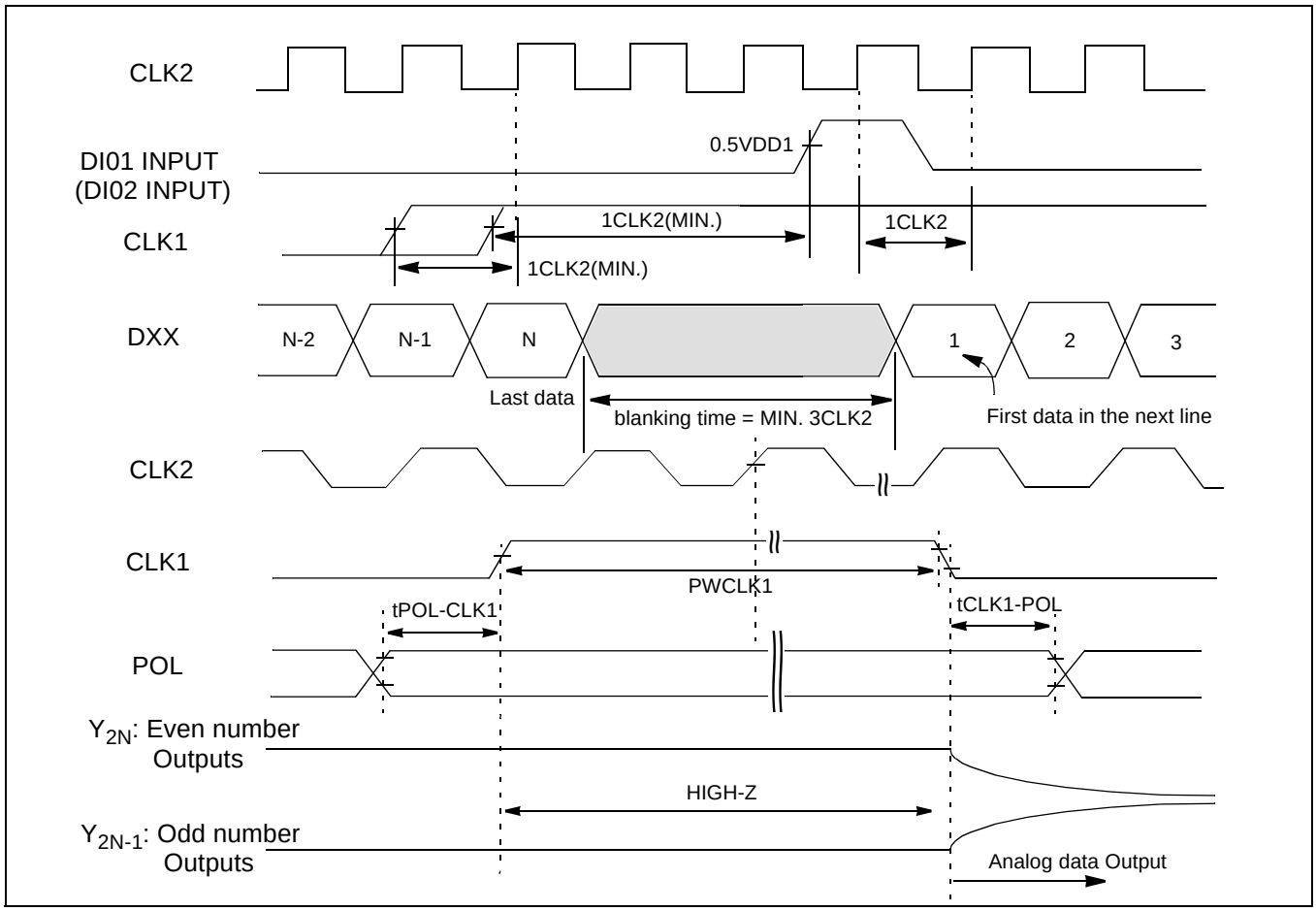
NOTES:

4. The value is specified when the drive voltage value reaches the target output voltage level of 90%.
5. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
6. Set the rising edge of the first CLK2 after the rising edge of DI01 (or DI02).

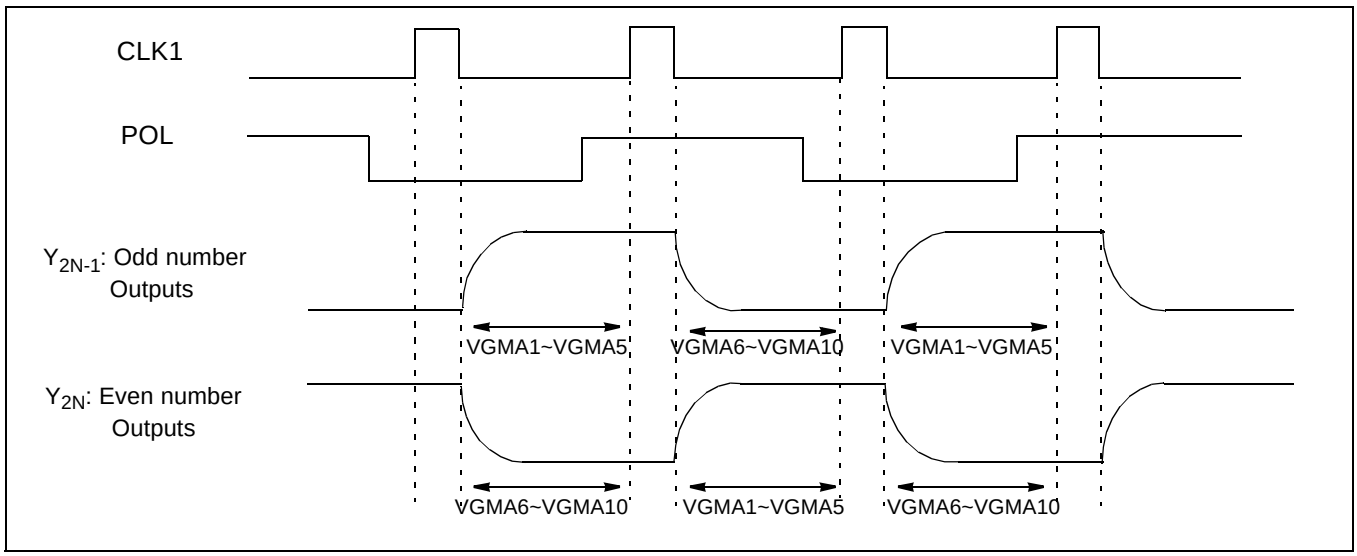
AC Waveform (VIH = 0.8VDD1, VIL= 0.2VDD1)



Relationship between CLK1/start pulse (DIO1, DIO2) and blanking period



Relationship between CLK1, POL and output



RELATIONSHIP BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

Relationship # 1 between Input Data and Output Voltage

Output voltage is decided based on the input data and 10 (5×2)of γ-corrected power supplies (VGMA1 to VGMA10).
Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins.
Among 5-by-2 γ-corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective 5 γ-corrected voltages of VGMA1 to VGMA5 and VGMA 6 to VGMA10.

data format: 1 PIXEL data (6 bits) × 2RGBs (6 dots)
Input width: 36 bits

- Details on display data

DX5	DX4	DX3	DX2	DX1	DX0
upper bits					lower bits

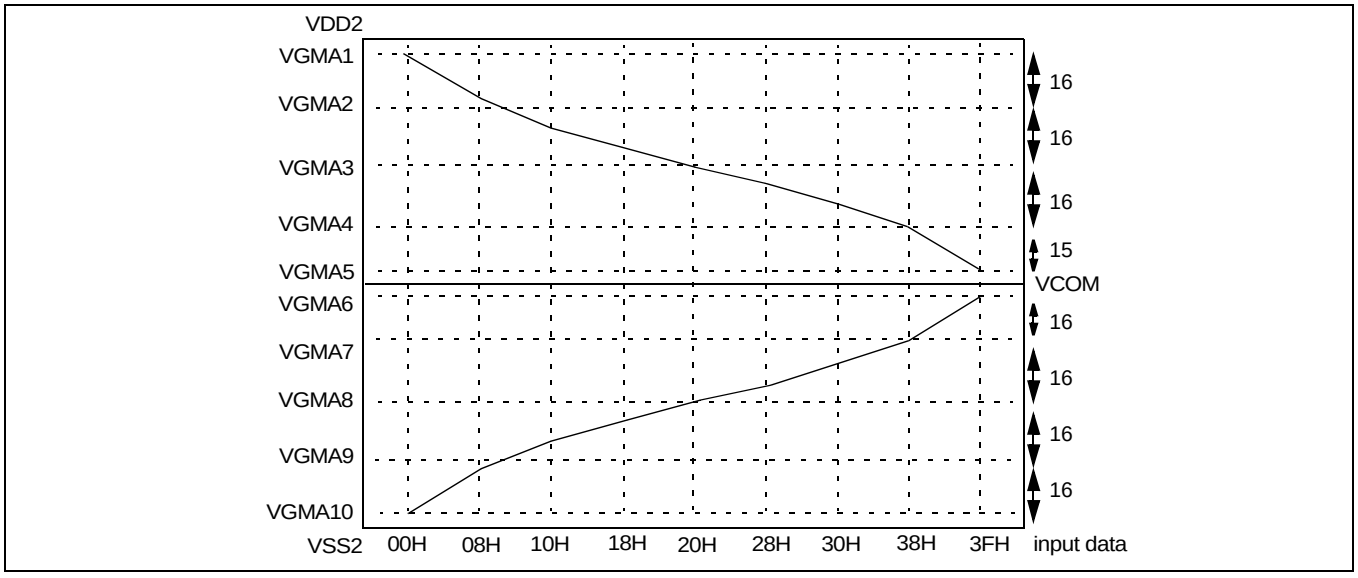
- Relationship between shift direction and output data
  SHL = H (Right shift)

Output	Y1	Y2	Y3	.....	Y382	Y383	Y384
–	First			→	Last		
DATA	D00 to D05	D10 to D15	D20 to D25	.....	D30 to D35	D40 to D45	D50 to 55

SHL = L (Left shift)

Output	Y1	Y2	Y3	.....	Y382	Y383	Y384
–	Last			←	First		
DATA	D00 to D05	D10 to D15	D20 to D25	.....	D30 to D35	D40 to D45	D50 to 55

γ - correction characteristic curve



RELATIONSHIP #2 BETWEEN INPUT DATA AND OUTPUT VOLTAGE (1)

VDD2>VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
00H	0	0	0	0	0	0	V0	VGMA1
01H	0	0	0	0	0	1	V1	VGMA2+(VGMA1-VGMA2)x7250/8050
02H	0	0	0	0	1	0	V2	VGMA2+(VGMA1-VGMA2)x6500/8050
03H	0	0	0	0	1	1	V3	VGMA2+(VGMA1-VGMA2)x5800/8050
04H	0	0	0	1	0	0	V4	VGMA2+(VGMA1-VGMA2)x5150/8050
05H	0	0	0	1	0	1	V5	VGMA2+(VGMA1-VGMA2)x4550/8050
06H	0	0	0	1	1	0	V6	VGMA2+(VGMA1-VGMA2)x4000/8050
07H	0	0	0	1	1	1	V7	VGMA2+(VGMA1-VGMA2)x3450/8050
08H	0	0	1	0	0	0	V8	VGMA2+(VGMA1-VGMA2)x2950/8050
09H	0	0	1	0	0	1	V9	VGMA2+(VGMA1-VGMA2)x2450/8050
0AH	0	0	1	0	1	0	V10	VGMA2+(VGMA1-VGMA2)x2050/8050
0BH	0	0	1	0	1	1	V11	VGMA2+(VGMA1-VGMA2)x1650/8050
0CH	0	0	1	1	0	0	V12	VGMA2+(VGMA1-VGMA2)x1300/8050
0DH	0	0	1	1	0	1	V13	VGMA2+(VGMA1-VGMA2)x950/8050
0EH	0	0	1	1	1	0	V4	VGMA2+(VGMA1-VGMA2)x600/8050
0FH	0	0	1	1	1	1	V15	VGMA2+(VGMA1-VGMA2)x300/8050
10H	0	1	0	0	0	0	V16	VGMA2
11H	0	1	0	0	0	1	V17	VGMA3+(VGMA2-VGMA3)x2450/2750
12H	0	1	0	0	1	0	V18	VGMA3+(VGMA2-VGMA3)x2200/2750
13H	0	1	0	0	1	1	V19	VGMA3+(VGMA2-VGMA3)x1950/2750
14H	0	1	0	1	0	0	V20	VGMA3+(VGMA2-VGMA3)x1700/2750
15H	0	1	0	1	0	1	V21	VGMA3+(VGMA2-VGMA3)x1500/2750
16H	0	1	0	1	1	0	V22	VGMA3+(VGMA2-VGMA3)x1300/2750
17H	0	1	0	1	1	1	V23	VGMA3+(VGMA2-VGMA3)x1100/2750
18H	0	1	1	0	0	0	V24	VGMA3+(VGMA2-VGMA3)x950/2750
19H	0	1	1	0	0	1	V25	VGMA3+(VGMA2-VGMA3)x800/2750
1AH	0	1	1	0	1	0	V26	VGMA3+(VGMA2-VGMA3)x650/2750
1BH	0	1	1	0	1	1	V27	VGMA3+(VGMA2-VGMA3)x500/2750
1CH	0	1	1	1	0	0	V28	VGMA3+(VGMA2-VGMA3)x400/2750
1DH	0	1	1	1	0	1	V29	VGMA3+(VGMA2-VGMA3)x300/2750
1EH	0	1	1	1	1	0	V30	VGMA3+(VGMA2-VGMA3)x200/2750
1FH	0	1	1	1	1	1	V31	VGMA3+(VGMA2-VGMA3)x100/2750

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
20H	1	0	0	0	0	0	V32	VGMA3
21H	1	0	0	0	0	1	V33	VGMA4+(VGMA3-VGMA4)x1500/1600
22H	1	0	0	0	1	0	V34	VGMA4+(VGMA3-VGMA4)x1400/1600
23H	1	0	0	0	1	1	V35	VGMA4+(VGMA3-VGMA4)x1300/1600
24H	1	0	0	1	0	0	V36	VGMA4+(VGMA3-VGMA4)x1200/1600
25H	1	0	0	1	0	1	V37	VGMA4+(VGMA3-VGMA4)x1100/1600
26H	1	0	0	1	1	0	V38	VGMA4+(VGMA3-VGMA4)x1000/1600
27H	1	0	0	1	1	1	V39	VGMA4+(VGMA3-VGMA4)x900/1600
28H	1	0	1	0	0	0	V40	VGMA4+(VGMA3-VGMA4)x800/1600
29H	1	0	1	0	0	1	V41	VGMA4+(VGMA3-VGMA4)x700/1600
2AH	1	0	1	0	1	0	V42	VGMA4+(VGMA3-VGMA4)x600/1600
2BH	1	0	1	0	1	1	V43	VGMA4+(VGMA3-VGMA4)x500/1600
2CH	1	0	1	1	0	0	V44	VGMA4+(VGMA3-VGMA4)x400/1600
2DH	1	0	1	1	0	1	V45	VGMA4+(VGMA3-VGMA4)x300/1600
2EH	1	0	1	1	1	0	V46	VGMA4+(VGMA3-VGMA4)x200/1600
2FH	1	0	1	1	1	1	V47	VGMA4+(VGMA3-VGMA4)x100/1600
30H	1	1	0	0	0	0	V48	VGMA4
31H	1	1	0	0	0	1	V49	VGMA5+(VGMA4-VGMA5)x3350/3450
32H	1	1	1	0	1	0	V50	VGMA5+(VGMA4-VGMA5)x3250/3450
33H	1	1	0	0	1	1	V51	VGMA5+(VGMA4-VGMA5)x3150/3450
34H	1	1	0	1	0	0	V52	VGMA5+(VGMA4-VGMA5)x3050/3450
35H	1	1	0	1	0	1	V53	VGMA5+(VGMA4-VGMA5)x2950/3450
36H	1	1	0	1	1	0	V54	VGMA5+(VGMA4-VGMA5)x2800/3450
37H	1	1	0	1	1	1	V55	VGMA5+(VGMA4-VGMA5)x2650/3450
38H	1	1	1	0	0	0	V56	VGMA5+(VGMA4-VGMA5)x2500/3450
39H	1	1	1	0	0	1	V57	VGMA5+(VGMA4-VGMA5)x2300/3450
3AH	1	1	1	0	1	0	V58	VGMA5+(VGMA4-VGMA5)x2100/3450
3BH	1	1	1	0	1	1	V59	VGMA5+(VGMA4-VGMA5)x1850/3450
3CH	1	1	1	1	0	0	V60	VGMA5+(VGMA4-VGMA5)x1600/3450
3DH	1	1	1	1	0	1	V61	VGMA5+(VGMA4-VGMA5)x1300/3450
3EH	1	1	1	1	1	0	V62	VGMA5+(VGMA4-VGMA5)x800/3450
3FH	1	1	1	1	1	1	V63	VGMA5

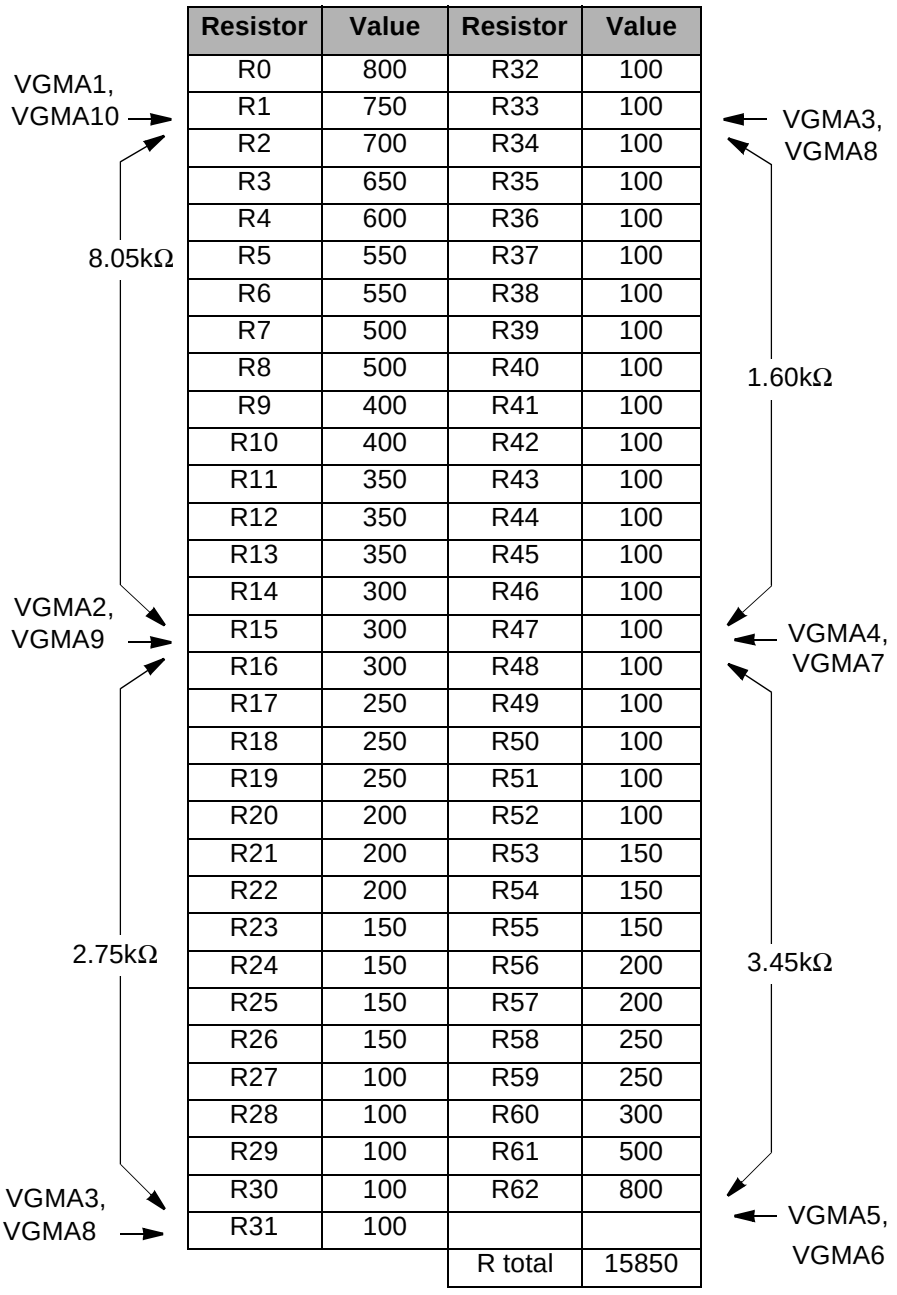
RELATIONSHIP #2 BETWEEN INPUT DATA AND OUTPUT VOLTAGE (2)

VGMA5>VGMA6>VGMA7>VGMA8>VGMA9>VGMA10>VSS2

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
00H	0	0	0	0	0	0	V0’	VGMA10
01H	0	0	0	0	0	1	V1’	VGMA10+(VGMA9-VGMA10)x800/8050
02H	0	0	0	0	1	0	V2’	VGMA10+(VGMA9-VGMA10)x1550/8050
03H	0	0	0	0	1	1	V3’	VGMA10+(VGMA9-VGMA10)x2250/8050
04H	0	0	0	1	0	0	V4’	VGMA10+(VGMA9-VGMA10)x2900/8050
05H	0	0	0	1	0	1	V5’	VGMA10+(VGMA9-VGMA10)x3500/8050
06H	0	0	0	1	1	0	V6’	VGMA10+(VGMA9-VGMA10)x4050/8050
07H	0	0	0	1	1	1	V7’	VGMA10+(VGMA9-VGMA10)x4600/8050
08H	0	0	1	0	0	0	V8’	VGMA10+(VGMA9-VGMA10)x5100/8050
09H	0	0	1	0	0	1	V9’	VGMA10+(VGMA9-VGMA10)x5600/8050
0AH	0	0	1	0	1	0	V10’	VGMA10+(VGMA9-VGMA10)x6000/8050
0BH	0	0	1	0	1	1	V11’	VGMA10+(VGMA9-VGMA10)x6400/8050
0CH	0	0	1	1	0	0	V12’	VGMA10+(VGMA9-VGMA10)x6750/8050
0DH	0	0	1	1	0	1	V13’	VGMA10+(VGMA9-VGMA10)x7100/8050
0EH	0	0	1	1	1	0	V4’	VGMA10+(VGMA9-VGMA10)x7450/8050
0FH	0	0	1	1	1	1	V15’	VGMA10+(VGMA9-VGMA10)x7750/8050
10H	0	1	0	0	0	0	V16’	VGMA9
11H	0	1	0	0	0	1	V17’	VGMA9+(VGMA8-VGMA9)x300/2750
12H	0	1	0	0	1	0	V18’	VGMA9+(VGMA8-VGMA9)x550/2750
13H	0	1	0	0	1	1	V19’	VGMA9+(VGMA8-VGMA9)x800/2750
14H	0	1	0	1	0	0	V20’	VGMA9+(VGMA8-VGMA9)x1050/2750
15H	0	1	0	1	0	1	V21’	VGMA9+(VGMA8-VGMA9)x1250/2750
16H	0	1	0	1	1	0	V22’	VGMA9+(VGMA8-VGMA9)x1450/2750
17H	0	1	0	1	1	1	V23’	VGMA9+(VGMA8-VGMA9)x1650/2750
18H	0	1	1	0	0	0	V24’	VGMA9+(VGMA8-VGMA9)x1800/2750
19H	0	1	1	0	0	1	V25’	VGMA9+(VGMA8-VGMA9)x1950/2750
1AH	0	1	1	0	1	0	V26’	VGMA9+(VGMA8-VGMA9)x2100/2750
1BH	0	1	1	0	1	1	V27’	VGMA9+(VGMA8-VGMA9)x2250/2750
1CH	0	1	1	1	0	0	V28’	VGMA9+(VGMA8-VGMA9)x2350/2750
1DH	0	1	1	1	0	1	V29’	VGMA9+(VGMA8-VGMA9)x2450/2750
1EH	0	1	1	1	1	0	V30’	VGMA9+(VGMA8-VGMA9)x2550/2750
1FH	0	1	1	1	1	1	V31’	VGMA9+(VGMA8-VGMA9)x2650/2750

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
20H	1	0	0	0	0	0	V32’	VGMA8
21H	1	0	0	0	0	1	V33’	VGMA8+(VGMA7-VGMA8)x100/1600
22H	1	0	0	0	1	0	V34’	VGMA8+(VGMA7-VGMA8)x200/1600
23H	1	0	0	0	1	1	V35’	VGMA8+(VGMA7-VGMA8)x300/1600
24H	1	0	0	1	0	0	V36’	VGMA8+(VGMA7-VGMA8)x400/1600
25H	1	0	0	1	0	1	V37’	VGMA8+(VGMA7-VGMA8)x500/1600
26H	1	0	0	1	1	0	V38’	VGMA8+(VGMA7-VGMA8)x600/1600
27H	1	0	0	1	1	1	V39’	VGMA8+(VGMA7-VGMA8)x700/1600
28H	1	0	1	0	0	0	V40’	VGMA8+(VGMA7-VGMA8)x800/1600
29H	1	0	1	0	0	1	V41’	VGMA8+(VGMA7-VGMA8)x900/1600
2AH	1	0	1	0	1	0	V42’	VGMA8+(VGMA7-VGMA8)x1000/1600
2BH	1	0	1	0	1	1	V43’	VGMA8+(VGMA7-VGMA8)x1100/1600
2CH	1	0	1	1	0	0	V44’	VGMA8+(VGMA7-VGMA8)x1200/1600
2DH	1	0	1	1	0	1	V45’	VGMA8+(VGMA7-VGMA8)x1300/1600
2EH	1	0	1	1	1	0	V46’	VGMA8+(VGMA7-VGMA8)x1400/1600
2FH	1	0	1	1	1	1	V47’	VGMA8+(VGMA7-VGMA8)x1500/1600
30H	1	1	0	0	0	0	V48’	VGMA7
31H	1	1	0	0	0	1	V49’	VGMA7+(VGMA6-VGMA7)x100/3450
32H	1	1	1	0	1	0	V50’	VGMA7+(VGMA6-VGMA7)x200/3450
33H	1	1	0	0	1	1	V51’	VGMA7+(VGMA6-VGMA7)x300/3450
34H	1	1	0	1	0	0	V52’	VGMA7+(VGMA6-VGMA7)x400/3450
35H	1	1	0	1	0	1	V53’	VGMA7+(VGMA6-VGMA7)x500/3450
36H	1	1	0	1	1	0	V54’	VGMA7+(VGMA6-VGMA7)x650/3450
37H	1	1	0	1	1	1	V55’	VGMA7+(VGMA6-VGMA7)x800/3450
38H	1	1	1	0	0	0	V56’	VGMA7+(VGMA6-VGMA7)x950/3450
39H	1	1	1	0	0	1	V57’	VGMA7+(VGMA6-VGMA7)x11500/3450
3AH	1	1	1	0	1	0	V58’	VGMA7+(VGMA6-VGMA7)x13500/3450
3BH	1	1	1	0	1	1	V59’	VGMA7+(VGMA6-VGMA7)x16000/3450
3CH	1	1	1	1	0	0	V60’	VGMA7+(VGMA6-VGMA7)x18500/3450
3DH	1	1	1	1	0	1	V61’	VGMA7+(VGMA6-VGMA7)x21500/3450
3EH	1	1	1	1	1	0	V62’	VGMA7+(VGMA6-VGMA7)x26500/3450
3FH	1	1	1	1	1	1	V63’	VGMA6

γ-corrected power circuit and relationship input data and output voltage.
* Ladder Resistance Value (R0 to R63, Unit: Ω, Rn = 15.85kΩ)



Resistor	Value	Resistor	Value
R0	800	R32	100
R1	750	R33	100
R2	700	R34	100
R3	650	R35	100
R4	600	R36	100
R5	550	R37	100
R6	550	R38	100
R7	500	R39	100
R8	500	R40	100
R9	400	R41	100
R10	400	R42	100
R11	350	R43	100
R12	350	R44	100
R13	350	R45	100
R14	300	R46	100
R15	300	R47	100
R16	300	R48	100
R17	250	R49	100
R18	250	R50	100
R19	250	R51	100
R20	200	R52	100
R21	200	R53	150
R22	200	R54	150
R23	150	R55	150
R24	150	R56	200
R25	150	R57	200
R26	150	R58	250
R27	100	R59	250
R28	100	R60	300
R29	100	R61	500
R30	100	R62	800
R31	100		
		R total	15850