Data Sheet | March 2001 | File Number 6005

+3V to +5.5V, 1Microamp, 250kbps, EIA/TIA-562, EIA/TIA-232 Transmitters/Receivers

The Intersil ISL8563 contains 3.0V to 5.5V powered transmitters/receivers which meet EIA/TIA-562 and EIA/TIA-232 specifications, even at V_{CC} = 3.0V. Targeted applications are PDAs, Palmtops, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with a manual powerdown function, reduce the standby supply current to a 1µA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. The ISL8563 is fully compatible with 3.3V only systems, mixed 3.3V and 5.0V systems, and 5.0V only systems.

This product features an improved charge pump which delivers ±5V transmitter supplies, allowing the use of the ISL8563 in RS-562 and RS-232 applications. RS-562 applications will benefit from the improved noise immunity afforded by the ±5V output swing capability.

Table 1 summarizes the features of the device represented by this data sheet, while Application Note AN9863 summarizes the features of each device comprising the 3V RS-232 family.

For a drop-in compatible part with ±15kV ESD protection, please see the ISL8563E data sheet.

Ordering Information

PART NO.	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ISL8563CB	0 to 70	18 Ld SOIC	M18.3
ISL8563CB-T	0 to 70	Tape and Reel	M18.3
ISL8563CP	0 to 70	18 Ld PDIP	E18.3
ISL8563IB	-40 to 85	18 Ld SOIC	M18.3
ISL8563IB-T	-40 to 85	Tape and Reel	M18.3

Features

- Drop in Replacement for MAX563, with Improved Output Voltage (±5V) for Enhanced Noise Immunity
- Available as ±15kV ESD Protected Version (ISL8563E)
- Meets EIA/TIA-562, and EIA/TIA-232 Specifications at 3V
- Latch-Up Free
- On-Chip Voltage Converters Require Only Four External 0.1µF Capacitors
- Receivers Active in Powerdown
- Receiver Hysteresis For Improved Noise Immunity
- Guaranteed Minimum Data Rate 250kbps
- Guaranteed Minimum Slew Rate 4V/µs
- Wide Power Supply Range. . . . . Single +3V to +5.5V
- Low Supply Current in Powerdown State 1µA

Applications

- Any System Requiring RS-562/RS-232 Communication Ports
  - Battery Powered, Hand-Held, and Portable Equipment
  - Laptop Computers, Notebooks, Palmtops
  - Digital Cameras
  - Bar Code Readers

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN9863, “3V to +5.5V, 250K-1Mbps, RS-232 Transmitters/Receivers”

Pinout

ISL8563 (PDIP, SOIC)
TOP VIEW

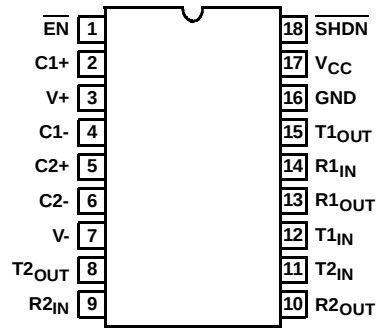


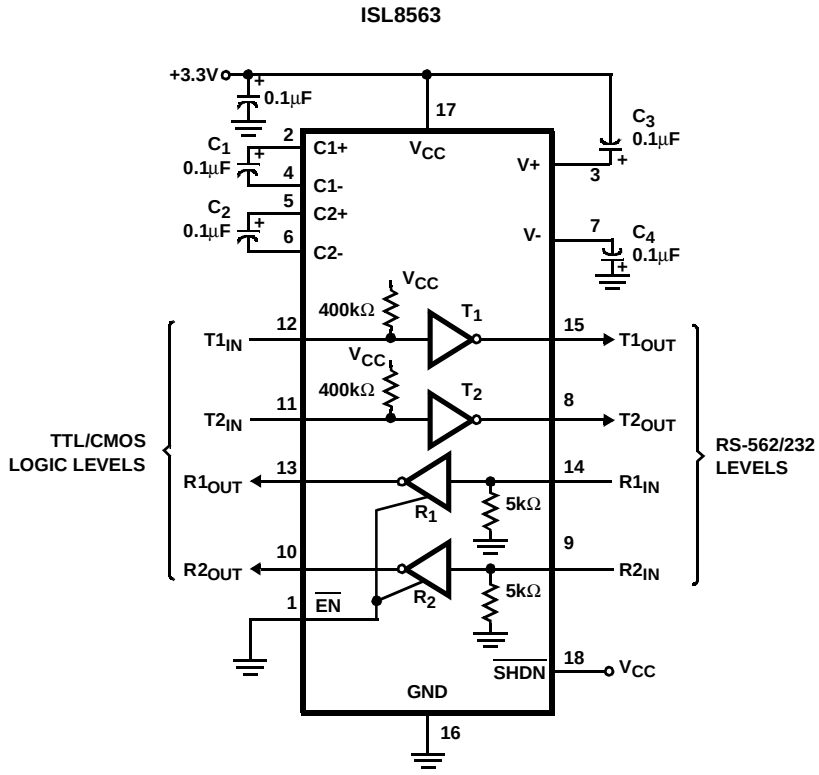
TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF Tx.	NO. OF Rx.	NO. OF MONITOR Rx. (R_{OUTB})	DATA RATE (kbps)	Rx. ENABLE FUNCTION?	READY OUTPUT?	MANUAL POWER-DOWN?	AUTOMATIC POWERDOWN FUNCTION?
ISL8563	2	2	0	250	YES	NO	YES	NO

Pin Descriptions

PIN	FUNCTION
V_{CC}	System Power Supply Input (3.0V to 5.5V).
V+	Internally Generated Positive Transmitter Supply (+5.5V).
V-	Internally Generated Negative Transmitter Supply (-5.5V).
GND	Ground Connection.
C1+	External Capacitor (Voltage Doubler) is connected to this lead.
C1-	External Capacitor (Voltage Doubler) is connected to this lead.
C2+	External Capacitor (Voltage Inverter) is connected to this lead.
C2-	External Capacitor (Voltage Inverter) is connected to this lead.
T_{IN}	TTL/CMOS Compatible Transmitter Inputs with pull-up resistors.
T_{OUT}	RS-562/RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	RS-562/RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS Level Receiver Outputs.
$\overline{EN}$	Active Low Receiver Enable Control.
$\overline{SHDN}$	Active Low Input which shuts down transmitters and on-board power supply, to place device in low power mode.

Typical Operating Circuit



Absolute Maximum Ratings

V_{CC} to Ground . . . . . -0.3V to 6V
V+ to Ground . . . . . -0.3V to 7V
V- to Ground . . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN}, $\overline{EN}$, $\overline{SHDN}$ . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT} . . . . . -0.3V to V_{CC} +0.3V
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
18 Ld PDIP Package	80
18 Ld SOIC Package	75

Moisture Sensitivity (see Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range
ISL8563CX . . . . . 0^{o}C to 70^{o}C
ISL8563IX . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at $T_A = 25^{o}$C

PARAMETER	TEST CONDITIONS		TEMP (^{o}C)	MIN	TYP	MAX	UNITS
RS-562/RS-232 TRANSMITTERS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching and Maintaining ±5V Output Swing		Full	250	500	-	kbps
Input Logic Threshold Low	T_{IN}		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}	V_{CC} = 3.0V to 5.0V	Full	2.4	-	-	V
Transmitter Pull-Up Input Current	T_{IN}	$\overline{SHDN}$ = V_{CC}	Full	-	2	20	µA
		$\overline{SHDN}$ = GND	Full	-	±0.01	±1.0	µA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3.6V to 5.5V, $\overline{SHDN}$ = GND		Full	-	-	±10	µA
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current	V_{OUT} = 0V		Full	-	±35	±60	mA
RS-562/RS-232 RECEIVERS							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		Full	-	1.2	0.6	V
	V_{CC} = 5.0V		Full	-	1.5	0.8	V
Input Threshold High	V_{CC} = 3.3V		Full	2.4	1.5	-	V
	V_{CC} = 5.0V		Full	2.4	1.8	-	V
Input Hysteresis	V_{CC} = 3.0V to 3.6V		Full	0.1	0.5	1.0	V
Input Resistance			Full	3	5	7	kΩ
Output Voltage Low	I_{OUT} = 3.2mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} -0.6	V_{CC} -0.1	-	V
Output Leakage Current	$\overline{EN}$ = V_{CC}		Full	-	±0.05	±10	µA
$\overline{EN}$ Input Logic Threshold Low			Full	-	-	0.8	V
$\overline{EN}$ Input Logic Threshold High	V_{CC} = 3.0V to 5.0V		Full	2.4	-	-	V
POWER SUPPLY							
Operating Supply Voltage			Full	3.0	-	5.5	V
Supply Current	$\overline{SHDN}$ = V_{CC}	All Outputs Unloaded	Full	-	0.5	6.0	mA
		All Outputs loaded, R_L = 3kΩ	25	-	14	-	mA
Supply Current, Powerdown	$\overline{SHDN}$ = GND		25	-	1	10	µA
			Full	-	1	25	µA
$\overline{SHDN}$ Input Leakage Current			Full	-	±0.01	±1.0	µA

Electrical Specifications Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Input Logic Threshold Low			Full	-	-	0.8	V
$\overline{SHDN}$ Input Logic Threshold High	V_{CC} = 3.0V to 5.0V		Full	2.4	-	-	V
AC CHARACTERISTICS							
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured From 3V to -3V or -3V to 3V, C_L = 50pF to 2500pF		25	4	-	30	V/µs
Transmitter Propagation Delay	Transmitter Input to Transmitter Output, C_L = 1000pF, R_L = 3kΩ	t_{PHL} (Note 2)	Full	-	1	3.5	µs
		t_{PLH} (Note 2)	Full	-	1	3.5	µs
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL} (Note 3)	Full	-	0.3	1.0	µs
		t_{PLH} (Note 3)	Full	-	0.3	1.0	µs
Receiver Output Enable Time	Figure 1	t_{ER}	Full	-	125	500	ns
Receiver Output Disable Time	Figure 1	t_{DR}	Full	-	160	500	ns
Transmitter Output Enable Time	Figure 2	t_{ET}	25	-	17	-	µs
Transmitter Output Disable Time	Figure 2	t_{DT}	25	-	600	-	ns
Transmitter Skew	t_{PHL} - t_{PLH} (Note 2)		25	-	100	-	ns
Receiver Skew	t_{PHL} - t_{PLH} (Note 3)		25	-	100	-	ns
ESD PERFORMANCE							
RS-562 Pins (T_{OUT}, R_{IN})	Human Body Model		25	-	±15	-	kV
	IEC1000-4-2 Contact Discharge		25	-	±8	-	kV
	IEC1000-4-2 Air Gap Discharge		25	-	±8	-	kV
All Other Pins	Human Body Model		25	-	±3	-	kV

NOTES:

2. Transmitter is measured at the transmitter zero crossing points.
3. Receiver is measured at the receiver 50 percent crossing points.

Test Waveforms

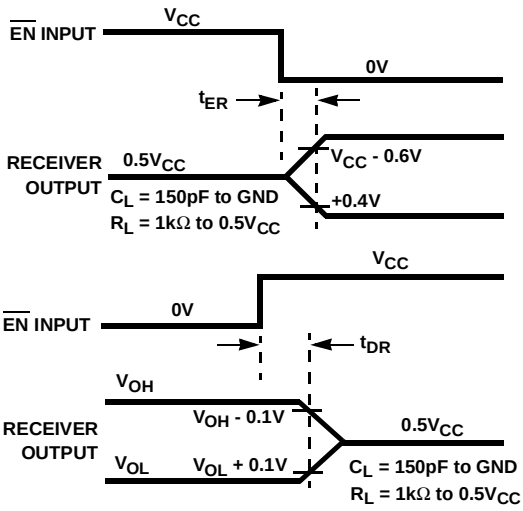


FIGURE 1. RECEIVER OUTPUT ENABLE AND DISABLE TIMING

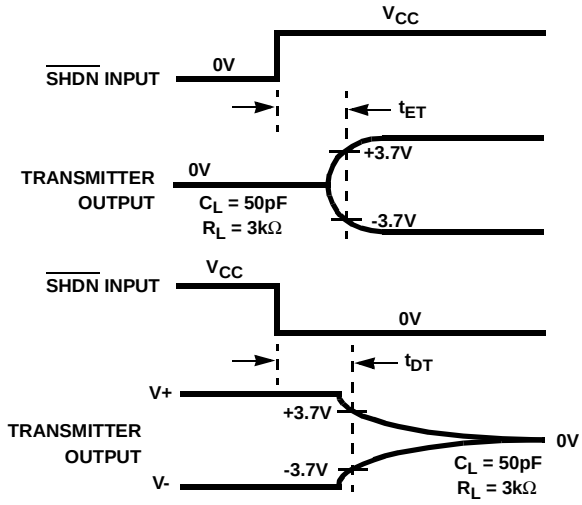


FIGURE 2. TRANSMITTER OUTPUT ENABLE AND DISABLE TIMING

Detailed Description

The ISL8563 operates from a single +3V to +5.5V supply, guarantees a 250kbps minimum data rate, requires only four small external 0.1µF capacitors, features low power consumption, and meets all EIA/TIA-562 and EIA/TIA-232 specifications. The circuit is divided into three sections: The charge pump, the transmitters, and the receivers.

Charge-Pump

Intersil's new ISL8563 utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions over the full V_{CC} range. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-562/232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-562/232 levels over a wide range of single supply system voltages.

All transmitter outputs disable and assume a high impedance state when the device enters the powerdown mode (see Table 2). These outputs may be driven to ±12V when disabled.

All devices guarantee a 250kbps data rate (V_{OUT} = ±5V) for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 900kbps.

Unused transmitter inputs may be left unconnected because they will be pulled to V_{CC} by the on-chip pull-up resistors. Forcing the ISL8563 into power down disables the pull-up resistors to further minimize power.

Receivers

The ISL8563 contains standard inverting receivers that three-state via the $\overline{EN}$ control line. All the receivers convert RS-562/232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 3) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis (even in powerdown) to increase noise immunity and decrease errors due to slow input signal transitions.

The ISL8563 inverting receivers disable only when $\overline{EN}$ is driven high. Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 4 and 5).

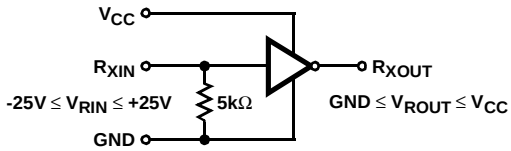


FIGURE 3. INVERTING RECEIVER CONNECTIONS

Powerdown Functionality

This 3V device requires a nominal supply current of 0.3mA during normal operation (not in powerdown mode). This is considerably less than the 5mA to 11mA current required by 5V devices. The already low current requirement drops significantly when the device enters powerdown mode. In powerdown, supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), the transmitter outputs three-state, and the transmitter input pull-ups disable. This micro-power mode makes the ISL8563 ideal for battery powered and portable applications.

Software Controlled (Manual) Powerdown

The ISL8563, is forced into its low power, stand by state via a simple shutdown ($\overline{SHDN}$) pin. Driving this pin high enables normal operation, while driving it low forces the IC into its powerdown state. Connect $\overline{SHDN}$ to V_{CC} if the powerdown function isn't needed. Note that all the receiver outputs remain enabled during shutdown (see Table 2). For the lowest power consumption during powerdown, the receivers should also be disabled by driving the $\overline{EN}$ input high (see next section, and Figures 4 and 5). The time required to exit powerdown, and resume transmission is less than 30µs.

Receiver ENABLE Control

The device also features an $\overline{EN}$ input to control the receiver outputs. Driving $\overline{EN}$ high disables all the receiver outputs placing them in a high impedance state. This is useful to eliminate supply current, due to a receiver output forward biasing the protection diode, when driving the input of a powered down (V_{CC} = GND) peripheral (see Figure 4). The enable input has no effect on transmitters.

TABLE 2. POWERDOWN AND ENABLE LOGIC TRUTH TABLE

$\overline{SHDN}$ INPUT	$\overline{EN}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	MODE OF OPERATION
L	L	High-Z	Active	Manual Powerdown
L	H	High-Z	High-Z	Manual Powerdown w/Rcvr. Disabled
H	L	Active	Active	Normal Operation
H	H	Active	High-Z	Normal Operation w/Rcvr. Disabled

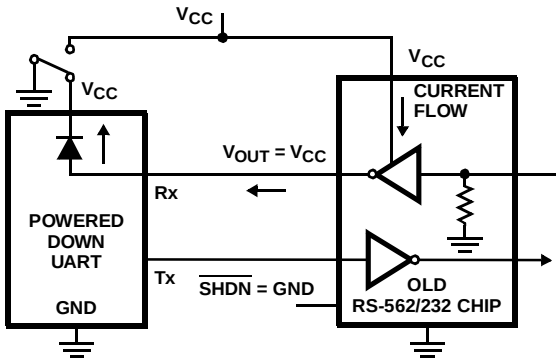


FIGURE 4. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

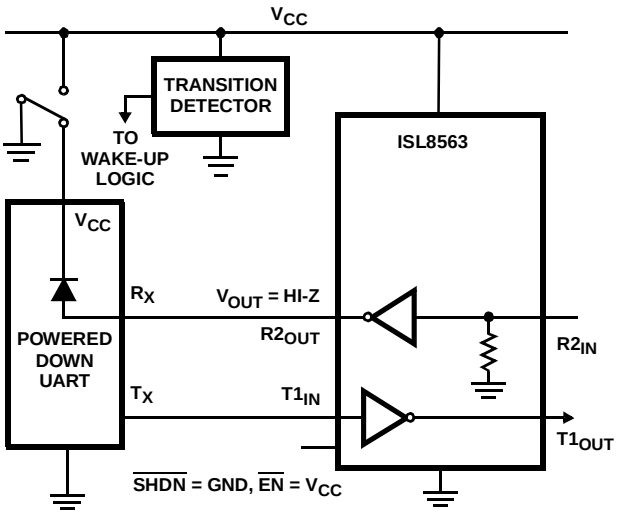


FIGURE 5. DISABLED RECEIVERS PREVENT POWER DRAIN

Capacitor Selection

The charge pumps operate with 0.1µF (or greater) capacitors for $3.0V \le V_{CC} \le 5.5V$. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value, however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Transmitter Outputs When Exiting Powerdown

Figure 6 shows the response of two transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-562/232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

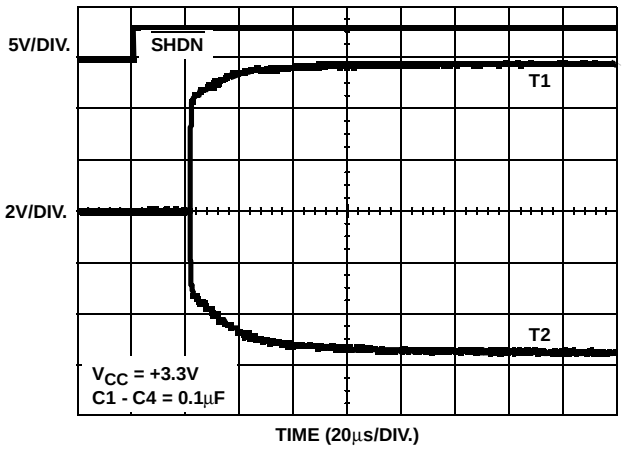


FIGURE 6. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN

High Data Rates

The ISL8563 maintains the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 7 details a transmitter loopback test circuit, and Figure 8 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 9 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

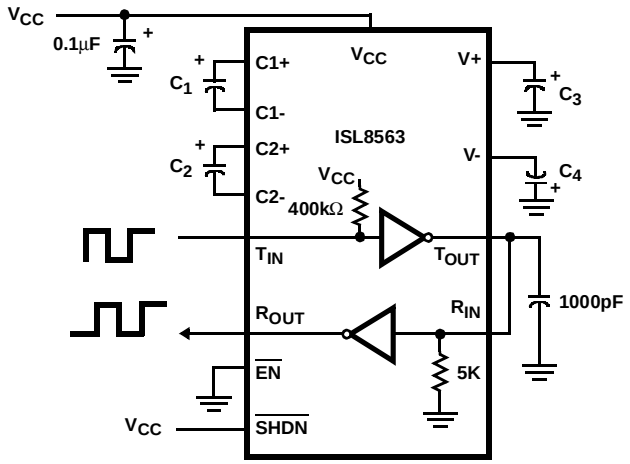


FIGURE 7. TRANSMITTER LOOPBACK TEST CIRCUIT

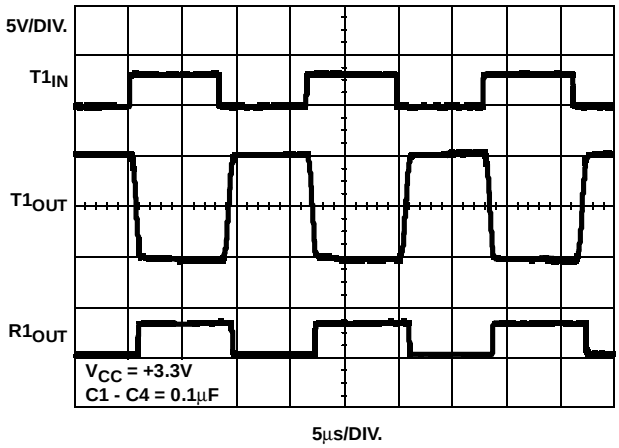


FIGURE 8. LOOPBACK TEST AT 120kbps

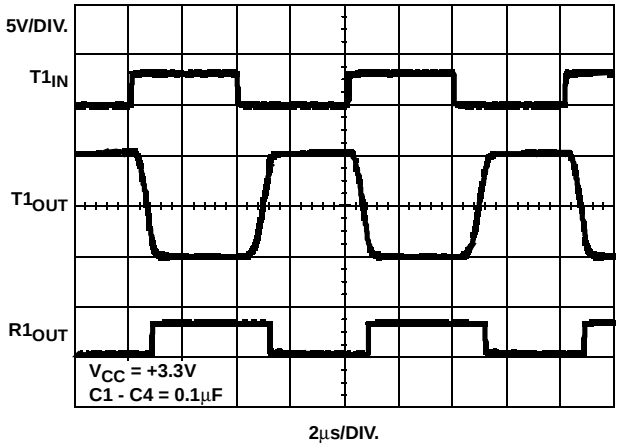


FIGURE 9. LOOPBACK TEST AT 250kbps

Interconnection with 3V and 5V Logic

The ISL8563 directly interface with most 5V logic families, including ACT and HCT CMOS. See Table 3 for more information on possible combinations of interconnections.

TABLE 3. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. Incompatible with AC, HC, or CD4000 CMOS.

Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C

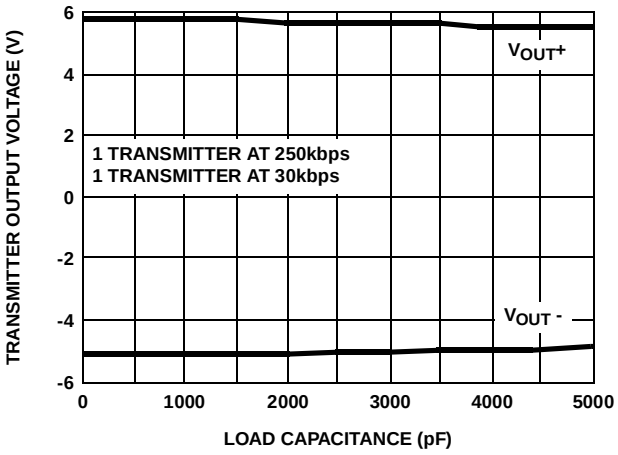


FIGURE 10. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

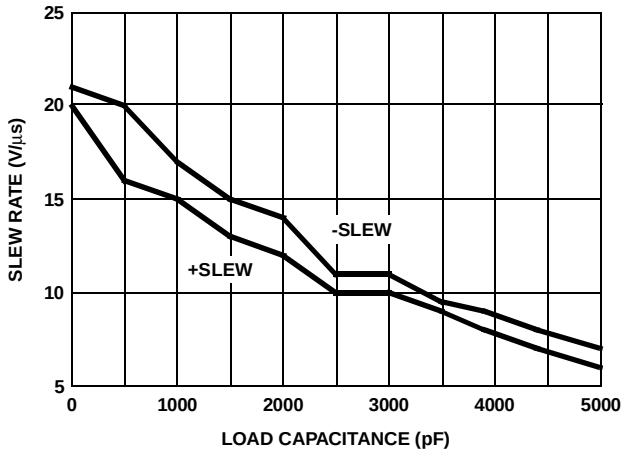


FIGURE 11. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C (Continued)

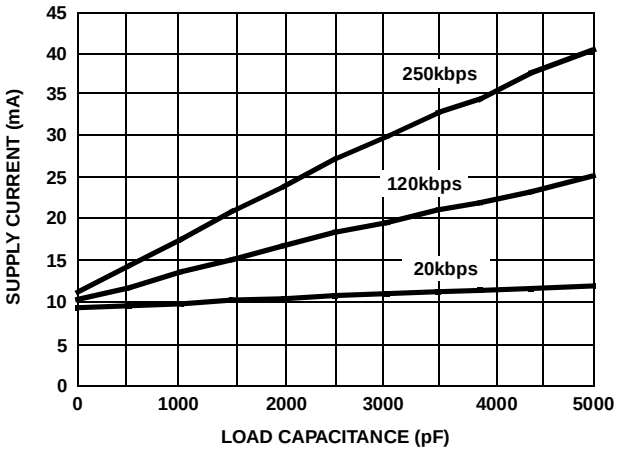


FIGURE 12. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

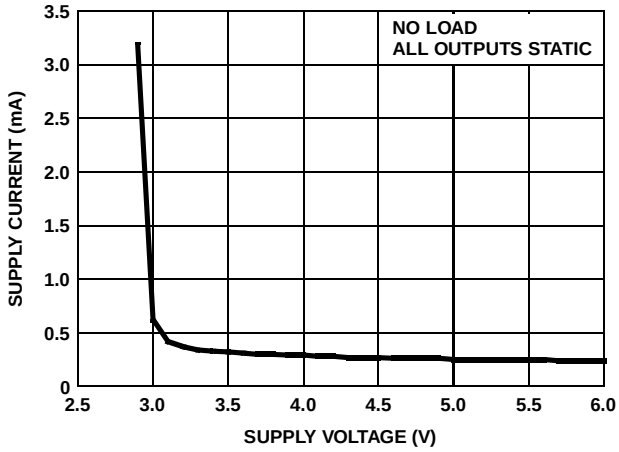


FIGURE 13. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

100 mils x 100 mils (2540µm x 2540µm)

METALLIZATION:

Type: Metal 1: AlSi(1%)
Thickness: Metal 1: 8kÅ
Type: Metal 2: AlSi (1%)
Thickness: Metal 2: 10kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Floating

PASSIVATION:

Type: Silox
Thickness: 13kÅ

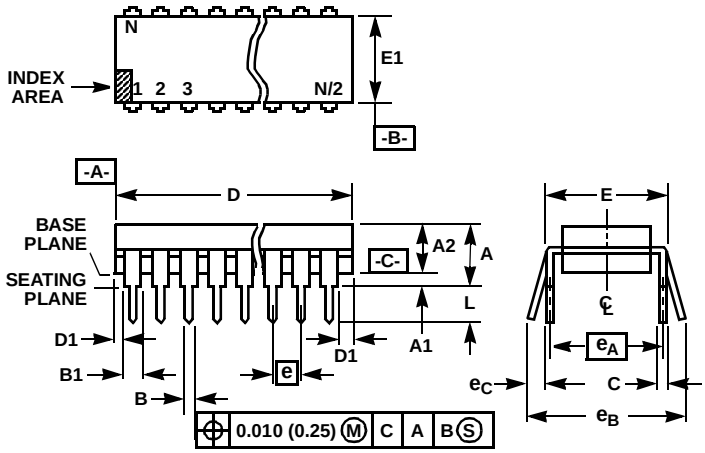
TRANSISTOR COUNT:

338

PROCESS:

Si Gate CMOS

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

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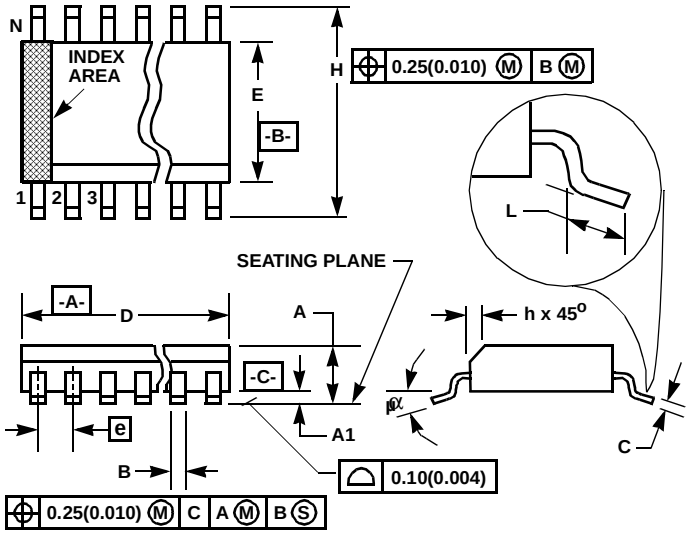
Small Outline Plastic Packages (SOIC)



M18.3 (JEDEC MS-013-AB ISSUE C)
18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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