

# IR4426/IR4427/IR4428

## DUAL LOW SIDE DRIVER

### Features

- Gate drive supply range from 6 to 20V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs (IR4426)
- Outputs in phase with inputs (IR4427)
- OutputA out of phase with inputA and OutputB in phase with inputB (IR4428)

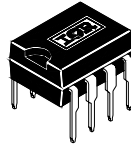
### Descriptions

The IR4426/IR4427/IR4428 is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

### Product Summary

$I_{O+/-}$	1.5A / 1.5A
$V_{OUT}$	6V - 20V
$t_{on/off}$ (typ.)	85 & 65 ns

### Packages

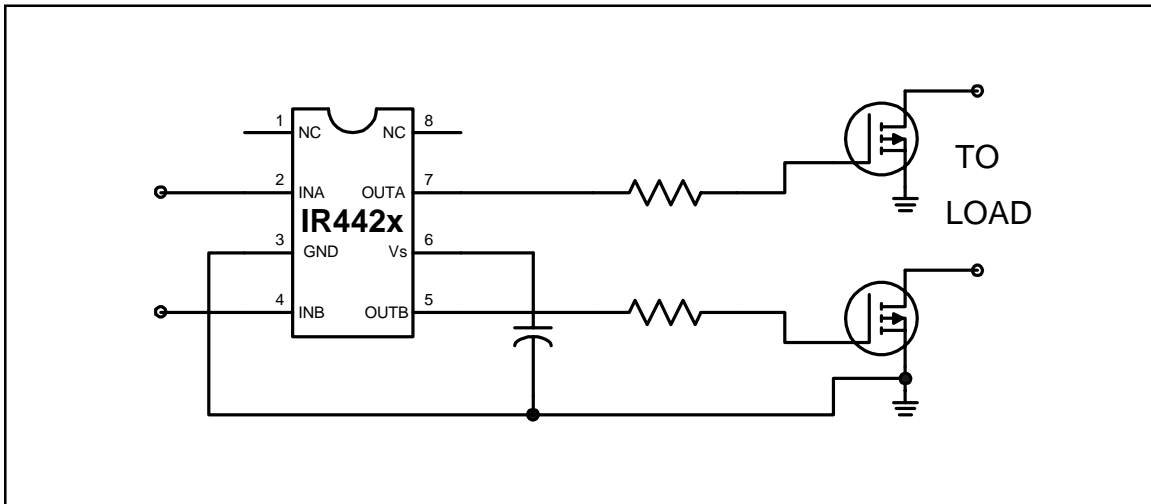


8 Lead PDIP



8 Lead SOIC

### Block Diagram



### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>S</sub>	Fixed supply voltage	-0.3	25	V	
V <sub>O</sub>	Output voltage	-0.3	V <sub>S</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage	-0.3	V <sub>S</sub> + 0.3		
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

### Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V <sub>S</sub>	Fixed supply voltage	6	20	V
V <sub>O</sub>	Output voltage	0	V <sub>S</sub>	
V <sub>IN</sub>	Logic input voltage	0	V <sub>S</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

### DC Electrical Characteristics

V<sub>BIAS</sub> (V<sub>S</sub>) = 15V, T<sub>A</sub> = 25°C unless otherwise specified. The V<sub>IN</sub> and I<sub>IN</sub> parameters are referenced to GND and are applicable to input leads: INA and INB. The V<sub>O</sub> and I<sub>O</sub> parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V <sub>IH</sub>	Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4426)	2.7	—	—	V	
	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4427)					
	Logic "0" input voltage (OUTA=LO), Logic "1" input voltage (OUTB=HI) (IR4428)					

**DC Electrical Characteristics cont.**

$V_{BIAS} (V_S) = 15V$ ,  $T_A = 25^\circ C$  unless otherwise specified. The  $V_{IN}$ , and  $I_{IN}$  parameters are referenced to GND and are applicable to input leads: INA and INB. The  $V_O$  and  $I_O$  parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

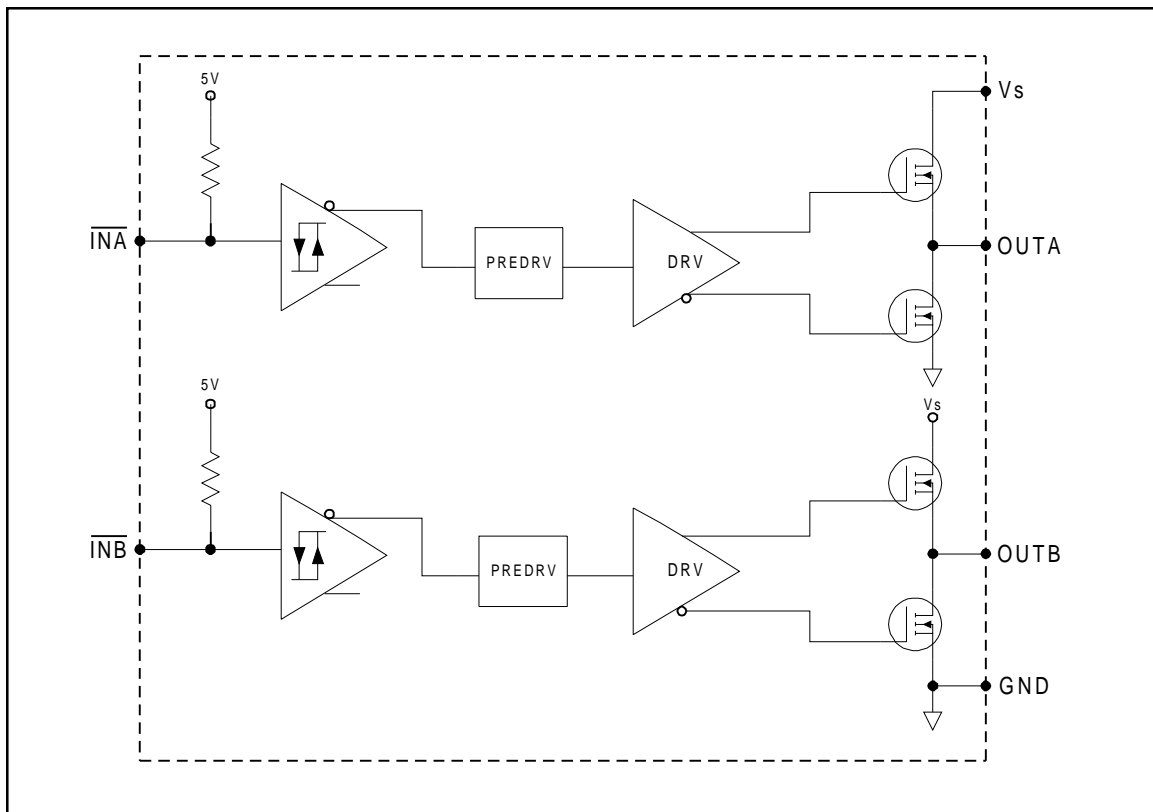
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IL}$	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4426) Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4427) Logic "1" input voltage (OUTA=HI), Logic "0" input voltage (OUTB=LO) (IR4428)	—	—	0.8	V	
$V_{OH}$	High level output voltage, $V_{BIAS}-V_O$	—	—	1.2		
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.1		
$I_{IN+}$	Logic "1" input bias current (OUT=HI)	—	5	15	μA	$V_{IN} = 0V$ (IR4426) $V_{IN} = V_S$ (IR4427) $V_{INA} = 0V$ (IR4428) $V_{INB} = V_S$ (IR4428)
$I_{IN-}$	Logic "0" input bias current (OUT=LO)	—	-10	-30		$V_{IN} = V_S$ (IR4426) $V_{IN} = 0V$ (IR4427) $V_{INA} = V_S$ (IR4428) $V_{INB} = 0V$ (IR4428)
$I_{QS}$	Quiescent $V_S$ supply current	—	100	200		$V_{IN} = 0V$ or $V_S$
$I_{O+}$	Output high short circuit pulsed current	1.5	2.3	—	A	$V_O = 0V, V_{IN} = 0$ (IR4426) $V_O = 0V, V_{IN} = V_S$ (IR4427) $V_O = 0V, V_{INA} = 0$ (IR4428) $V_O = 0V, V_{INB} = V_S$ (IR4428) $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	1.5	3.3	—		$V_O = 15V, V_{IN} = V_S$ (IR4426) $V_O = 15V, V_{IN} = 0$ (IR4427) $V_O = 15V, V_{INA} = V_S$ (IR4428) $V_O = 15V, V_{INB} = 0$ (IR4428) $PW \leq 10 \mu s$

**AC Electrical Characteristics**

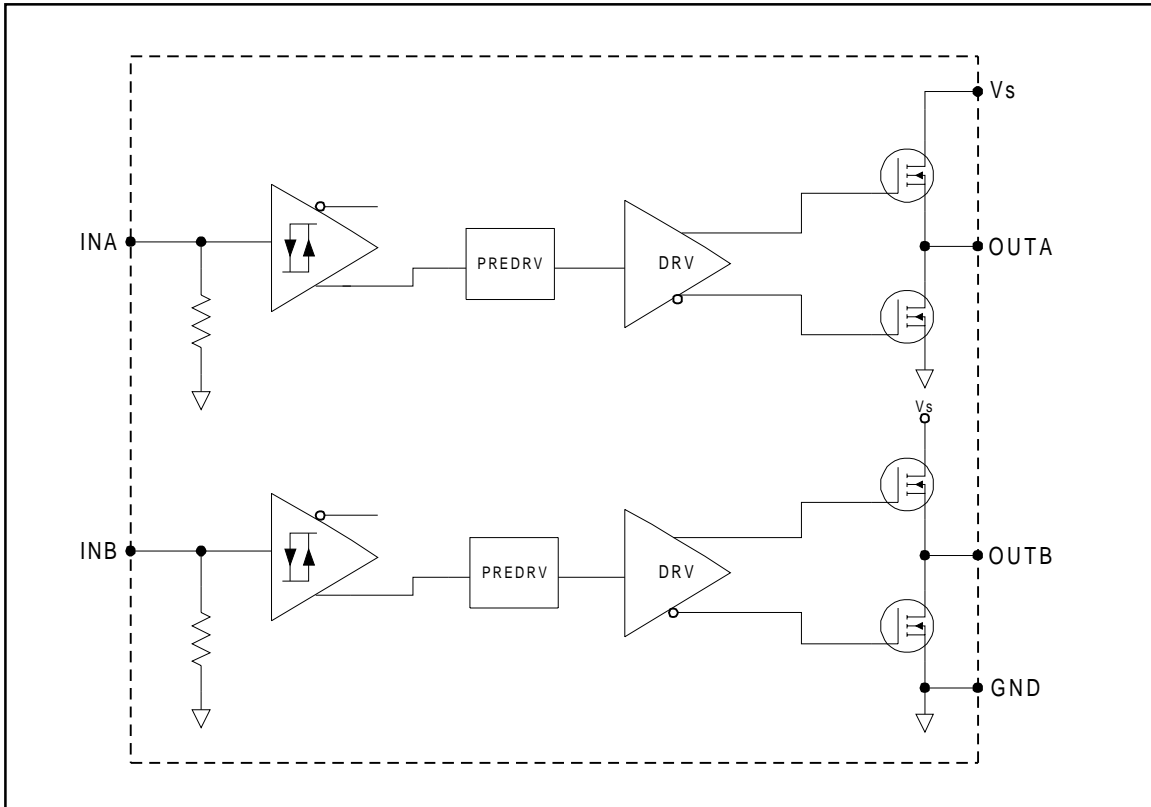
$V_{BIAS} (V_S) = 15V$ ,  $C_L = 1000pF$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
<b>Propagation delay characteristics</b>						
$t_{d1}$	Turn-on propagation delay	—	85	160	ns	figure 4
$t_{d2}$	Turn-off propagation delay	—	65	150		
$t_r$	Turn-on rise time	—	15	35		
$t_f$	Turn-off fall time	—	10	25		

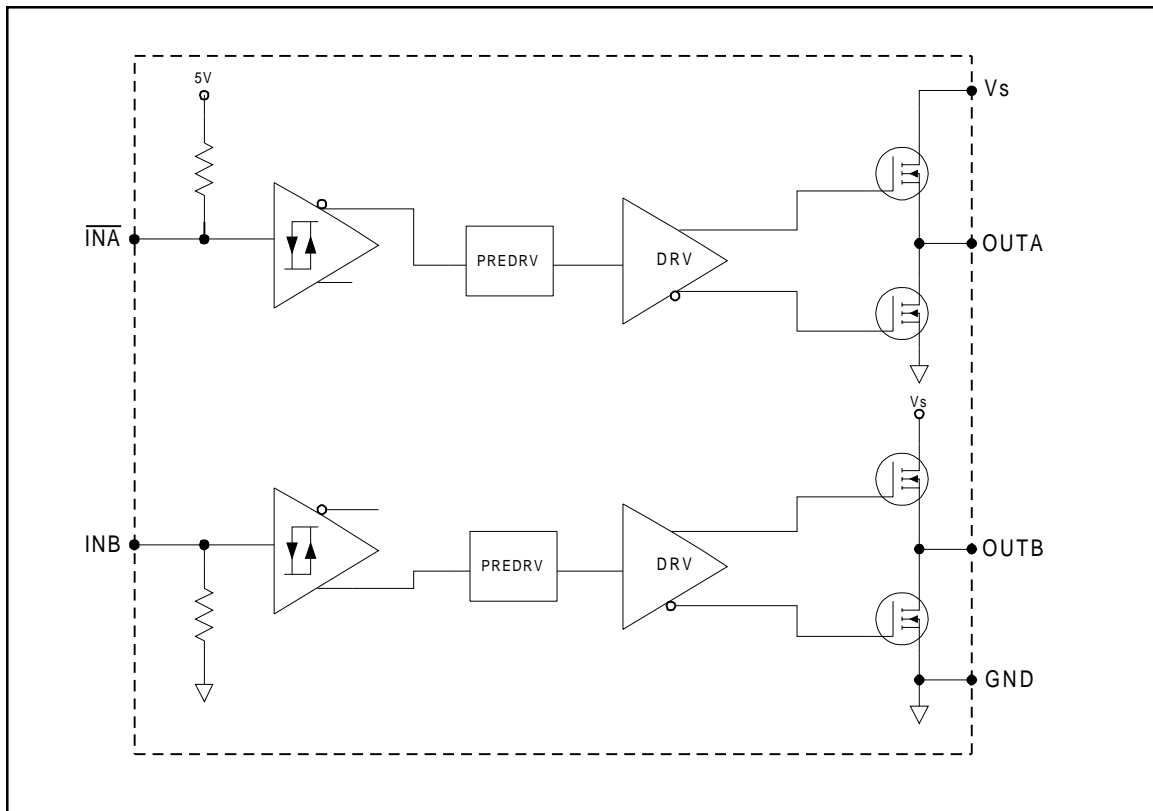
**Functional Block Diagram IR4426**



**Functional Block Diagram IR4427**



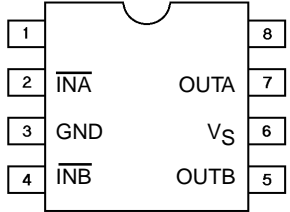
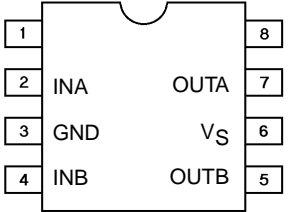
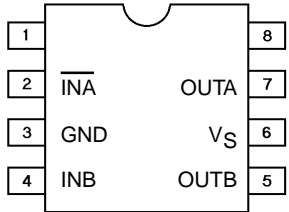
Functional Block Diagram IR4428



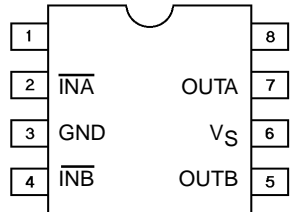
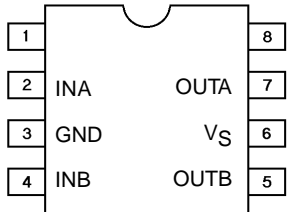
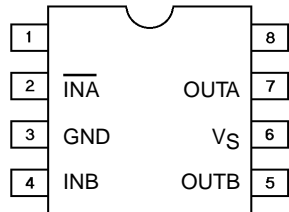
Lead Definitions

Symbol	Description
V <sub>s</sub>	Supply voltage
GND	Ground
INA	Logic input for gate driver output (OUTA), out of phase (IR4426, IR4428), in phase (IR4427)
INB	Logic input for gate driver output (OUTB), out of phase (IR4426), in phase (IR4427, IR4428)
OUTA	Gate drive output A
OUTB	Gate drive output B

**Lead Assignments**

 <p>8 Lead PDIP</p>	 <p>8 Lead PDIP</p>	 <p>8 Lead PDIP</p>
<b>IR4426</b>	<b>IR4427</b>	<b>IR4428</b>
<b>Part Number</b>		

**Lead Assignments**

 <p>8 Lead SOIC</p>	 <p>8 Lead SOIC</p>	 <p>8 Lead SOIC</p>
<b>IR4426S</b>	<b>IR4427S</b>	<b>IR4428S</b>
<b>Part Number</b>		

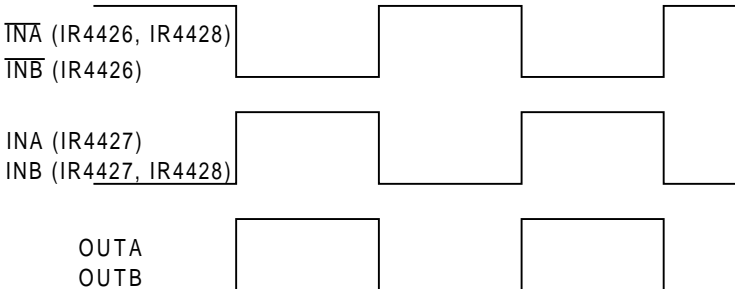


Figure 3. Timing Diagram

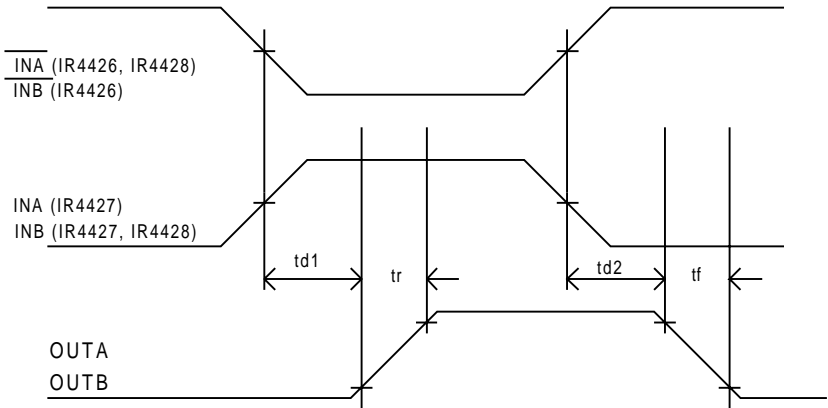


Figure 4. Switching Time Waveforms



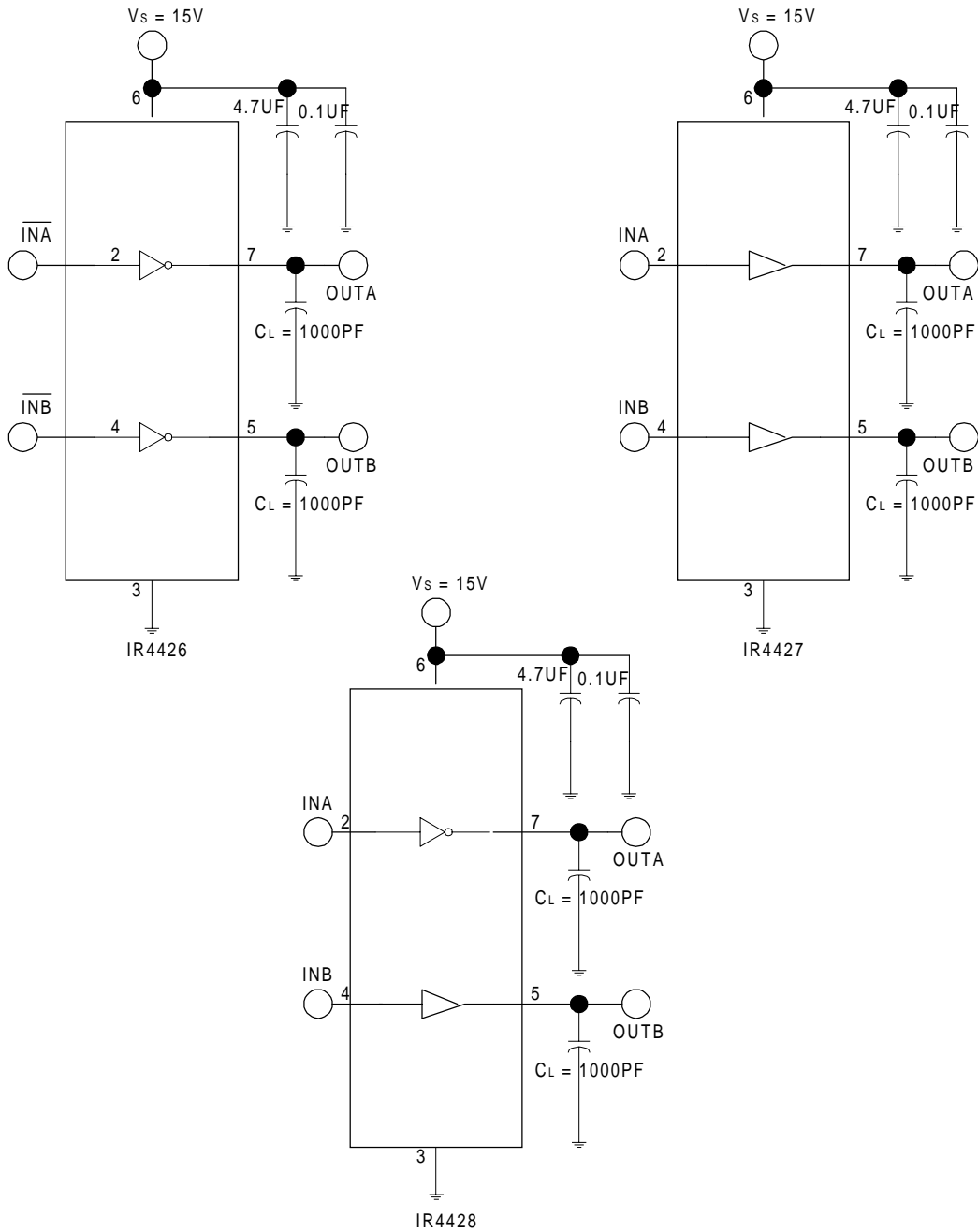
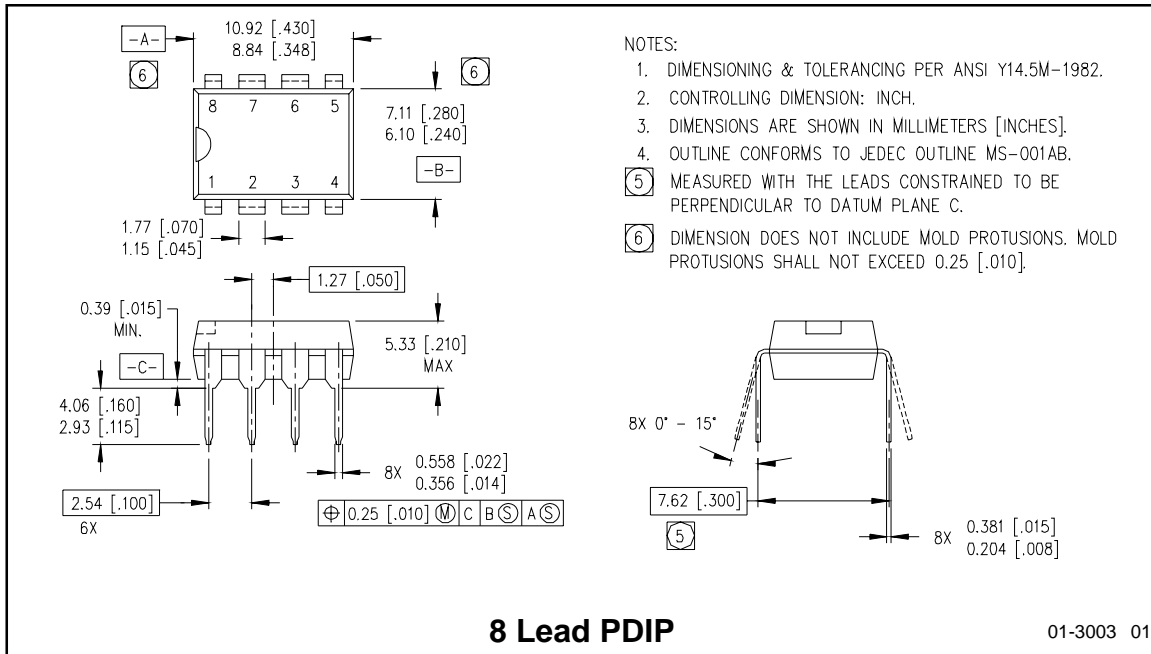
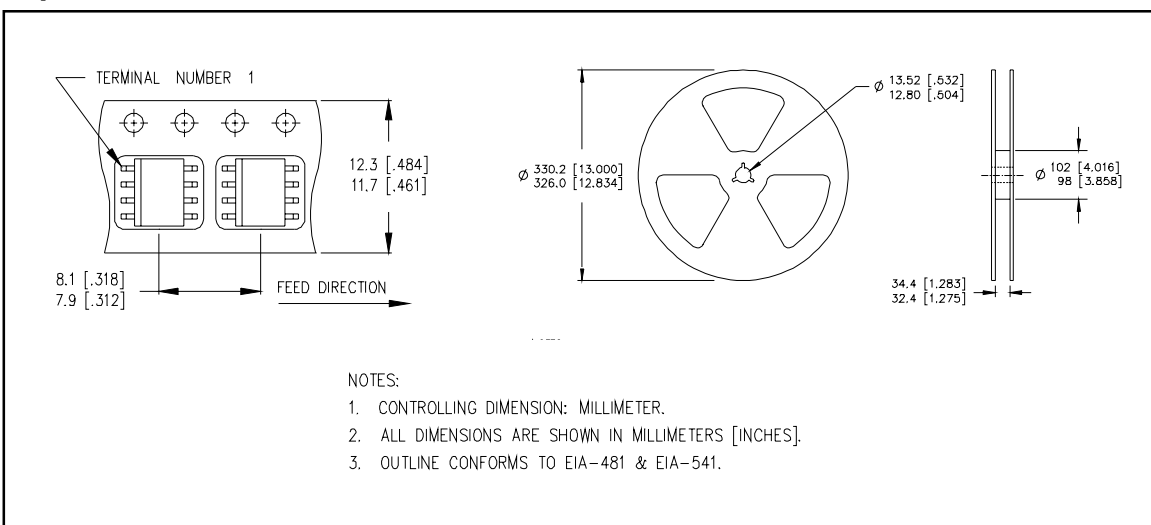


Figure 5. Switching Time Test Circuits

Caseoutline



Tape & Reel



Case Outline - 8 Lead SOIC

