

IR2118

SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output out of phase with input

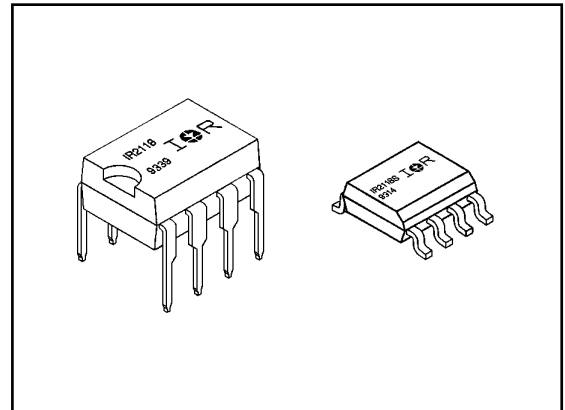
Product Summary

| | |
|----------------------------|-----------------|
| V_{OFFSET} | 600V max. |
| $I_{\text{O+/-}}$ | 200 mA / 420 mA |
| V_{OUT} | 10 - 20V |
| $t_{\text{on/off (typ.)}}$ | 125 & 105 ns |

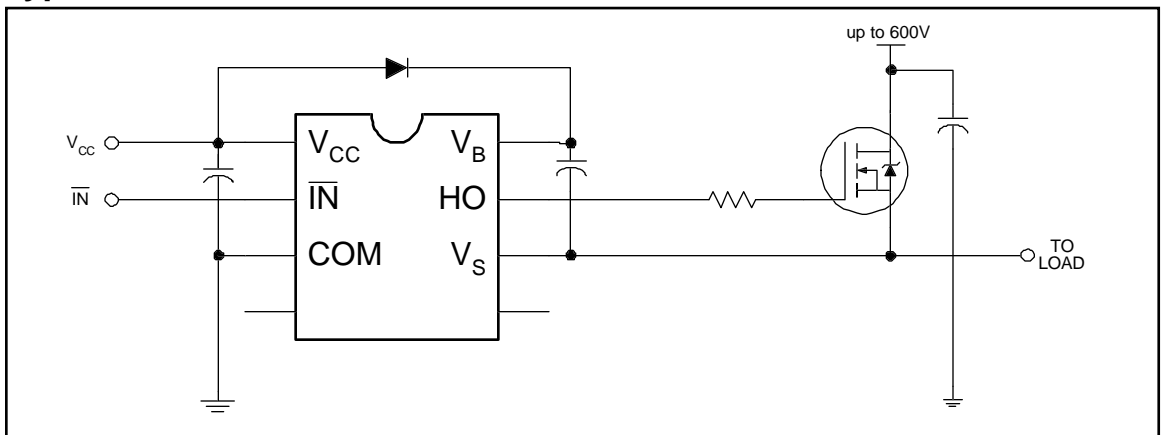
Description

The IR2118 is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 600 volts.

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 5 through 8.

| Symbol | Parameter Definition | Value | | Units |
|---------------------|---|----------------------|-----------------------|-------|
| | | Min. | Max. | |
| V _B | High Side Floating Supply Voltage | -0.3 | 625 | V |
| V _S | High Side Floating Supply Offset Voltage | V _B - 25 | V _B + 0.3 | |
| V _{HO} | High Side Floating Output Voltage | V _S - 0.3 | V _B + 0.3 | |
| V _{CC} | Logic Supply Voltage -0.3 | 25 | | |
| V _{IN} | Logic Input Voltage | -0.3 | V _{CC} + 0.3 | |
| dV _S /dt | Allowable Offset Supply Voltage Transient (Figure 2) | — | 50 | V/ns |
| P _D | Package Power Dissipation @ T _A ≤ +25°C (8 Lead DIP) | — | 1.0 | W |
| | (8 Lead SOIC) | — | 0.625 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (8 Lead DIP) | — | 125 | °C/W |
| | (8 Lead SOIC) | — | 200 | |
| T _J | Junction Temperature | — | 150 | °C |
| T _S | Storage Temperature | -55 | 150 | |
| T _L | Lead Temperature (Soldering, 10 seconds) | — | 300 | |

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

| Symbol | Parameter Definition | Value | | Units |
|-----------------|--|---------------------|---------------------|-------|
| | | Min. | Max. | |
| V _B | High Side Floating Supply Absolute Voltage | V _S + 10 | V _S + 20 | V |
| V _S | High Side Floating Supply Offset Voltage | Note 1 | 600 | |
| V _{HO} | High Side Floating Output Voltage | V _S | V _B | |
| V _{CC} | Logic Supply Voltage | 10 | 20 | |
| V _{IN} | Logic Input Voltage | 0 | V _{CC} | |
| T _A | Ambient Temperature | -40 | 125 | °C |

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

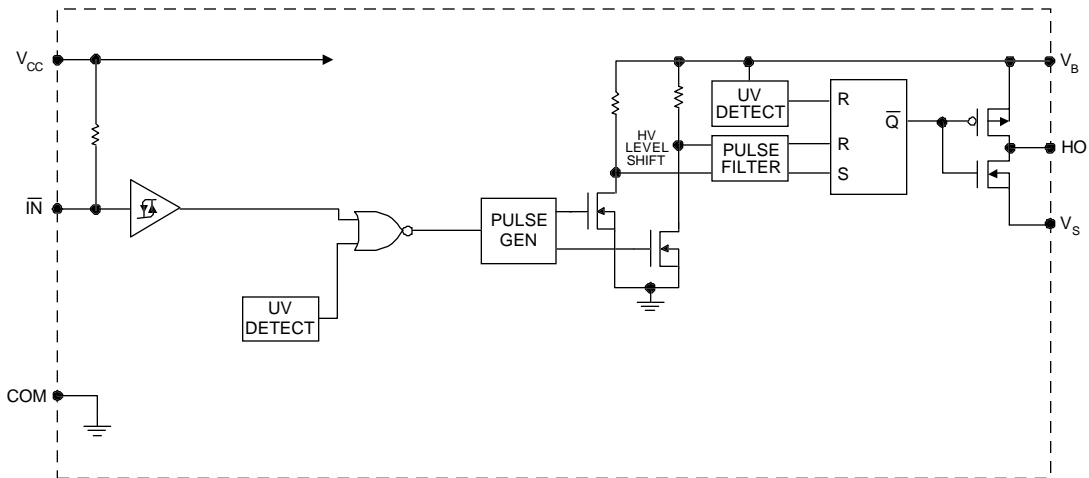
| Symbol | Parameter Definition | Value | | | Units | Test Conditions |
|-----------|----------------------------|-------|------|------|-------|-----------------|
| | | Min. | Typ. | Max. | | |
| t_{on} | Turn-On Propagation Delay | — | 125 | 200 | ns | $V_S = 0V$ |
| t_{off} | Turn-Off Propagation Delay | — | 105 | 180 | | $V_S = 600V$ |
| t_r | Turn-On Rise Time | — | 80 | 130 | | |
| t_f | Turn-Off Fall Time | — | 40 | 65 | | |

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Parameter Definition | Value | | | Units | Test Conditions |
|-------------|---|-------|------|------|---------|--|
| | | Min. | Typ. | Max. | | |
| V_{IH} | Logic "0" Input Voltage | 6.4 | — | — | V | $V_{CC} = 10V$ |
| | | 9.5 | — | — | | $V_{CC} = 15V$ |
| | | 12.6 | — | — | | $V_{CC} = 20V$ |
| V_{IL} | Logic "1" Input Voltage | — | — | 3.8 | | $V_{CC} = 10V$ |
| | | — | — | 6.0 | | $V_{CC} = 15V$ |
| | | — | — | 8.3 | | $V_{CC} = 20V$ |
| V_{OH} | High Level Output Voltage, $V_{BIAS} - V_O$ | — | — | 100 | mV | $I_O = 0A$ |
| V_{OL} | Low Level Output Voltage, V_O | — | — | 100 | | $I_O = 0A$ |
| I_{LK} | Offset Supply Leakage Current | — | — | 50 | μA | $V_B = V_S = 600V$ |
| I_{QBS} | Quiescent V_{BS} Supply Current | — | 50 | 240 | | $V_{IN} = 0V$ or V_{CC} |
| I_{QCC} | Quiescent V_{CC} Supply Current | — | 70 | 340 | | $V_{IN} = 0V$ or V_{CC} |
| I_{IN+} | Logic "1" Input Bias Current | — | — | 1.0 | | $V_{IN} = 0V$ |
| I_{IN-} | Logic "0" Input Bias Current | — | 20 | 40 | | $V_{IN} = 15V$ |
| V_{BSUV+} | V_{BS} Supply Undervoltage Positive Going Threshold | 7.6 | 8.6 | 9.6 | V | |
| V_{BSUV-} | V_{BS} Supply Undervoltage Negative Going Threshold | 7.2 | 8.2 | 9.2 | | |
| V_{CCUV+} | V_{CC} Supply Undervoltage Positive Going Threshold | 7.6 | 8.6 | 9.6 | | |
| V_{CCUV-} | V_{CC} Supply Undervoltage Negative Going Threshold | 7.2 | 8.2 | 9.2 | | |
| I_{O+} | Output High Short Circuit Pulsed Current | 200 | 250 | — | mA | $V_O = 0V, V_{IN} = 0V$ $PW \leq 10 \mu s$ |
| I_{O-} | Output Low Short Circuit Pulsed Current | 420 | 500 | — | | $V_O = 15V, V_{IN} = V_{CC}$ $PW \leq 10 \mu s$ |

Functional Block Diagram



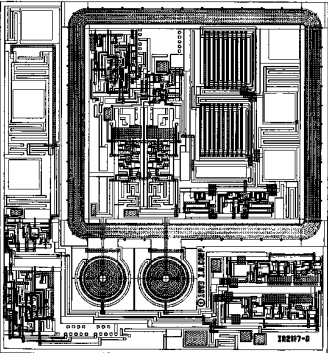
Lead Definitions

| Lead | |
|-----------------|---|
| Symbol | Description |
| V _{CC} | Logic and gate drive supply |
| IN | Logic input for gate driver output (HO), out of phase with HO |
| COM | Low side return |
| V _B | High side floating supply |
| HO | High side gate drive output |
| V _S | High side floating supply return |

Lead Assignments

| | |
|--|-----------------------------------|
| <p>8 Lead DIP</p> <p>IR2118</p> | <p>SO-8</p> <p>IR2118S</p> |
| Part Number | |

Device Information

| | | |
|-------------------------|-------------------------------|--|
| Process & Design Rule | | HVDCMOS 4.0 μ m |
| Transistor Count | | 114 |
| Die Size | | 70 X 77 X 26 (mil) |
| Die Outline | |  |
| Thickness of Gate Oxide | | 800Å |
| Connections | Material | Poly Silicon |
| | First Layer | Width Spacing Thickness |
| | | 4 μ m 6 μ m 5000Å |
| Second Layer | Material | Al - Si (Si: 1.0% \pm 0.1%) |
| | Width Spacing Thickness | 6 μ m 9 μ m 20,000Å |
| Contact Hole Dimension | | 8 μ m X 8 μ m |
| Insulation Layer | Material | PSG (SiO ₂) |
| | Thickness | 1.5 μ m |
| Passivation | Material | PSG (SiO ₂) |
| | Thickness | 1.5 μ m |
| Method of Saw | | Full Cut |
| Method of Die Bond | | Ablebond 84 - 1 |
| Wire Bond | Method | Thermo Sonic |
| | Material | Au (1.0 mil / 1.3 mil) |
| Leadframe | Material | Cu |
| | Die Area | Ag |
| | Lead Plating | Pb : Sn (37 : 63) |
| Package | Types | 8 Lead PDIP / SO-8 |
| | Materials | EME6300 / MP150 / MP190 |
| Remarks: | | |

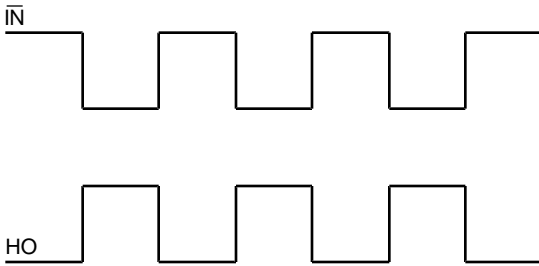


Figure 1. Input/Output Timing Diagram

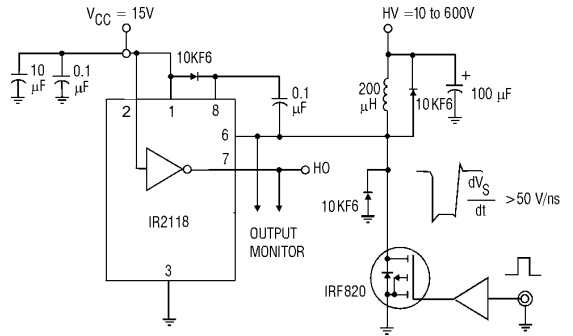


Figure 2. Floating Supply Voltage Transient Test Circuit

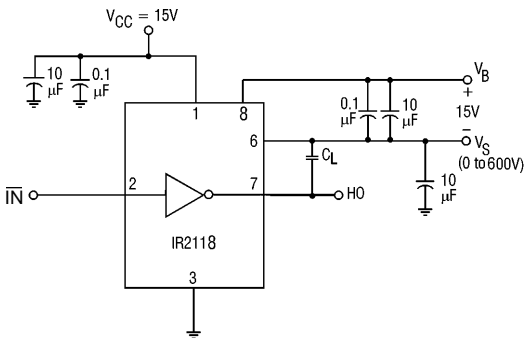


Figure 3. Switching Time Test Circuit

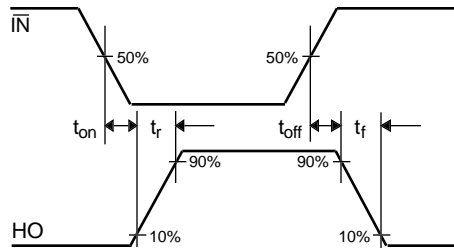


Figure 4. Switching Time Waveform Definition

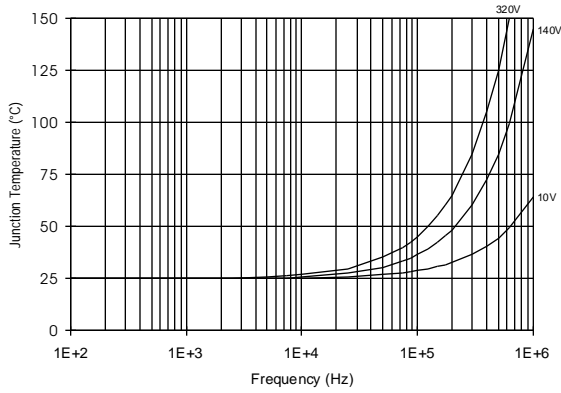


Figure 5. IR2118 T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

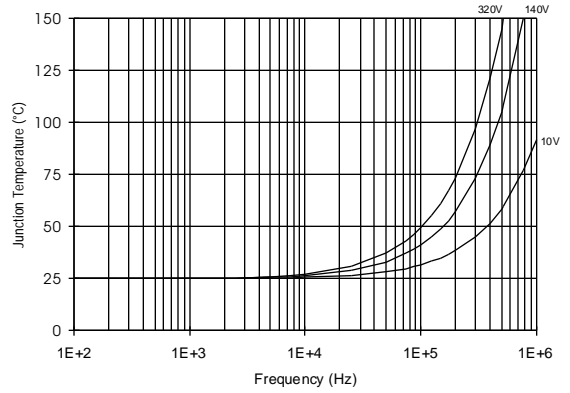


Figure 6. IR2118 T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

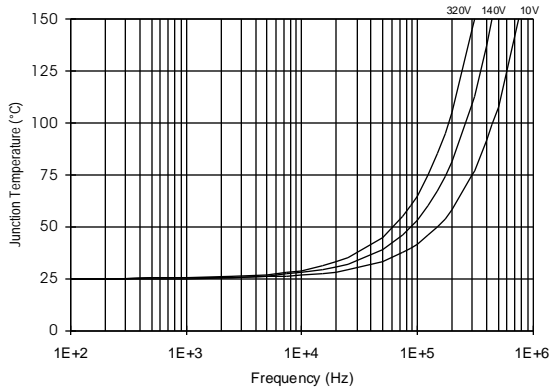


Figure 7. IR2118 T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

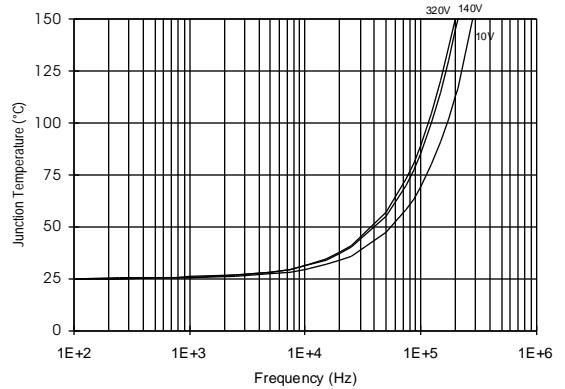


Figure 8. IR2118 T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V