# SONY

# ILX510

## 5150-pixel CCD Linear Sensor (B/W)

### Description

The ILX510 is a reduction type CCD linear sensor developed for high resolution copiers. This sensor reads A3-size documents at a density of 400 DPI, and A4-size documents at a density of 600 DPI at high speed.
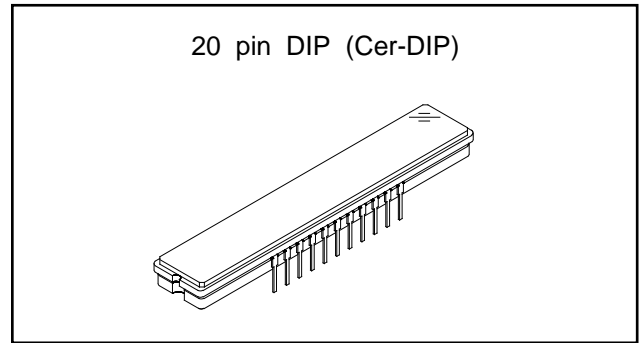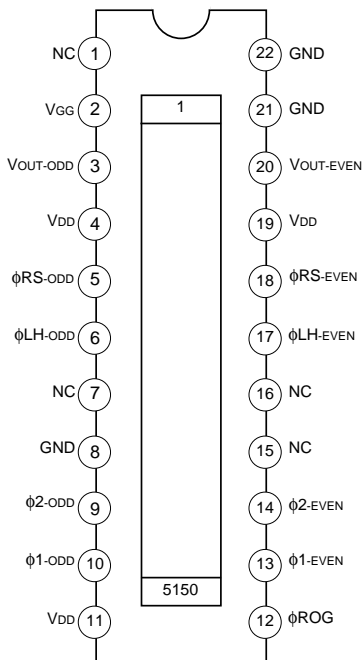
20 pin DIP (Cer-DIP)

### Features

- Number of effective pixels: 5150 pixels
- Pixel size: 7 μm×7 μm (7 μm pitch)
- Signal output phase of two-output simultaneous-output (alternate-output is available)
- Ultra high sensitivity/Ultra low lag
- Max Data Rate: 40 MHz
- Single 12 V power supply
- Input Clock Pulse: CMOS 5V drive
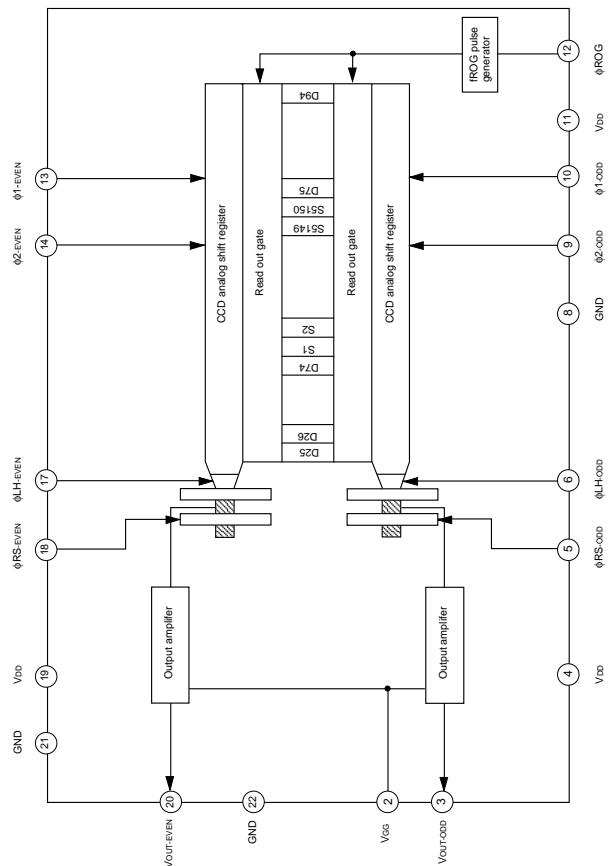- Package: 22 pin cer-DIP (400 mil)

### Absolute Maximum Ratings

- Supply voltage     VDD     15     V
- Operating temperature     −10 to +60     °C
- Storage temperature     −30 to +80     °C

### Pin Configuration (TOP VIEW)

| | | | |
|---|---|---|---|
| NC | 1 | 22 | GND |
| $V_{GG}$ | 2 | 21 | GND |
| $V_{OUT-ODD}$ | 3 | 20 | $V_{OUT-EVEN}$ |
| $V_{DD}$ | 4 | 19 | $V_{DD}$ |
| $\phi RS\text{-ODD}$ | 5 | 18 | $\phi RS\text{-EVEN}$ |
| $\phi LH\text{-ODD}$ | 6 | 17 | $\phi LH\text{-EVEN}$ |
| NC | 7 | 16 | NC |
| GND | 8 | 15 | NC |
| $\phi 2\text{-ODD}$ | 9 | 14 | $\phi 2\text{-EVEN}$ |
| $\phi 1\text{-ODD}$ | 10 | 13 | $\phi 1\text{-EVEN}$ |
| $V_{DD}$ | 11 | 12 | $\phi ROG$ |

### Block Diagram

E94106-TE

## Pin Description

| Pin No | Symbol | Description | Pin No | Symbol | Description |
|--------|--------|-------------|--------|--------|-------------|
| 1 | NC | NC | 12 | $\phi$ROG | Readout gate clock pulse input |
| 2 | V$_{GG}$ | Output circuit gate bias | 13 | $\phi$1-EVEN | Clock pulse input (even pixel) |
| 3 | V$_{OUT-ODD}$ | Signal out (odd pixel) | 14 | $\phi$2-EVEN | Clock pulse input (even pixel) |
| 4 | V$_{DD}$ | 12 V power supply | 15 | NC | NC |
| 5 | $\phi$RS-ODD | Clock pulse input (odd pixel) | 16 | NC | NC |
| 6 | $\phi$LH-ODD | Clock pulse input (odd pixel) | 17 | $\phi$LH-EVEN | Clock pulse input (even pixel) |
| 7 | NC | NC | 18 | $\phi$RS-EVEN | Clock pulse input (even pixel) |
| 8 | GND | GND | 19 | V$_{DD}$ | 12 V power supply |
| 9 | $\phi$2-ODD | Clock pulse input (odd pixel) | 20 | V$_{OUT-EVEN}$ | Signal out (even pixel) |
| 10 | $\phi$1-ODD | Clock pulse input (odd pixel) | 21 | GND | GND |
| 11 | V$_{DD}$ | 12 V power supply | 22 | GND | GND |

## Recommended Supply Voltage

| Item | Min. | Typ. | Max. | Unit |
|------|------|------|------|------|
| V$_{DD}$ | 11.4 | 12 | 12.6 | V |

## Clock Characteristics

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------|--------|------|------|------|------|
| Input capacity of $\phi$1*, f2* | C$\phi$1, C$\phi$2 | — | 400 | — | pF |
| Input capacity of $\phi$LH* | C$\phi$LH | — | 10 | — | pF |
| Input capacity of $\phi$RS* | C$\phi$RS | — | 10 | — | pF |
| Input capacity of $\phi$ROG | C$\phi$ROG | — | 10 | — | pF |

*It indicates that $\phi$1-ODD, $\phi$1-EVEN as $\phi$1, $\phi$2-ODD, $\phi$2-EVEN as $\phi$2, $\phi$LH-ODD, $\phi$LH-EVEN as $\phi$LH, $\phi$RS-ODD, $\phi$RS-EVEN as $\phi$RS.

## Clock Frequency

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------|--------|------|------|------|------|
| $\phi$1, $\phi$2, $\phi$LH, $\phi$RS | f$\phi$1, f$\phi$2,f$\phi$LH,f$\phi$RS | — | 1 | 20 | MHz |
| Data rate | f$\phi$R | — | 2 | 40 | MHz |

## Input Clock Pulse Voltage Condition

| Item | | Min. | Typ. | Max. | Unit |
|------|------|------|------|------|------|
| $\phi$1, $\phi$2, $\phi$LH, $\phi$RS, $\phi$ROG pulse voltage | High level | 4.75 | 5.0 | 5.25 | V |
| | Low level | — | 0 | 0.1 | V |

**Electrooptical Characteristics** (Note 1)

(Ta = 25 °C, V$_{DD}$ = 12 V, Data rate f$_\phi$R=2 MHz, Simultaneous output, Input clock =5 Vp-p

Light source = 3200 K, IR cut filter CM-500S (t = 1.0 mm)

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Sensitivity 1 | R1 | 9 | 12 | 15 | V/(lx ∙ s) | Note2 |
| Sensitivity 2 | R2 | — | 27.4 | — | V/(lx ∙ s) | Note3 |
| Sensitivity nonuniformity | PRNU | — | 4 | 10 | % | Note4 |
| Saturation output voltage | V$_{SAT}$ | 1.0 | 1.5 | — | V | Note5 |
| Saturation exposure | SE | 0.067 | 0.125 | — | lx ∙ s | Note6 |
| Register imbalance | RI | — | 2 | 7 | % | Note7 |
| Dark voltage average | V$_{DRK}$ | — | 0.3 | 2.0 | mV | Note8 |
| Dark signal nonuniformity | DSNU | — | 0.6 | 3.0 | mV | Note9 |
| Image lag | IL | — | 0.02 | — | % | Note10 |
| Supply current | I$_{VDD}$ | — | 30 | 60 | mA | — |
| Total transfer efficiency | TTE | 92 | 98 | — | % | — |
| Output impedance | Z$_O$ | — | 150 | — | Ω | — |
| Offset level | V$_{OS}$ | — | 6.5 | — | V | Note11 |
| Dynamic range | DR | 500 | 5000 | — | — | Note12 |

**Note**

1) In accordance with the given electrooptical characteristics, the even black level is defined as the average value of D6, D8 to D24.  The odd black level is defined as the average value of D5, D7 to D23.

2) For the sensitivity test light is applied with a uniform intensity of illumination.

3) W lamp (2854 K).

4) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.
   V$_{OUT}$=500 mV (Typ.)

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 \ (\%)$$

   Where the 5150 pixels are divided into blocks of 103, even and odd pixels, respectively.  The maximum output of each block is set to V$_{MAX}$, the minimum output to V$_{MIN}$ and the average output to V$_{AVE}$.

5) Use below the minimum value of the saturation output voltage.

6) Saturation exposure is defined as follows.      $SE = \dfrac{V_{SAT}}{R1}$

7) RI is defined as indicated below.  V$_{OUT}$=500 mV (Typ.)

$$RI = \frac{|V_{ODD\text{-}AVE} - V_{EVEN\text{-}AVE}|}{\left(\dfrac{V_{ODD\text{-}AVE} + V_{EVEN\text{-}AVE}}{2}\right)} \times 100 \ (\%)$$

   Where average of odd pixels output is set to V$_{ODD\text{-}AVE}$, even pixels to V$_{EVEN\text{-}AVE}$.

8) Optical signal accumulated time $\tau$ int stands at 10 ms.

9) The difference between the maximum and average values of the dark output voltage is calculated for even and odd respectivery. The larger value is defined as the dark signal nonuniformity.
   Optical signal accumulated time t int stands at 10 ms.

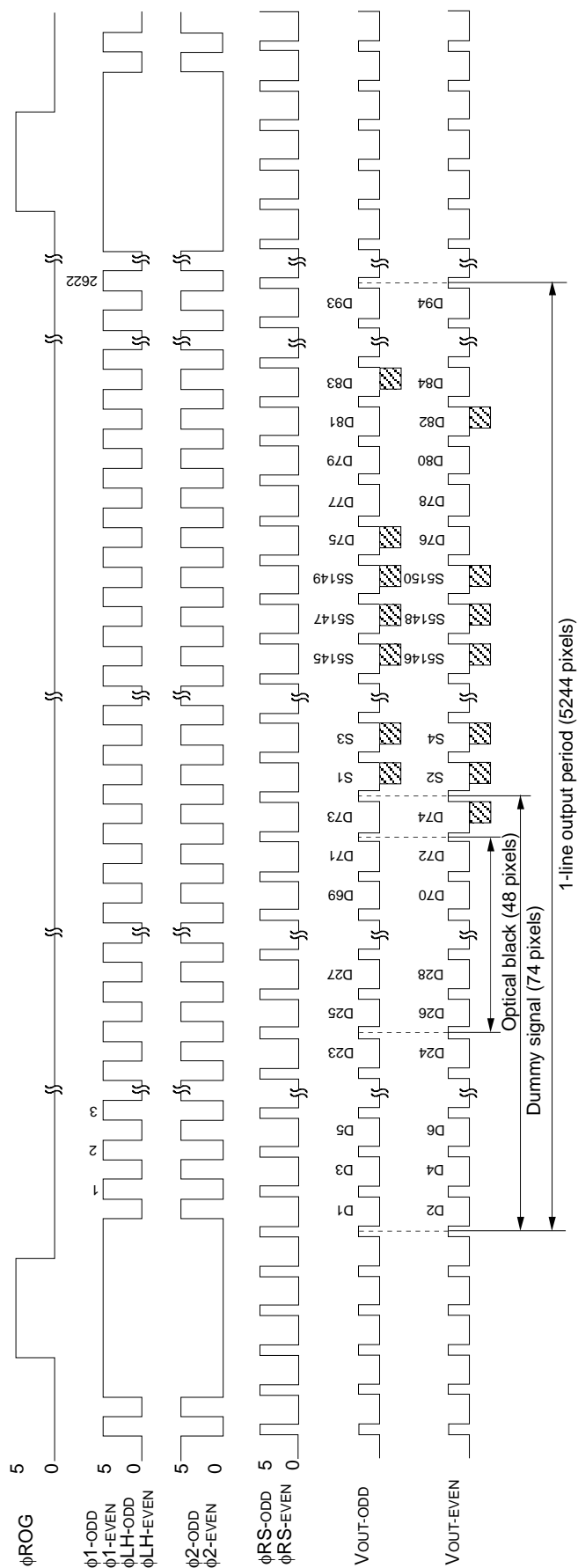10) $V_{OUT}$ = 500 mV (Typ.)

11) Vos is defined as indicated bellow.
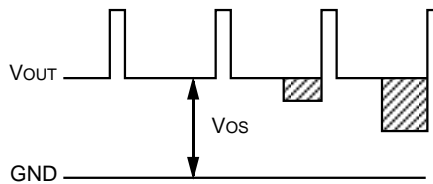


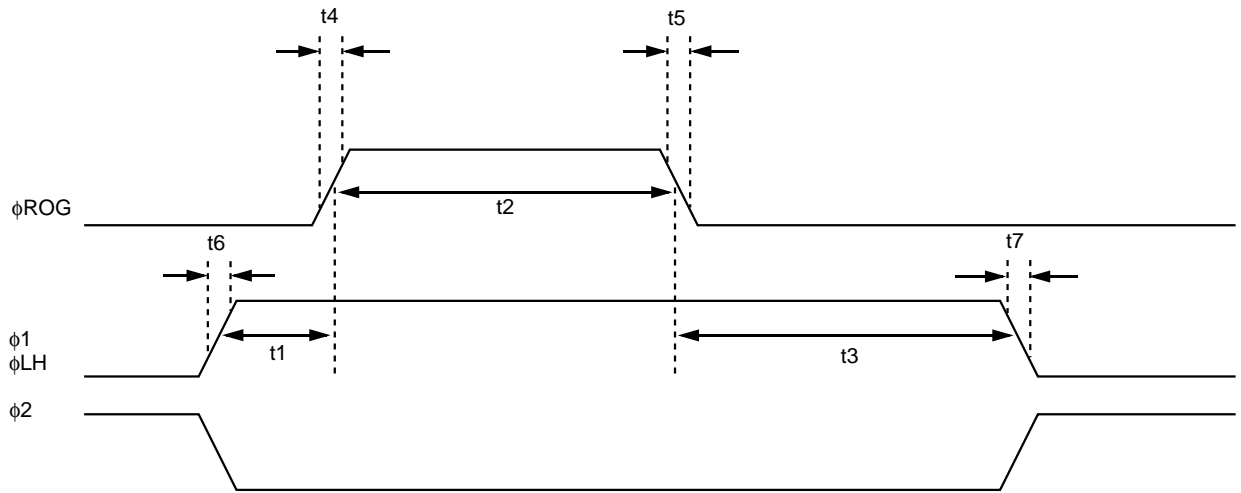12) Dynamic range is defined as follows.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

When the optical signal accumulated time is shorter, the dynamic range gets wider because the optical signal accumulated time is in proportion to the dark voltage.
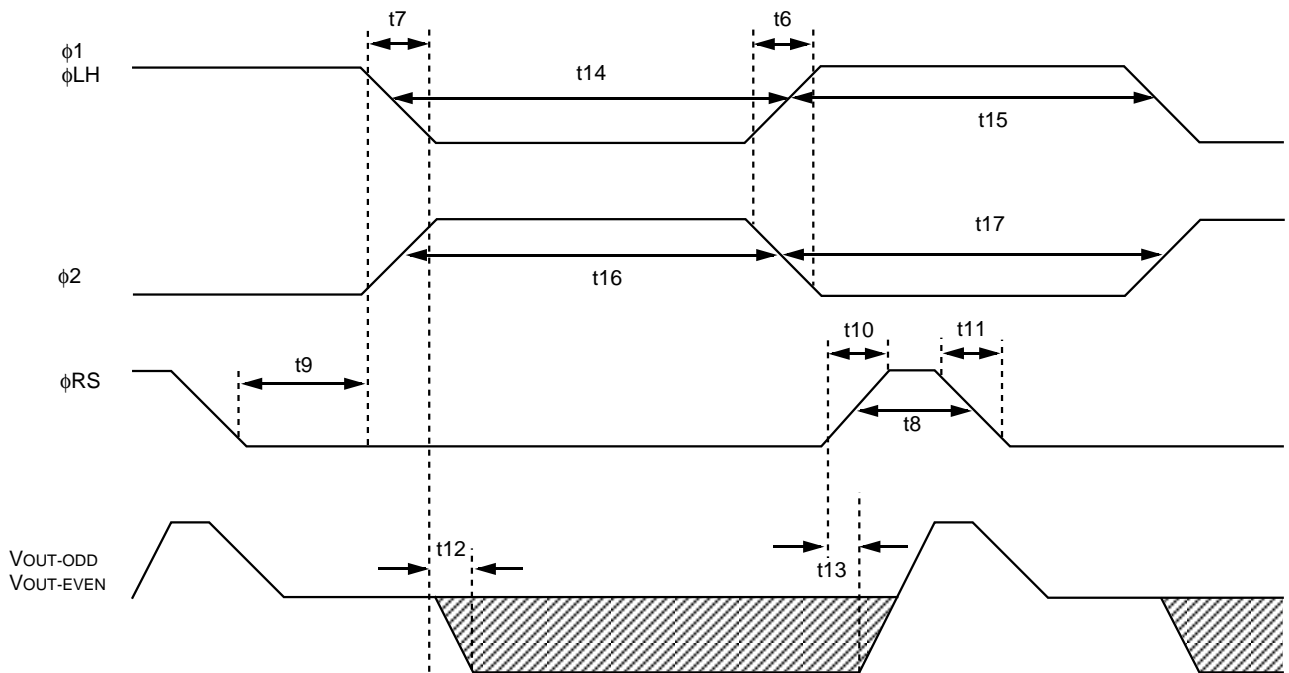
**Clock Timing Chart 1 (simultaneous output)**



φROG

φ1-ODD
φ1-EVEN
φLH-ODD
φLH-EVEN

φ2-ODD
φ2-EVEN

φRS-ODD
φRS-EVEN

V$_{OUT}$-ODD

V$_{OUT}$-EVEN

Optical black (48 pixels)

Dummy signal (74 pixels)

1-line output period (5244 pixels)

Note) The transfer pulses (φ1, φ2, φLH) must have more than 2622 cycles.

**Clock Timing Chart 2**



**Clock Timing Chart 3**



Clock timing of $\phi 1$, $\phi 2$, $\phi LH$, $\phi RS$, and $V_{OUT}$ at odd or even are the same as timing chart 3 in the case of alternate output.

**Clock Timing Chart 4**

Cross point φ1 and φ2

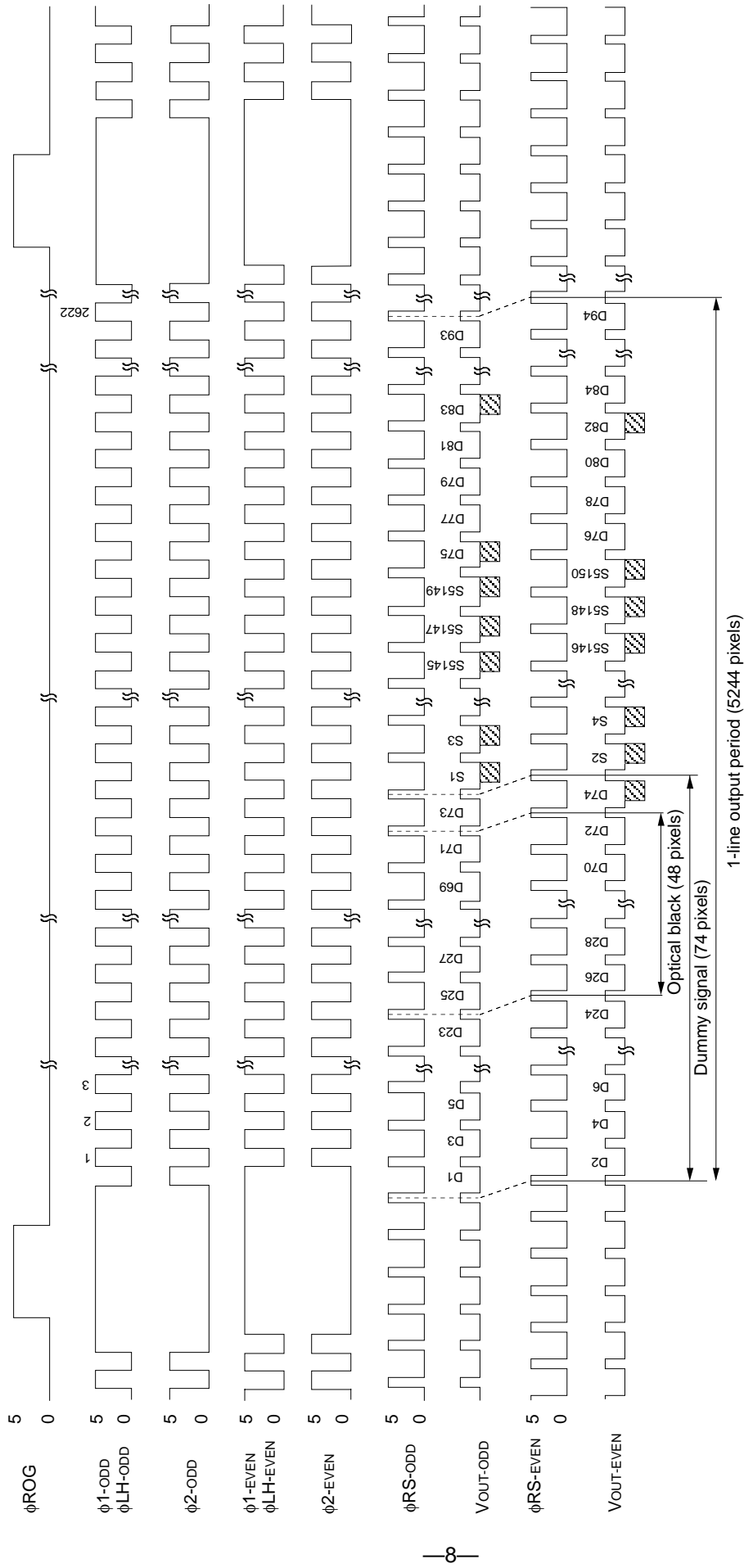φ1    5V

φ2    0V

1.5V (Min.)

1.5V (Min.)

Cross point φLH and φ2

φ2    5V

φLH  0V

2.0V (Min.)

0.5V (Min.)
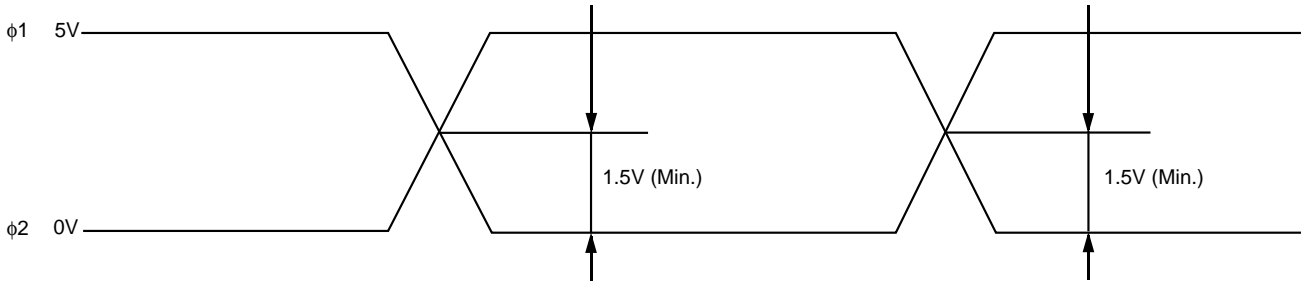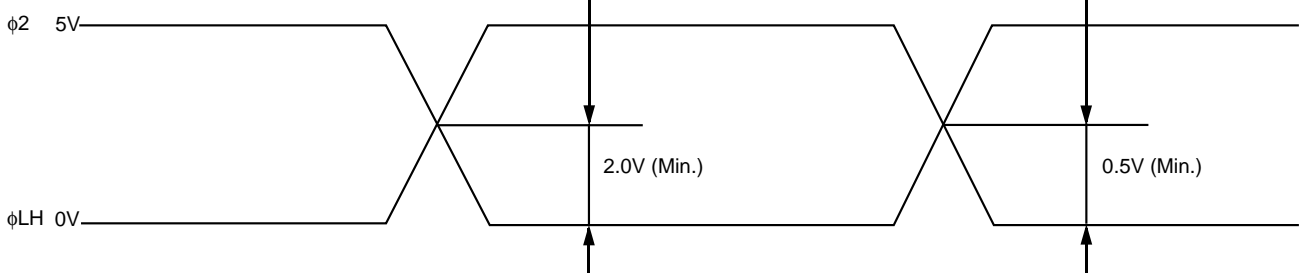
**Clock Timing Chart 5 (alternate output)**



Note) The transfer pulses (φ1, φ2, φLH) must have more than 2622 cycles.

*Alternate output is available by making φ1-EVEN, φ2-EVEN, φLH-EVEN, φRS-EVEN delayed to φ1-ODD, φ2-ODD, φLH-ODD, φRS-ODD for half a cycle.

**Clock Pulse Recommended Timing**

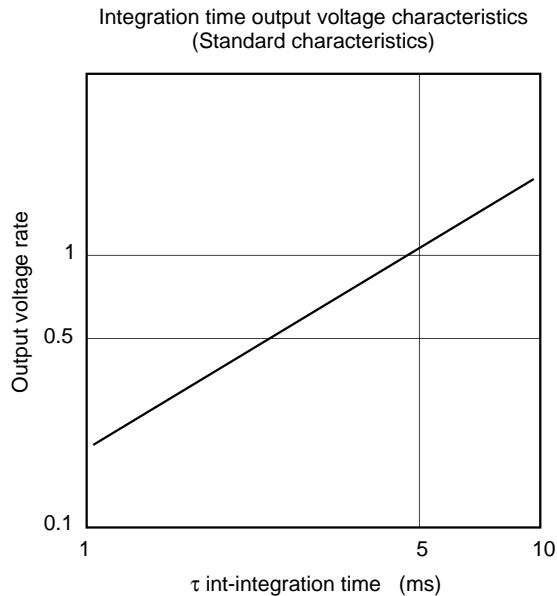| | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| φROG, φ1pulse timing | t1 | 50 | 100 | — | ns |
| φROG pulse high level period | t2 | 600 | 1000 | — | ns |
| φROG, φ1 pulse timing | t3 | 400 | 1000 | — | ns |
| φROG pulse rise time | t4 | 0 | 5 | 10 | ns |
| φROG pulse fall time | t5 | 0 | 5 | 10 | ns |
| φ1 pulse rise time /φ2 pulse fall time | t6 | 0 | 20 | 60 | ns |
| φ1 pulse fall time / φ2 pulse rise time | t7 | 0 | 20 | 60 | ns |
| φRS pulse high level period | t8 | 20 | 250* | — | ns |
| φRS, φLH pulse timing | t9 | 0 | 250* | — | ns |
| φRS pulse rise time | t10 | 0 | 10 | 30 | ns |
| φRS pulse fall time | t11 | 0 | 10 | 30 | ns |
| Signal output delay time | t12 | — | 8 | — | ns |
| | t13 | — | 8 | — | ns |
| φ1, φLH pulse low level period/φ2 pulse high level period | t14, t16 | 25 | 500* | — | ns |
| φ1, φLH pulse high level period/φ2 pulse low level period | t15, t17 | 25 | 500* | — | ns |

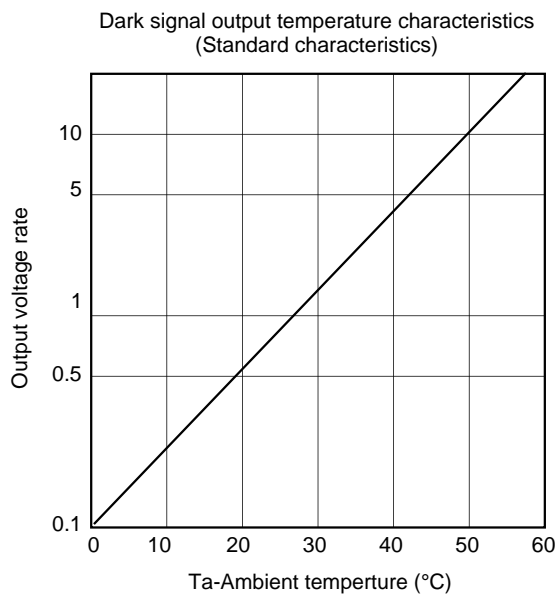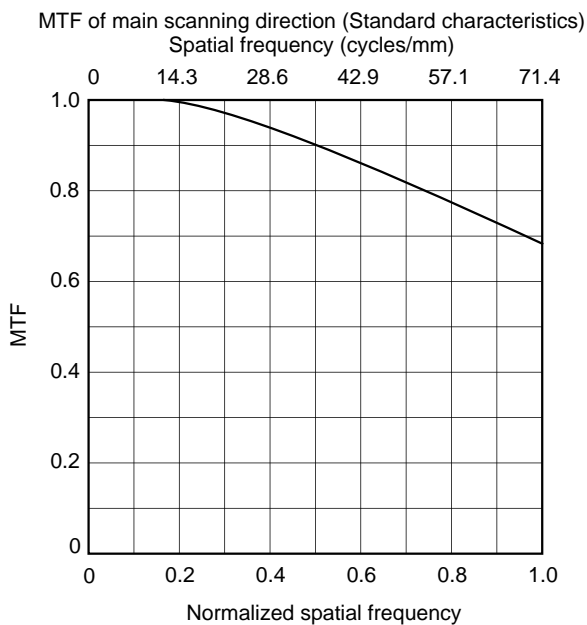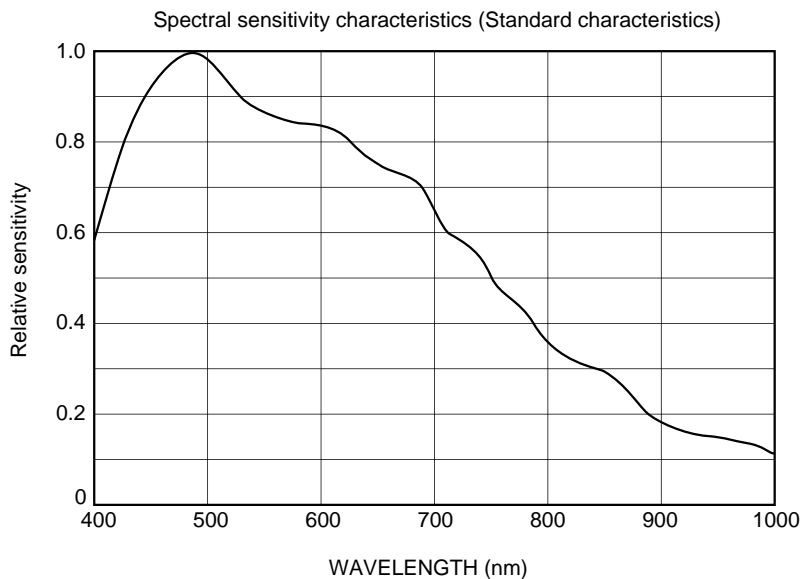(∗) These timing is the recommended condition under fφ1=1 MHz.

## Application Circuit * (inphase output)

IC1 : 74AC04
Tr1 : 2SC2785
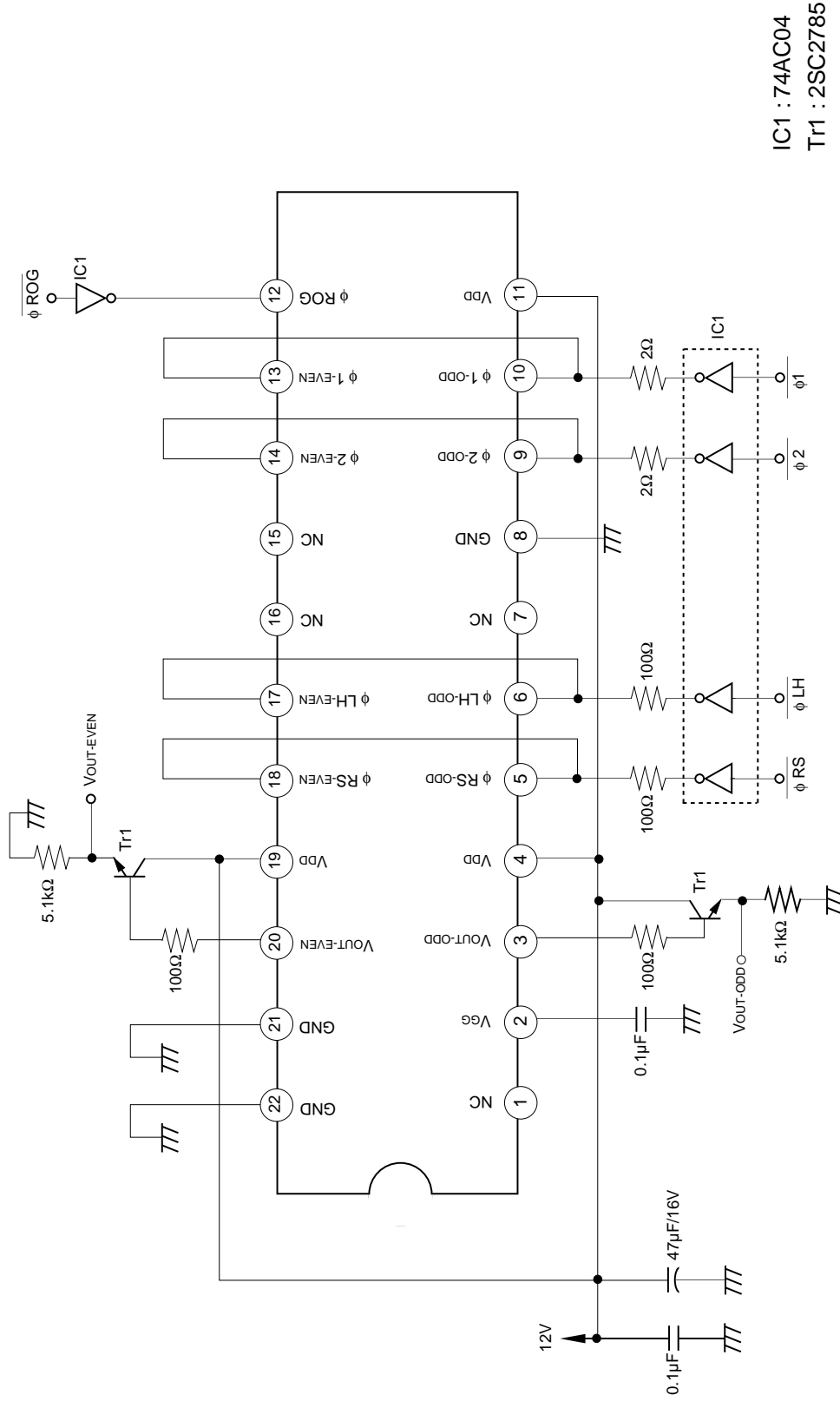


*Data rate f$\phi$R = 2 MHz

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

## Example of Representative Characteristics  (V$_{DD}$ = 12 V, Ta = 25 °C)

Spectral sensitivity characteristics (Standard characteristics)



WAVELENGTH (nm)

MTF of main scanning direction (Standard characteristics)
Spatial frequency (cycles/mm)



Normalized spatial frequency

Dark signal output temperature characteristics
(Standard characteristics)



Ta-Ambient temperture (°C)

Integration time output voltage characteristics
(Standard characteristics)



$\tau$ int-integration time   (ms)

Operational frequency response of supply supply current
(Standard characteristics)

Ta = 25°C

$|V_{DD}$-supply current (mA)

Data rate $f\phi_R$ (MHz)
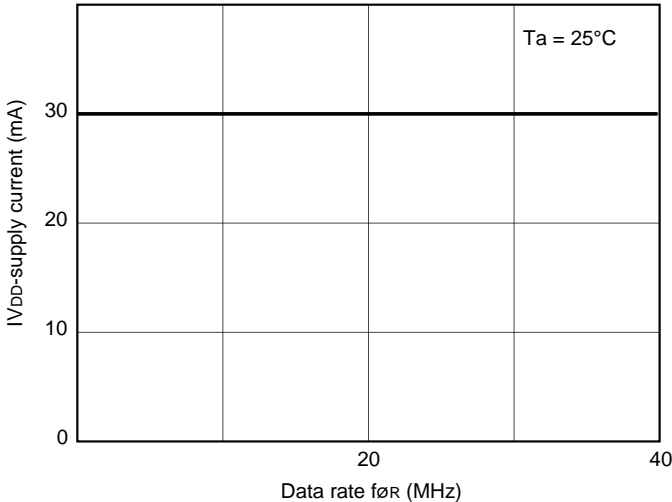
Offset level vs. $V_{DD}$ characteristics
(Standard characteristics)

Ta = 25°C

$V_{OS}$-Offset level (V)

$$\frac{\Delta V_{OS}}{\Delta V_{DD}} \simeq -0.2$$

$V_{DD}$ (V)
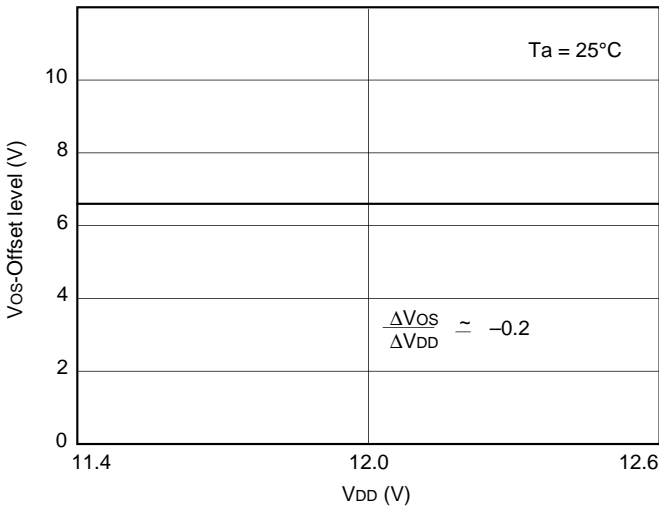
Offset level vs. Temperature characteristics
(Standard characteristics)

$$\frac{\Delta V_{OS}}{\Delta T_a} \simeq 8 \text{ mV/°C}$$

$V_{OS}$-Offset level (V)

Ta-Ambient temperature (°C)
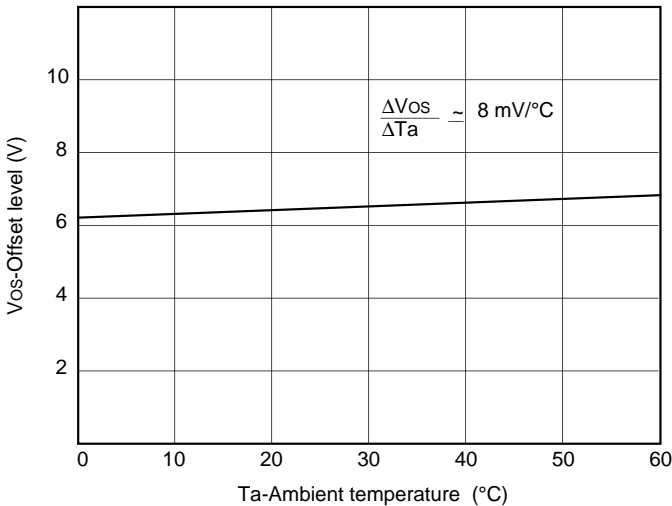
**Notes of Handling**

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.

   b) When handling directly use an earth band.

   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

   d) Ionized air is recommended for discharge when handling CCD image sensor.

   e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

   a) Remain within the following limits when applying static load to the ceramic portion of the package:

   (1) Compressive strength: 39 N/surface (Do not apply load more than 0.7 mm inside the outer perimeter of the glass portion.)

   (2) Shearing strength: 29 N/surface

   (3) Tensile strength: 29 N/surface

   (4) Torsional strength: 0.9 Nm

   b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
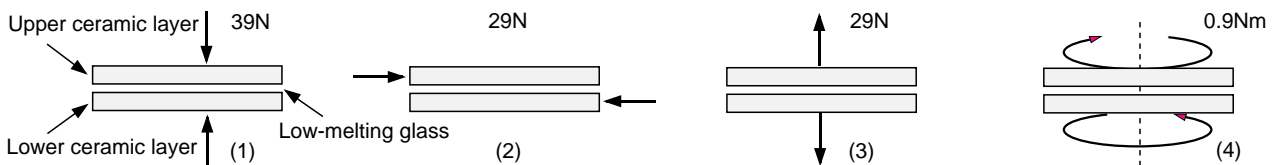


   c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

   (1) Applying repetitive bending stress to the external leads.

   (2) Applying heat to the external leads for an extended period of time with soldering iron

   (3) Rapid cooling or heating

   (4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

   (5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.
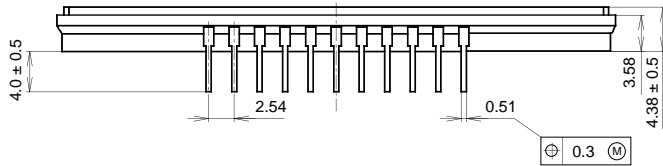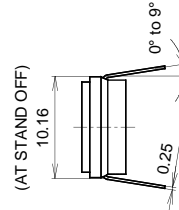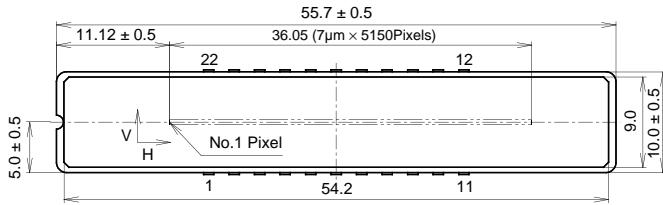
3) Soldering

   a) Make sure the package temperature does not exceed 80 °C.

   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30 W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.

   c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection

   a) Operate in clean environments.

   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.

   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

## Package Outline   Unit : mm

22pin DIP (400mil)



55.7 ± 0.5

11.12 ± 0.5     36.05 (7µm × 5150Pixels)

22                    12

9.0    10.0 ± 0.5

5.0 ± 0.5

V

H         No.1 Pixel

1          54.2          11

(AT STAND OFF)   10.16

0° to 9°

0.25

4.0 ± 0.5

2.54          0.51

3.58    4.38 ± 0.5

⊕  0.3  Ⓜ

1.  The height from the bottom to the sensor surface is 2.38 ± 0.3mm.

2.  The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

| PACKAGE MATERIAL | Cer-DIP |
|---|---|
| LEAD TREATMENT | TIN PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE WEIGHT | 7.1g |