3.3V CMOS 18-BIT READ/WRITE BUFFER WITH 5 VOLT TOLERANT I/O

IDT74LVCH16702A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH16702A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

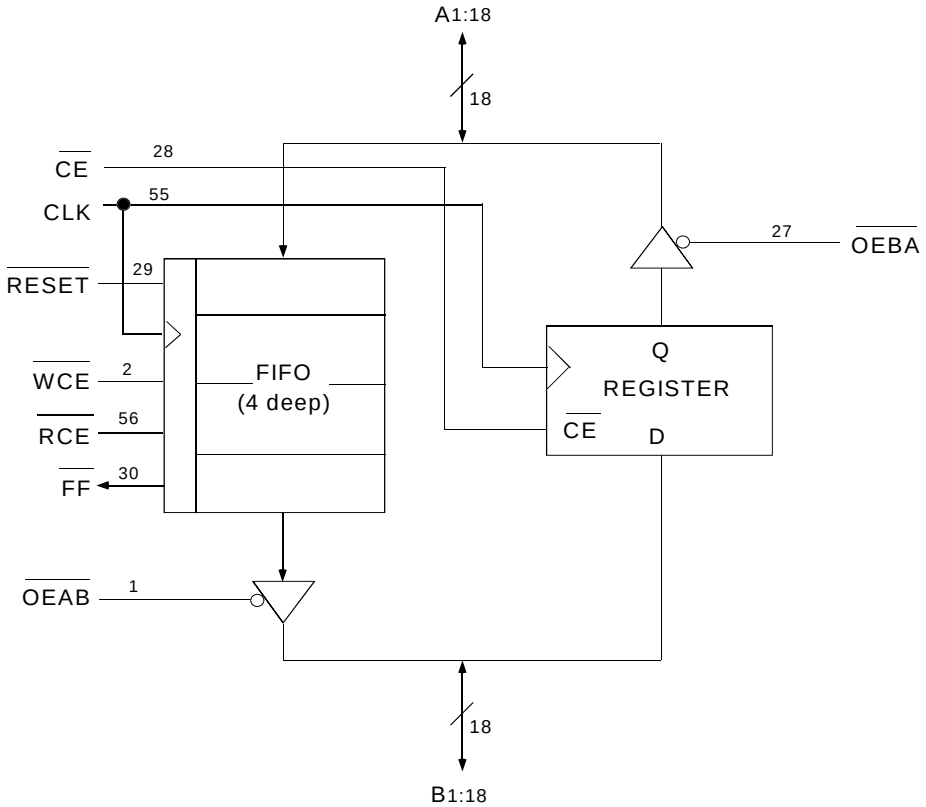
The LVCH16702A 18-bit read/write buffer is built using advanced dual metal CMOS technology. The device is designed as an 18-bit read/write buffer with a four deep FIFO and a read-back latch. It can be used as a read/write buffer between a CPU and a memory or to interface a high-speed bus and a slow peripheral. The A-to-B (write) path has a four deep FIFO for pipelined operations. The FIFO can be reset and a FIFO full condition is indicated by the full flag ($\overline{FF}$). The B-to-A (read) path has a latch.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

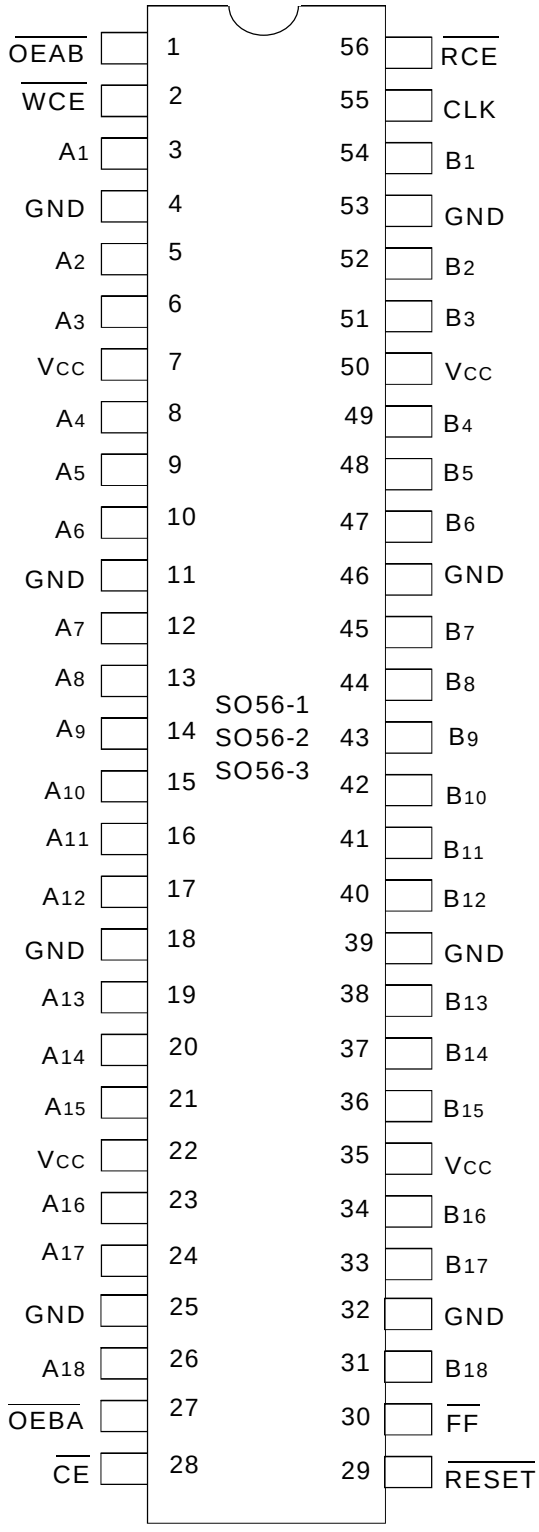
The LVCH16702A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16702A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	– 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

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NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	I/O	Description
A_{1-18}	I/O	18 bit I/O port.
B_{1-18}	I/O	18 bit I/O port.
CLK	I	Clock Input.
$\overline{WCE}$	I	Enable pin for FIFO input clock. When $\overline{WCE}$ is low data clocks into the FIFO on the rising edge of CLK.
$\overline{RCE}$	I	Enable pin for FIFO output clock. When $\overline{RCE}$ is low data clocks out of the FIFO on the rising edge of CLK.
$\overline{FF}$	O	Write path FIFO full flag. Goes low when FIFO is full. When FIFO is full all further writes to the FIFO are inhibited. When FIFO is empty all reads from the FIFO are inhibited.
$\overline{RESET}$	I	Synchronous FIFO reset - when low CLK resets the FIFO. The FIFO pointers are initialized to the "empty" condition and FIFO output is forced high (all ones). The FIFO full flag ($\overline{FF}$) will be high immediately after reset.
$\overline{OEAB}$	I	Output Enable pin for B port.
$\overline{OEBA}$	I	Output Enable pin for A port.
$\overline{CE}$	I	Clock Enable pin for B to A register.

NOTE:
1. These pins have “Bus-hold”. All other pins are standard inputs, outputs, or I/Os.

FUNCTIONAL TABLE (1)

INPUTS				OUTPUTS		Notes
$\overline{OEBA}$	$\overline{OEAB}$	$\overline{CE}$	CLK	A	B	
L	H	L	↑	B to A	B Bus Activity	
L	H	H	↑	Q_0(A)	B Bus Activity	
H	H	L	↑	Q_0(A)Bus Hold		
H	L	X	↑		A to B signal is delayed by 4 clocks	See timing diagram
L	L	L	↑		Q_0(A) - 5 clocks	Case not recommended
L	L	H	↑	Q_0(B)	Q_0(A) - 5 clocks	Case not recommended
H	H	H	↑	Q_0(A)Bus Hold	Q_0(B) Bus hold	

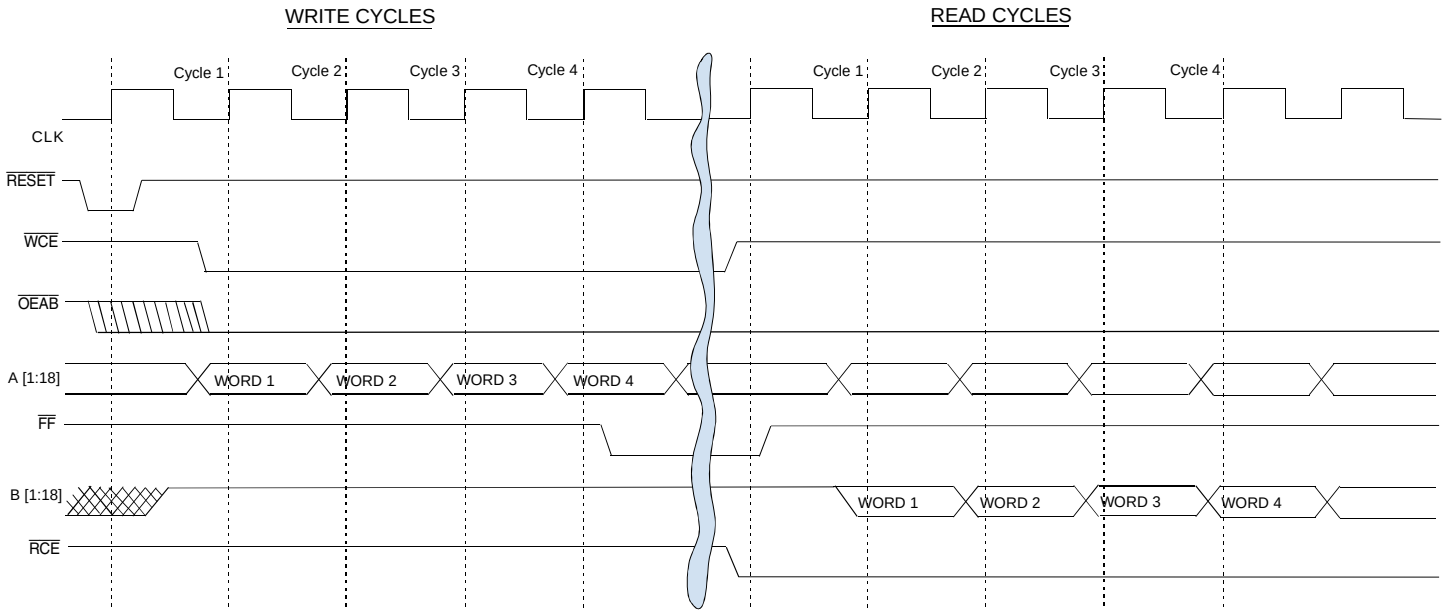
NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don’t Care
   ↑ = Low-to-High Transition
   Q_0 = Level of Q before the indicated steady-state input conditions were established.

FUNCTIONAL DESCRIPTION

This device is useful as a read/write buffer for modular high end designs. It provides multi-level buffering in the write path and single deep buffering in the read path, and is suited to write back cache implementation. The read path provides a register for full synchronous operation.

The four deep FIFO uses one clock with two clock enable pins, $\overline{WCE}$ and $\overline{RCE}$ to clock data in and out. The FIFO has an external full flag which goes LOW when the FIFO is full. Internal read and write pointers keep track of the words stored in the FIFO. A write attempt to a full FIFO is ignored. An attempt to read from an empty FIFO will have no effect and the last read data remains at the output of the FIFO. The FIFO may be reset by the synchronous $\overline{RESET}$ input. This resets the read and write pointers to the original “empty” condition and also sets all B outputs = 1. Simultaneous read and write attempts (clock data into FIFO as well as clock data out of FIFO) are possible except on FIFO empty and full boundaries. When the FIFO is empty, and a simultaneous read and write is attempted, the read is ignored while the write is executed. If the same is attempted when the FIFO is full, the write is ignored while the read is executed. Normal operation of the four deep FIFO in the write path is independent of the read path operation.

TIMING DIAGRAM



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
I_{CCZ}			$3.6 \leq V_{IN} \leq 5.5V$(2)	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V other inputs at V_{CC} or GND		—	—	500	µA

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NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	—	—	—	µA
I_{BHL}			V_I = 0.7V	—	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation WCE Mode $\overline{OEAB}$ = 0	C_L = 0pF, f = 10Mhz		pF
C_{PD}	Power Dissipation in RCE mode $\overline{OEBA}$ = 0			pF
C_{PD}	Registered channel (B to A) Power Dissipation $\overline{OEBA}$ = 0; $\overline{CE}$ = 0			pF
C_{PD}	Registered channel Power Dissipation $\overline{OEBA}$ = 0: $\overline{CE}$ = 1			pF

SWITCHING CHARACTERISTICS (1)

	Parameter	Test Conditions	Vcc = 2.7V		Vcc = 3.3V±0.3V		Unit
			Min.	Max.	Min.	Max.	
PROPAGATION DELAYS							
1	CLK to $A_{1\text{-}18}$	Read path/register	—	7.5	—	6.5	ns
2	CLK to $\overline{FF}$	Write path	—	8.2	—	7.2	ns
3	CLK to $B_{1\text{-}18}$	Write path	—	7.5	—	6.5	ns
4	Output Skew(2)	Write path	—	—	—	1	ns
SETUP & HOLD TIMES							
5	$A_{1\text{-}18}$, $B_{1\text{-}18}$ to CLK (LOW to HIGH) Setup	Write path	2.1	—	1.8	—	ns
6	$A_{1\text{-}18}$, $B_{1\text{-}18}$ to CLK (LOW to HIGH) Hold	Write path	1.3	—	1	—	ns
7	$\overline{CE}$ (LOW) to CLK Setup	Read path/register	2.4	—	2.1	—	ns
8	$\overline{CE}$ (LOW) to CLK Hold	Read path/register	1.3	—	1	—	ns
9	$\overline{WCE}$, $\overline{RCE}$ (LOW) to CLK Setup	Write path	3.8	—	3	—	ns
10	$\overline{WCE}$, $\overline{RCE}$ (LOW) to CLK Hold	Write path	1	—	0.7	—	ns
11	$\overline{RESET}$ (LOW) to CLK Setup	Write path	2.1	—	1.8	—	ns
12	$\overline{RESET}$ (LOW) to CLK Hold	Write path	1.3	—	1	—	ns
ENABLE & DISABLE TIMES							
13	$\overline{OEBA}$ LOW to $A_{1\text{-}18}$ Enable	Write path	—	7	—	6	ns
14	$\overline{OEBA}$ HIGH to $A_{1\text{-}18}$ Disable	Write path	—	7	—	6	ns
15	$\overline{OEAB}$ LOW to $B_{1\text{-}18}$ Enable	Read path	—	7	—	6	ns
16	$\overline{OEAB}$ HIGH to $B_{1\text{-}18}$ Disable	Read path	—	7	—	6	ns
MINIMUM PULSE WIDTHS							
17	CLK HIGH or LOW Pulse Width	Write path/READ	6	—	5	—	ns
18	Clock cycle frequency		—	—	—	75	MHz
19	Clock cycle time		—	—	13	—	ns

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V ±0.3V	$V_{CC}^{(1)}$ = 2.7V	$V_{CC}^{(2)}$= 2.5V ±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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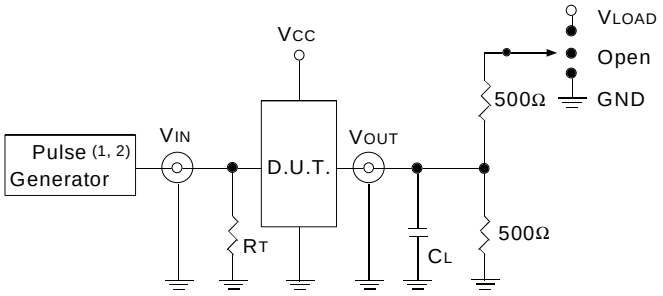
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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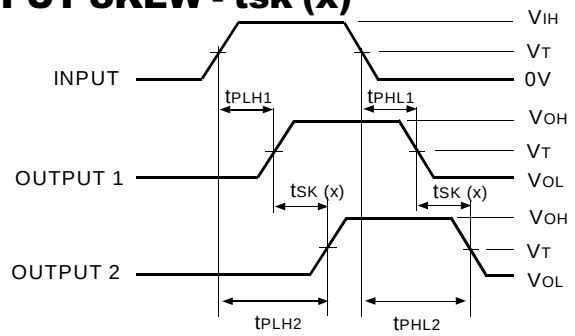
OUTPUT SKEW - tsk (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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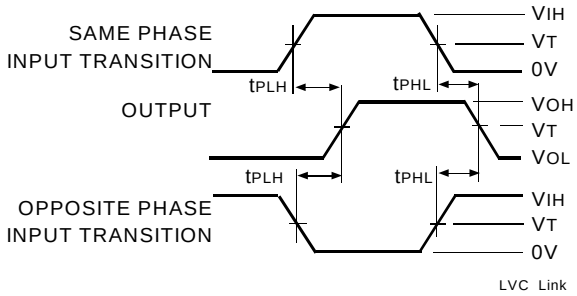
NOTES:
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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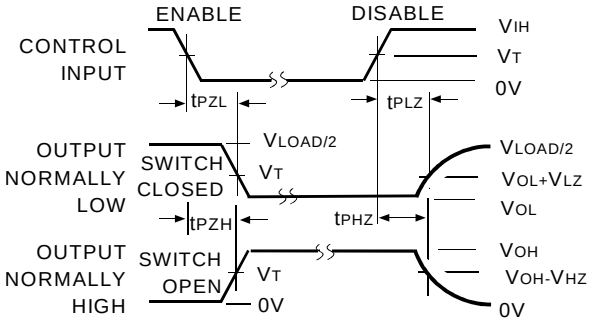
ENABLE AND DISABLE TIMES



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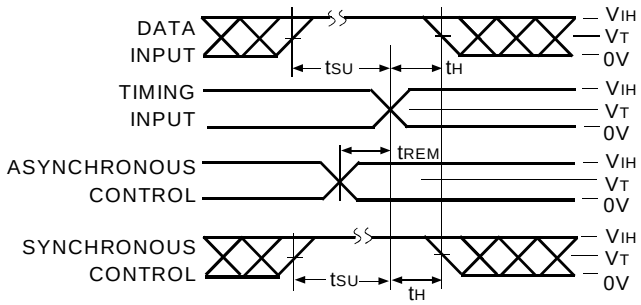
NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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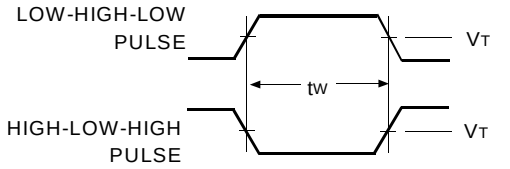
PULSE WIDTH



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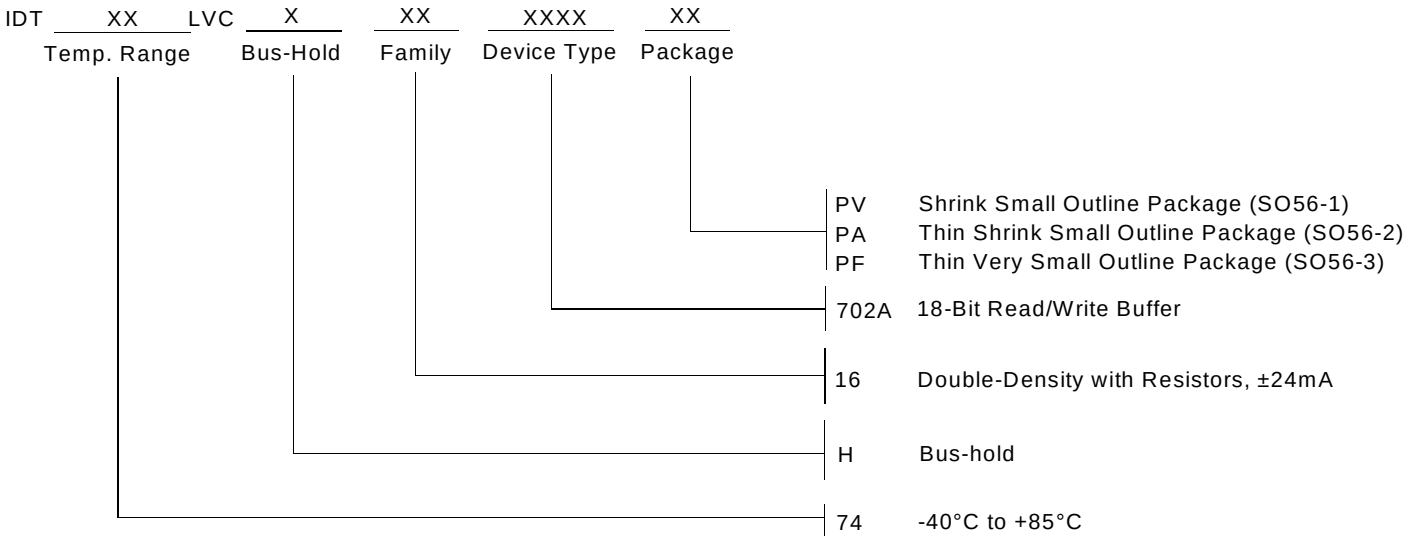
ORDERING INFORMATION



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